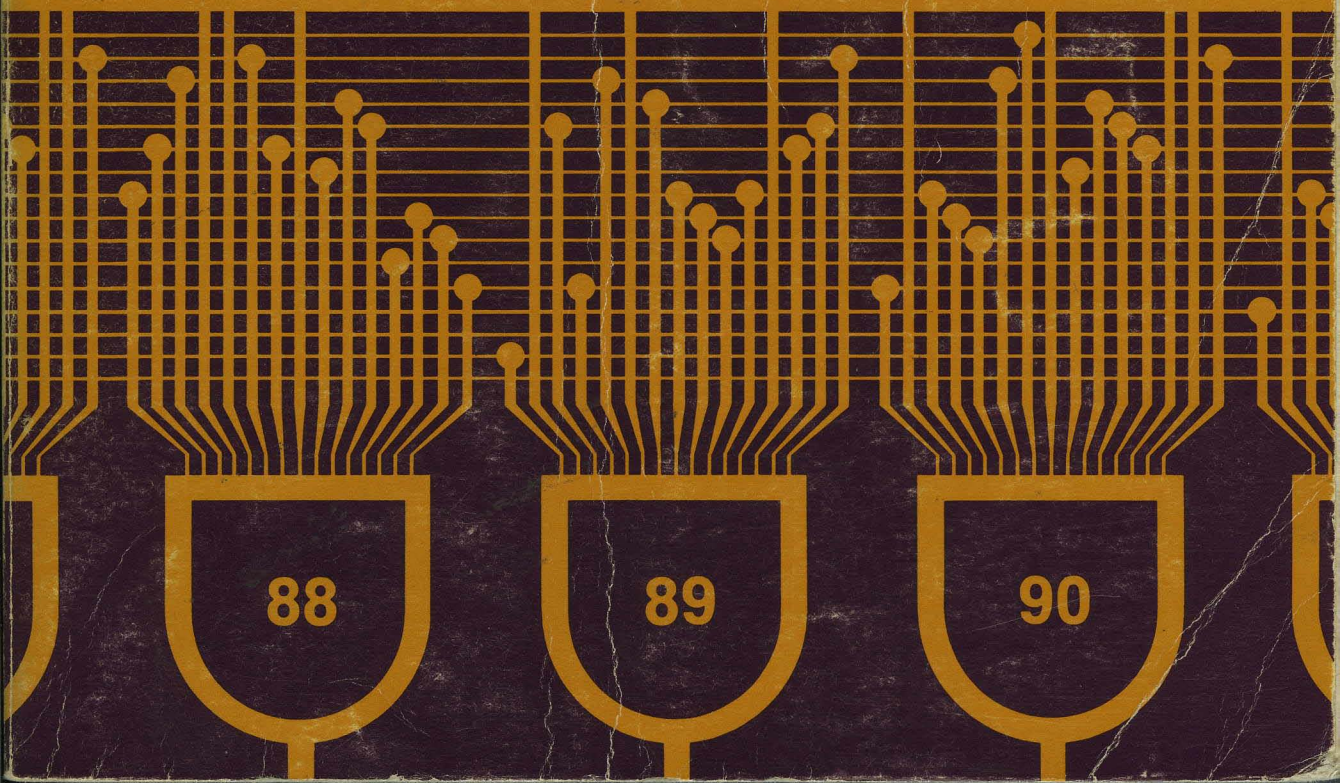
DIGITAL INTEGRATED CIRCUITS

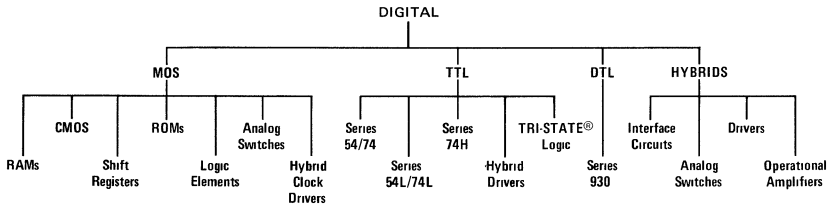
National

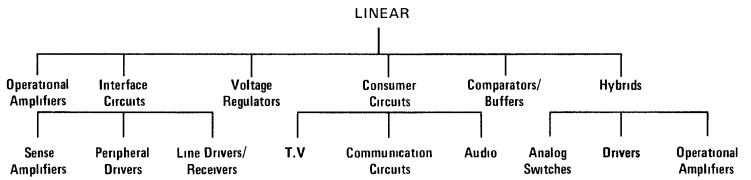


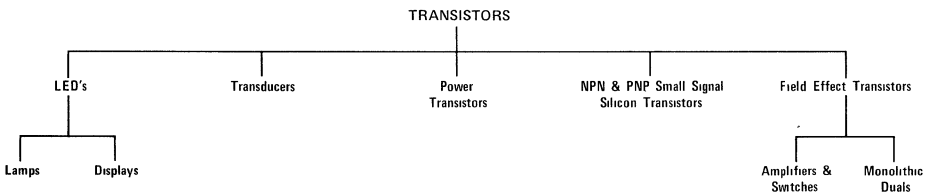
Introduction

Here is the new Digital Data Handbook from National It gives complete specifications for devices useful in building nearly all types of electronic systems, from small instruments to computer designs

For information regarding newer devices introduced since the printing of this handbook, or for further information on listed parts, please contact our local representative, distributor, or regional office



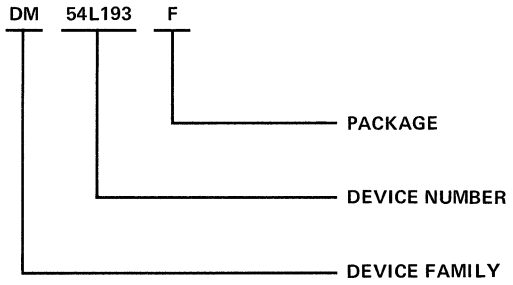




Ordering Information

For available packages, consult the tables which precede each section. Then refer to the package drawings (pages I through VI) in the back of the catalog.

The ordering information for National devices covered in this catalog is as follows:



DEVICE FAMILY

AH – Analog Hybrid
AM – Analog Monolithic
DM – Digital Monolithic
LH – Linear Hybrid
LM – Linear Monolithic
MM – MOS Monolithic

DEVICE NUMBER

4, 5, or 6 digit number.
Suffix Indicators:
A – Improved Electrical Specification
C – Reduced Temperature Range

PACKAGE

D – Glass/Metal Dual-In-Line Package
F – Flat Package (0 25" wide)
G – TO-8 (12 lead) Metal Can
H – TO-5 (multi-lead) Metal Can
J – Glass/Glass Dual-In-Line Package
N – Molded Dual-In-Line Package
W – Flat Package (0.275" wide)

For most of the products listed in this catalog the temperature range can be obtained from the first one or two numbers following the family designation. For example:

DM54XX	All numbers beginning with 5 denote $-55^{\circ}C$ to $+125^{\circ}C$ temperature operation.
DM74XX	If the "74" is indicated, the operating temperature is $0^{\circ}C$ to $+70^{\circ}C$.
DM7XXX	All other numbers beginning with 7 (besides the "74" shown above) are NSC proprietary products and a 7 here indicates $-55^{\circ}C$ to $+125^{\circ}C$.
DM8XXX	All numbers beginning with 8 denote $0^{\circ}C$ to $+70^{\circ}C$ temperature operation.

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SERIES 54/74 – SECTION 1 (CONTINUED)

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SERIES 54L/74L — SECTION 3 (CONTINUED)

SERIES 74S — SECTION 4

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SERIES 10000 — SECTION 7

SERIES 10000 — SECTION 7 (CONTINUED)

CMOS — SECTION 8

INTERFACE CIRCUITS — SECTION 9

INTERFACE CIRCUITS – SECTION 9 (CONTINUED)

Edge Index by Product Family

Product Function Guide

GATES

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DM5401/DM7401
DM5402/DM7402
DM5403/DM7403
DM5404/DM7404
DM5405/DM7405
DM5408/DM7408
DM5409/DM7409
DM5410/DM7410
DM5411/DM7411
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DM5453/DM7453
DM5454/DM7454
DM5460/DM7460
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DM7090/DM8090
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DM7092/DM8092

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DM54H01/DM74H01
DM54H04/DM74H04
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DM54H11/DM74H11
DM54H20/DM74H20
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DM54H22/DM74H22
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DM54H40/DM74H40
DM54H50/DM74H50
DM54H51/DM74H51
DM54H52/DM74H52
DM54H53/DM74H53
DM54H54/DM74H54
DM54H55/DM74H55
DM54H60/DM74H60
DM54H61/DM74H61
DM54H62/DM74H62

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DM54L02/DM74L02
DM54L03/DM74L03
DM54L04/DM74L04
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DM54L30/DM74L30
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DM54L51/DM74L51
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DM74S22
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DM74S135

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DM9003C
DM9004C
DM9005C
DM9006C
DM9008C
DM9009C
DM9012C
DM9016C

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DM10102
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DM10121

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DM5407/DM7407
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DM5437/DM7437
DM5438/DM7438
DM5440/DM7440
DM54125/DM74125
DM54126/DM74126
DM7093/DM8093
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DM74S140

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DM5473/DM7473
DM5474/DM7474
DM5475/DM7475
DM5476/DM7476
DM54107/DM74107
DM54173/DM74173
DM54174/DM74174
DM54175/DM74175
DM7511/DM8511

FLIP FLOPS LATCHES STORAGE REGISTERS (con't)

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DM7551/DM8551
DM7553/DM8553
DM7613/DM8613

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DM54H72/DM74H72
DM54H73/DM74H73
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DM75L12/DM85L12
DM75L51/DM85L51
DM76L13/DM86L13

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DM74S112
DM74S113
DM74S114

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DM9099

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DM54192/DM74192
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DM54196/DM74196
DM54197/DM74197
DM7280/DM8280
DM7281/DM8281
DM7288/DM8288
DM7290/DM8290
DM7291/DM8291
DM7520/DM8520
DM7552/DM8552
DM7554/DM8554
DM7555/DM8555
DM7556/DM8556
DM7560/DM8560
DM7563/DM8563

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DM54L93/DM74L93
DM54L192/DM74L192
DM54L193/DM74193
DM75L52/DM85L52
DM75L54/DM85L54
DM76L75/DM86L75
DM76L76/DM86L76
DM76L93/DM86L93

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DM5495/DM7495
DM5496/DM7496
DM54164/DM74164
DM54165/DM74165
DM54166/DM74166
DM54195/DM74195
DM54198/DM74198
DM54199/DM74199
DM7570/DM8570
DM7590/DM8590

DM54L91/DM74L91
DM54L95/DM74L95
DM54L165A/DM74L165A
DM76L70/DM86L70
DM76L90/DM86L90

DM9300/DM8300

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DM54156/DM74156
DM54157/DM74157
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DM7223/DM8223
DM7230/DM8230
DM7875A/DM8875A
DM7875B/DM8875B
DM71L22/DM81L22
DM71L23/DM81L23
DM74S151/DM74S251
DM74S153/DM74S253
DM74S157/DM74S257
DM74S158/DM74S258
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DM9312/DM8312
DM9322/DM8322

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DM5446A/DM7446A
DM5447A/DM7447A
DM5448/DM7448
DM54141/DM74141
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DM54187/DM74187
DM74200
DM7573/DM8573
DM7574/DM8574
DM7575/DM8575
DM7576/DM8576
DM8582
DM7595/DM8595
DM7596/DM8596
DM7597/DM8597
DM7598/DM8598
DM7599/DM8599

DM54L89A/DM74L89A
DM54L187A/DM74L187A
DM76L97/DM86L97
DM76L99/DM86L99

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DM5485/DM7485
DM7130/DM8130
DM7131/DM8131
DM7136/DM8136
DM7160/DM8160
DM7200/DM8200

DM54L85/DM74L85

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DM5483/DM7483
DM54181/DM74181
DM54182/DM74182

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DM7875A/DM8875A
DM7875B/DM8875B

PARITY GENERATORS

DM54180/DM74180
DM7220/DM8220

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DM54123/DM74123
DM54L123/DM74L123
DM9601/DM8601
DM9602/DM8602

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DM7800/DM8800
DM7810/DM8810
DM7811/DM8811
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DM7835/DM8835
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LM161
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LM75324
LM75461
LM75462
LM75463
LM75464
MH7803/MH8803
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MH8804
MH8805

CMOS

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MM54C02/MM74C02
MM54C04/MM74C04
MM54C10/MM74C10
MM54C20/MM74C20
MM54C42/MM74C42
DM54C73/MM74C73
MM54C74/MM74C74
MM54C76/MM74C76
MM54C95/MM74C95
MM54C107/MM74C107
MM54C151/MM74C151
MM54C154/MM74C154
MM54C157/MM74C157
MM54C160/MM74C160
MM54C161/MM74C161
MM54C162/MM74C162
MM54C163/MM74C163
MM54C164/MM74C164
MM54C173/MM74C173
MM54C192/MM74C192
MM54C193/MM74C193
MM54C195/MM74C195

Series 54/74

REFERENCE

The following table references all Physical Dimension Drawings, Waveforms, and Test Circuits for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES											WAVE-FORMS		TEST CIRCUITS	
		Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)						
Devices	Pg.	Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Fig.	Pg.
DM5400	1-1	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7400	1-1	3	II	11	IV	J							1	11-5	1	11-1
DM5401	1-3	3	II	11	IV	J	18	V	W				1	11-5	2	11-1
DM7401	1-3	3	II	11	IV	J							1	11-5	2	11-1
DM5402	1-5	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7402	1-5	3	II	11	IV	J							1	11-5	1	11-1
DM5403	1-3	3	II	11	IV	J							1	11-5	2	11-1
DM7403	1-3	3	II	11	IV	J							1	11-5	2	11-1
DM5404	1-7	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7404	1-7	3	II	11	IV	J							1	11-5	1	11-1
DM5405	1-3	3	II	11	IV	J	18	V	W				1	11-5	2	11-1
DM7405	1-3	3	II	11	IV	J							1	11-5	2	11-1
DM5406	1-9	3	II	11	IV	J	18	V	W				2	11-5	4	11-1
DM7406	1-9	3	II	11	IV	J							2	11-5	4	11-1
DM5407	1-11	3	II	11	IV	J	18	V	W				3	11-5	4	11-1
DM7407	1-11	3	II	11	IV	J							3	11-5	4	11-1
DM5408	1-13	3	II	11	IV	J	18	V	W				3	11-5	1	11-1
DM7408	1-13	3	II	11	IV	J							3	11-5	1	11-1
DM5409	1-13	3	II	11	IV	J	18	V	W				3	11-5	2	11-1
DM7409	1-13	3	II	11	IV	J							3	11-5	2	11-1
DM5410	1-1	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7410	1-1	3	II	11	IV	J							1	11-5	1	11-1
DM5411	1-15	3	II	11	IV	J							3	11-5	1	11-1
DM7411	1-15	3	II	11	IV	J							3	11-5	1	11-1
DM5413	1-17	3	II	11	IV	J	18	V	W				42	11-19	1	11-1
DM7413	1-17	3	II	11	IV	J							42	11-19	1	11-1
DM5416	1-9	3	II	11	IV	J	18	V	W				2	11-5	4	11-1
DM7416	1-9	3	II	11	IV	J							2	11-5	4	11-1
DM5417	1-11	3	II	11	IV	J	18	V	W				3	11-5	4	11-1
DM7417	1-11	3	II	11	IV	J							3	11-5	4	11-1
DM5420	1-1	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7420	1-1	3	II	11	IV	J							1	11-5	1	11-1
DM5426	1-19	3	II	11	IV	J							4	11-5	2	11-1
DM7426	1-19	3	II	11	IV	J							4	11-5	2	11-1
DM5430	1-21	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7430	1-21	3	II	11	IV	J							1	11-5	1	11-1
DM5432	1-23	3	II	11	IV	J	18	V	W				3	11-5	1	11-1
DM7432	1-23	3	II	11	IV	J							3	11-5	1	11-1
DM5437	1-25	3	II	11	IV	J	18	V	W				1	11-5	6	11-1
DM7437	1-25	3	II	11	IV	J	18	V	W				1	11-5	6	11-1
DM5438	1-25	3	II	11	IV	J	18	V	W				1	11-5	2	11-1
DM7438	1-25	3	II	11	IV	J	18	V	W				1	11-5	2	11-1
DM5440	1-27	3	II	11	IV	J	18	V	W				1	11-5	6	11-1
DM7440	1-27	3	II	11	IV	J							1	11-5	6	11-1
DM5441A	1-29			12	IV	J	19	V	W							
DM7441A	1-29	5	II	12	IV	J										
DM5442	1-31			12	IV	J	19	V	W				5	11-5	1	11-1
DM7442	1-31	5	II	12	IV	J							5	11-5	1	11-1
DM5445	1-33			12	IV	J	19	V	W				9	11-6	2	11-4
DM7445	1-33	5	II	12	IV	J	19	V	W				9	11-6	2	11-1
DM5450	1-35	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7450	1-35	3	II	11	IV	J							1	11-5	1	11-1
DM5451	1-35	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7451	1-35	3	II	11	IV	J							1	11-5	1	11-1

*Order Numbers. use Device No. suffixed with package letter, i e. DM7800W.

**Also available in D package. See page III.

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
		Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
Devices	Pg.	Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type		Fig.	Pg.	Fig.	Pg.
DM5453	1-35	3	II	11	IV	J	18	V	W					1	11-5	1	11-1
DM7453	1-35	3	II	11	IV	J								1	11-5	1	11-1
DM5454	1-35	3	II	11	IV	J	18	V	W					1	11-5	1	11-1
DM7454	1-35	3	II	11	IV	J								1	11-5	1	11-1
DM5460	1-35	3	II	11	IV	J	18	V	W								
DM7460	1-35	3	II	11	IV	J											
DM5470	1-38	3	II	11	IV	J	18	V	W								
DM7470	1-38	3	II	11	IV	J											
DM5472	1-40	3	II	11	IV	J	18	V	W					6	11-5	1	11-1
DM7472	1-40	3	II	11	IV	J								6	11-5	1	11-1
DM5473	1-42	3	II	11	IV	J	18	V	W					6	11-5	1	11-1
DM7473	1-42	3	II	11	IV	J								6	11-5	1	11-1
DM5474	1-44	3	II	11	IV	J	18	V	W					7	11-6	1	11-1
DM7474	1-44	3	II	11	IV	J								7	11-6	1	11-1
DM5475	1-46	5	II	12	IV	J	19	V	W					8	11-6	1	11-1
DM7475	1-46	5	II	12	IV	J								8	11-6	1	11-1
DM5476	1-42	5	II	12	IV	J	19	V	W					6	11-5	1	11-1
DM7476	1-42	5	II	12	IV	J								6	11-5	1	11-1
DM5483	1-48			12	IV	J	19	V	W								
DM7483	1-48	5	II	12	IV	J											
DM5486	1-51	3	II	11	IV	J	18	V	W					15	11-9	1	11-1
DM7486	1-51	3	II	11	IV	J								15	11-9	1	11-1
DM5488	1-53	5	II	12	IV	J	19	V	W					13	11-8	2	11-1
DM7488	1-53	5	II	12	IV	J	19	V	W					13	11-8	2	11-1
DM5489	1-57			12	IV	J								16	11-9	7	11-1
DM7489	1-57	5	II	12	IV	J								16	11-9	7	11-1
DM5490	1-59	3	II	11	IV	J	18	V	W					18	11-10	1	11-1
DM7490	1-59	3	II	11	IV	J								18	11-10	1	11-1
DM5492	1-59	3	II	11	IV	J	18	V	W					18	11-10	1	11-1
DM7492	1-59	3	II	11	IV	J								18	11-10	1	11-1
DM5493	1-59	3	II	11	IV	J	18	V	W					18	11-10	1	11-1
DM7493	1-59	3	II	11	IV	J								18	11-10	1	11-1
DM5495	1-63	3	II	11	IV	J	18	V	W					14	11-9	1	11-1
DM7495	1-63	3	II	11	IV	J								14	11-9	1	11-1
DM5496	1-66			12	IV	J	19	V	W								
DM7496	1-66	5	II	12	IV	J											
DM54107	1-42	5	II	12	IV	J								6	11-5	1	11-1
DM74107	1-42	5	II	12	IV	J								6	11-5	1	11-1
DM54121	1-68	3	II	11	IV	J	18	V	W							1	11-1
DM74121	1-68	3	II	11	IV	J										1	11-1
DM54145	1-33			12	IV	J	19	V	W					9	11-6	2	11-1
DM74145	1-33	5	II	12	IV	J	19	V	W					9	11-6	2	11-1
DM54150	1-70			13	IV	J	17	V	F								
DM74150	1-70	7	III	13	IV	J											
DM54151	1-73			12	IV	J	19	V	W					9	11-6	1	11-1
DM74151	1-73	5	II	12	IV	J	19	V	W					9	11-6	1	11-1
DM54153	1-75			12	IV	J	19	V	W					3	11-5	1	11-1
DM74153	1-75	5	II	12	IV	J	19	V	W					3	11-5	1	11-1
DM54154	1-77			13	IV	J	17	V	F					19	11-10	1	11-1
DM74154	1-77	7	III	13	IV	J	17	V	F					19	11-10	1	11-1
DM54155	1-80			12	IV	J	19	V	W					9	11-6	1	11-1
DM74155	1-80	5	II	12	IV	J	19	V	W					9	11-6	1	11-1
DM54156	1-80			12	IV	J	19	V	W					9	11-6	2	11-1
DM74156	1-80	5	II	12	IV	J	19	V	W					9	11-6	2	11-1
DM54166	1-82			12	IV	J	19	V	W								
DM74166	1-82	5	II	12	IV	J	19	V	W								
DM54180	1-84			11	IV	J	19	V	W					9	11-6		
DM74180	1-84	3	II	11	IV	J	18	V	W					9	11-6		
DM54181	1-86			13	IV	J								20	11-10	12	11-4
DM74181	1-86	7	III	13	IV	J								20	11-10	12	11-4
DM54182	1-92			12	IV	J								3	11-5	1	11-1
DM74182	1-92	5	II	12	IV	J								3	11-5	1	11-1
DM54184	1-94			12	IV	J	19	V	W					13	11-8	2	11-1
DM74184	1-94	5	II	12	IV	J	19	V	W					13	11-8	2	11-1
DM54185A	1-94			12	IV	J	19	V	W					13	11-8	2	11-1
DM74185A	1-94	5	II	12	IV	J	19	V	W					13	11-8	2	11-1
DM54187	1-96			12	IV	J								13	11-8	7	11-1
DM74187	1-96	5	II	12	IV	J								13	11 8	7	11-1
DM54190	1-99			12	IV	J	19	V	W								
DM74190	1-99	5	II	12	IV	J	19	V	W								

DATA SHEETS		PACKAGES											WAVE-FORMS		TEST CIRCUITS	
		Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)						
Devices	Pg.	Fig.	Pg.	Fig.	Pg.	Type	Fig	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Fig.	Pg.
DM54191	1-101			12	IV	J	19	V	W							
DM74191	1-101	5	II	12	IV	J	19	V	W							
DM54198	1-103			13	IV	J	17	V	F							
DM74198	1-103	7	III	13	IV	J	17	V	F							
DM54199	1-105			13	IV	J	17	V	F							
DM74199	1-105	7	III	13	IV	J	17	V	F							
DM74200	1-146	5	II	9	III	D										
DM7090	1-107	5	II	12	IV	J	19	V	W				1	11-5	1	11-1
DM8090	1-107	5	II	12	IV	J	19	V	W				1	11-5	1	11-1
DM7091	1-109	3	II	11	IV	J	18	V	W				1	11-5	6	11-1
DM8091	1-109	3	II	11	IV	J	18	V	W				1	11-5	6	11-1
DM7092	1-111	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM8092	1-111	3	II	11	IV	J	18	V	W				1	11-5	1	11-1
DM7093	1-113			11	IV	J	18	V	W				10	11-7	3	11-1
DM8093	1-113	3	II	11	IV	J							10	11-7	3	11-1
DM7094	1-113			11	IV	J	18	V	W				10	11-7	3	11-1
DM8094	1-113	3	II	11	IV	J							10	11-7	3	11-1
DM7095	1-116			12	IV	J	19	V	W				21	11-11	3	11-1
DM8095	1-116	5	II	12	IV	J	19	V	W				21	11-11	3	11-1
DM7096	1-116			12	IV	J	19	V	W				21	11-11	3	11-1
DM8096	1-116	5	II	12	IV	J	19	V	W				21	11-11	3	11-1
DM7097	1-116			12	IV	J	19	V	W				21	11-11	3	11-1
DM8097	1-116	5	II	12	IV	J	19	V	W				21	11-11	3	11-1
DM7098	1-116			12	IV	J	19	V	W				21	11-11	3	11-1
DM8098	1-116	5	II	12	IV	J	19	V	W				21	11-11	3	11-1
DM7121	1-118			12	IV	J	19	V	W				12	11-8	3	11-1
DM8121	1-118	5	II	12	IV	J	19	V	W				12	11-8	3	11-1
DM7123	1-120			12	IV	J	19	V	W				12	11-8	3	11-1
DM8123	1-120	5	II	12	IV	J	16	V	F				12	11-8	3	11-1
DM7130	1-122			10	III	D	17	V	F				11	11-8	2	11-1
DM8130	1-122	7	III	10	III	D	17	V	F				11	11-8	2	11-1
DM7131	1-124	5	II	12	IV	J	19	V	W							
DM8131	1-124	5	II	12	IV	J										
DM7136	1-124			12	IV	J	19	V	W							
DM8136	1-124	5	II													
DM7160	1-122			9	III	D	19	V	W				11	11-8	2	11-1
DM8160	1-122	5	II	12	IV	J	19	V	W				11	11-8	2	11-1
DM7200	1-126	3	II	11	IV	J	18	V	W				22	11-12	1	11-1
DM8200	1-126	3	II	11	IV	J							22	11-12	1	11-1
DM7210	1-128			11	IV	J	18	V	W				23	11-12	1	11-1
DM8210	1-128	3	II	11	IV	J							23	11-12	1	11-1
DM7211	1-128			12	IV	J	19	V	W				23	11-12	1	11-1
DM8211	1-128	5	II	12	IV	J							23	11-12	1	11-1
DM7214	1-131			12	IV	J	19	V	W				12	11-8	3	11-1
DM8214	1-131	5	II	12	IV	J	19	V	W				12	11-8	3	11-1
DM7219	1-133			10	III	D	17	V	F				12-A	11-8	15	11-4
DM8219	1-133	7	III	10	III	D	17	V	F				12-A	11-8	15	11-4
DM7220	1-136	3	II	11	IV	J	18	V	W				9	11-6	1	11-1
DM8220	1-136	3	II	11	IV	J							9	11-6	1	11-1
DM7223	1-138			12	IV	J							5	11-5	1	11-1
DM8223	1-138	5	II	12	IV	J							5	11-5	1	11-1
DM7230	1-140			12	IV	J	19	V	W				12	11-8	3	11-1
DM8230	1-140	5	II	12	IV	J							12	11-8	3	11-1
DM7280	1-143			11	IV	J	18	V	W				18	11-10	1	11-1
DM8280	1-143	3	II	11	IV	J	18	V	W				18	11-10	1	11-1
DM7281	1-143			11	IV	J	18	V	W				18	11-10	1	11-1
DM8281	1-143	3	II	11	IV	J	18	V	W				18	11-10	1	11-1
DM7288	1-143			11	IV	J	18	V	W				18	11-10	1	11-1
DM8288	1-143	3	II	11	IV	J	18	V	W				18	11-10	1	11-1
DM7520	1-148			12	IV	J	19	V	W				24	11-12	1	11-1
DM8520	1-148	5	II	12	IV	J							24	11-12	1	11-1
DM7551	1-152			12	IV	J	19	V	W				25	11-12	3	11-1
DM8551	1-152	5	II	12	IV	J							25	11-12	3	11-1
DM7552	1-155			12	IV	J	19	V	W				26	11-13	11	11-3
DM8552	1-155	5	II	12	IV	J	19	V	W				26	11-13	11	11-3
DM7553	1-159			12	IV	J	19	V	W				27	11-14	13	11-4
DM8553	1-159	5	II	12	IV	J	19	V	W				27	11-14	13	11-4
DM7554	1-155			12	IV	J	19	V	W				26	11-13	11	11-3
DM8554	1-155	5	II	12	IV	J	19	V	W				26	11-13	11	11-3
DM7560	1-161			12	IV	J	19	V	W				28	11-15	1	11-1

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
		Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
Devices	Pg.	Fig.	Pg.	Fig.	Pg.	Type	Fig	Pg	Type	Fig.	Pg.	Type		Fig.	Pg.	Fig.	Pg.
DM8560	1-161	5	II	12	IV	J								28	11-15	1	11-1
DM7563	1-164			12	IV	J	19	V	W					28	11-15	1	11-1
DM8563	1-164	5	II	12	IV	J								28	11-15	1	11-1
DM7570	1-167			11	IV	J	18	V	W					29	11-15	5	11-1
DM8570	1-167	3	II	11	IV	J								29	11-15	5	11-1
DM7573	1-169			9	III	D								31	11-16	7	11-1
DM8573	1-169			9	III	D								31	11-16	7	11-1
DM7574	1-172			9	III	D											
DM8574	1-172			9	III	D											
DM7575	1-175			10	III	D											
DM8575	1-175	7	III	10	III	D											
DM7576	1-175			10	III	D											
DM8576	1-175	7	III	10	III	D											
DM8582	1-146	5	II	9	III	D								33	11-16	2	11-1
DM7590	1-180			12	IV	J	19	V	W					30	11-15	1	11-1
DM8590	1-180	5	II	12	IV	J								30	11-15	1	11-1
DM7595	1-182			10	III	D											
DM8595	1-182	7	III	10	III	D											
DM7596	1-184			10	III	D											
DM8596	1-184	7	III	10	III	D											
DM7597	1-187			9	III	D								32	11-16	3	11-1
DM8597	1-187	5	II	12	IV	J								32	11-16	3	11-1
DM7598	1-190			12	IV	J								32	11-16	3	11-1
DM8598	1-190	5	II	12	IV	J								32	11-16	3	11-1
DM7599	1-195			12	IV	J								17	11-9	3	11-1
DM8599	1-195	5	II	12	IV	J								17	11-9	3	11-1
DM7695	1-182			10	III	D											
DM8695	1-182	7	III	10	III	D											
DM7696	1-184			10	III	D											
DM8696	1-184	7	III	10	III	D											
DM7800	1-197									21	V	H		34	11-17		
DM8800	1-197									21	V	H		34	11-17		
DM7806	1-200			11	IV	J	18	V	W								
DM8806	1-200	3	II	11	IV	J	18	V	W								
DM7810	1-202	3	II	11	IV	J								4	11-5	2	11-1
DM8810	1-202	3	II	11	IV	J								4	11-5	2	11-1
DM7811	1-202	3	II	11	IV	J	18	V	W					4	11-5	2	11-1
DM8811	1-202	3	II	11	IV	J	18	V	W					4	11-5	2	11-1
DM7812	1-202	3	II	11	IV	J	18	V	W					4	11-5	2	11-1
DM8812	1-202	3	II	11	IV	J	18	V	W					4	11-5	2	11-1
DM7819	1-204	3	II	11	IV	J	18	V	W					35	11-17	2	11-1
DM8819	1-204	3	II	11	IV	J	18	V	W					35	11-17	2	11-1
DM7820	1-206			11	IV	J**	18	V	W								
DM8820	1-206	3	II	11	IV	J	18	V	W								
DM7820A	1-208			11	IV	J**	18	V	W								
DM8820A	1-208	3	II	11	IV	J	18	V	W								
DM7822	1-210			11	IV	J**											
DM8822	1-210	3	II														
DM7830	1-212			11	IV	J**	18	V	W								
DM8830	1-212	3	II	11	IV	J	18	V	W								
DM7831	1-214			12	IV	J**	19	V	W								
DM8831	1-214	5	II	12	IV	J	19	V	W								
DM7832	1-214			12	IV	J**	19	V	W								
DM8832	1-214	5	II	12	IV	J**	19	V	W								
DM7836	1-217			11	IV	J											
DM8836	1-217	3	II	11	IV	J											
DM7837	1-219			12	IV	J	19	V	W								
DM8837	1-219	5	II	12	IV	J	19	V	W								
DM7838	1-221			12	IV	J	19	V	W								
DM8838	1-221	5	II	12	IV	J											
DM7875A	1-223			9	III	D								12	11-8	3	11-1
DM8875A	1-223	5	II	12	IV	J								12	11-8	3	11-1
DM7875B	1-223			9	III	D								12	11-8	3	11-1
DM8875B	1-223	5	II	12	IV	J								12	11-8	3	11-1
DM7880	1-225			12	IV	J											
DM8880	1-225	5	II	12	IV	J											
DM8884A	1-228	5	II														
DM8885	1-230	5	II	12	IV	J											

Series 54/74

DM5400/DM7400(SN5400/SN7400) quadruple 2-input NAND gate
DM5410/DM7410(SN5410/SN7410) triple 3-input NAND gate
DM5420/DM7420(SN5420/SN7420) dual 4-input NAND gate

general description

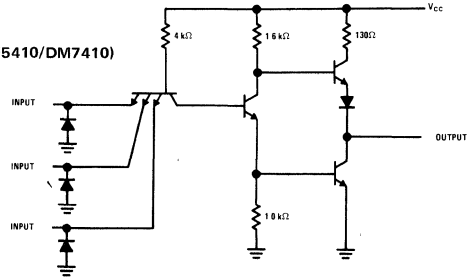
Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The gates are compatible with and interchangeable with Series 54/74 equivalent.

features

- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

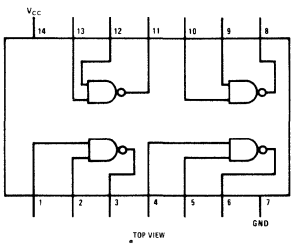
schematic and connection diagrams

(shown for DM5410/DM7410)



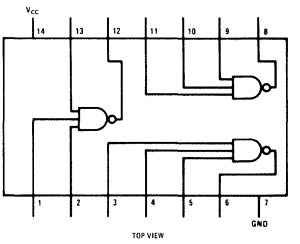
DM5400/DM7400

Dual-In-Line Package



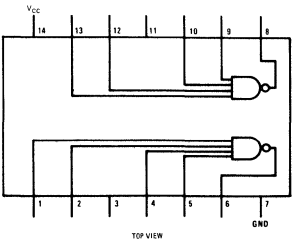
DM5410/DM7410

Dual-In-Line Package



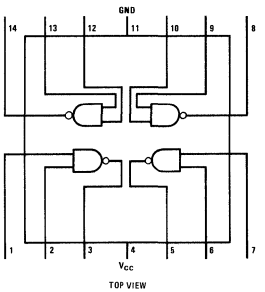
DM5420/DM7420

Dual-In-Line Package



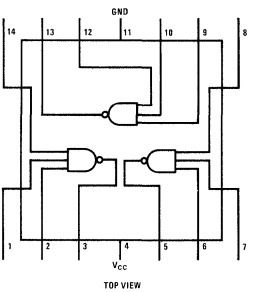
DM5400

Flat Package



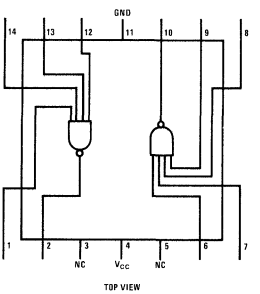
DM5410

Flat Package



DM5420

Flat Package



absolute maximum ratings

V_{CC}	7.0V
Input Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54XX	4 95	5.25	V
DM74XX	4.75	5 25	V
Temperature (T_A)			
DM54XX	−55	+125	°C
DM74XX	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min V_{IN} = 0 8V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = Max V_{IN} = 0V, V_0 = 0V DM74XX / DM54XX	−20 / −18		−55	mA
Supply Current— Logical "0" (Note 3)	V_{CC} = Max V_{IN} = 5.0V		3	5.1	mA
Supply Current— Logical "1" (Note 3)	V_{CC} = Max V_{IN} = 0V		1	1.8	mA
Propagation Delay Time to Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		8	15	ns
Propagation Delay Time to Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		13	25	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54XX and across the 0°C to 70°C range for the DM74XX All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 2: Not more than 1 output should be shorted at a time

Note 3: Each gate.

Series 54/74

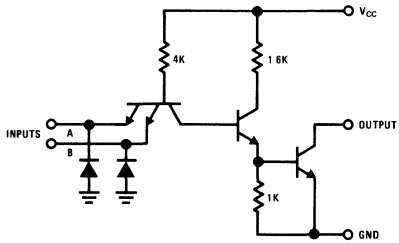
DM5401/DM7401 (SN5401/SN7401) quad 2-input gate (open collector)
DM5403/DM7403(SN5403/SN7403) quad 2-input gate (open collector)
DM5405/DM7405(SN5405/SN7405) hex inverter (open collector)

general description

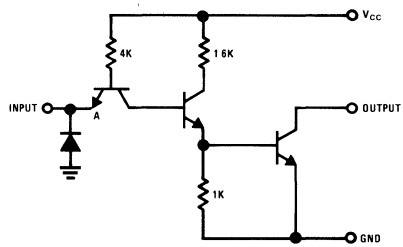
These Series 54/74 functions are designed for applications where the normal TTL "totem-pole" output configuration is not wanted Such applications include implementation of the Wire-OR function

Aside from the output, the circuitry is identical to the standard quad two-input gate (DM5400/DM7400) and hex inverter (DM5404/DM7404).

schematic and connection diagrams

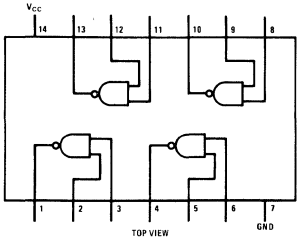


DM5401/DM7401, DM5403/DM7403

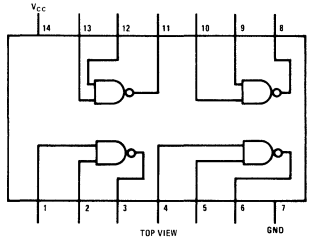


DM5405/DM7405

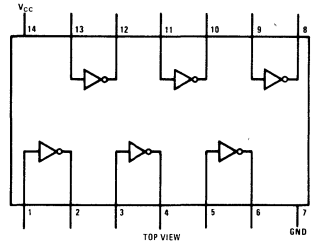
DM5401/DM7401
Dual-In-Line Package



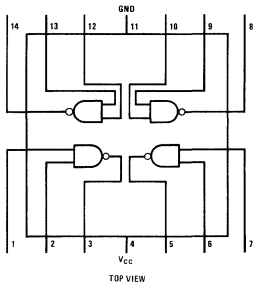
DM5403/DM7403
Dual-In-Line Package



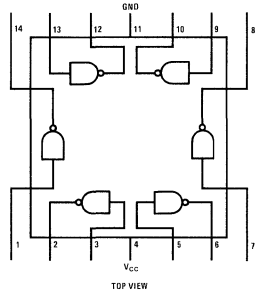
DM5405/DM7405
Dual-In-Line Package



DM5401
Flat Package



DM5405
Flat Package



absolute maximum ratings

V_{CC}		7V
Input Voltage		5.5V
Operating Temperature Range	DM5401, DM5403, DM5405	−55°C to +125°C
	DM7401, DM7403, DM7405	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C I_{IN} = −12 mA			−1 5	V
Logical "1" Input Voltage	DM5401,3,5 / DM7401,3,5	V_{CC} = 4 5V / V_{CC} = 4 75V	2 0			V
Logical "0" Input Voltage	DM5401,3,5 / DM7401,3,5	V_{CC} = 4 5V / V_{CC} = 4 75V			0 8	V
Logical "1" Output Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5 25V, V_{IN} = 0 8V, V_{OUT} = 5 5V			250	μA
		V_{IN} = 0 0V, V_{OUT} = 5 5V			40	μA
Logical "0" Output Voltage	DM5401,3,5 / DM7401,3,5	V_{CC} = 4 5V / V_{CC} = 4 75V, V_{IN} = 2 0V I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 2 4V			40	μA
Logical "1" Input Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0 4V			−1 6	mA
Supply Current—Logical "0" (Each Gate)	DM5401,3,5 / DM7401,3,5	V_{CC} = 5 5V / V_{CC} = 5.25V, V_{IN} = 5 0V		3 0	5 1	mA
Supply Current—Logical "1" (Each Gate)	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 390Ω (Note 2)	3	7 5	15	ns
Propagation Delay Time to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 3.9 kΩ (Note 2)	18	28	45	ns

Note 1: Min/Max units apply across the guaranteed temperature range unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: C_{OUT} includes device output capacitance of approximately 8 5 pF and wiring capacitance

Series 54/74

DM5402/DM7402 (SN5402/SN7402) quad 2-input NOR gate

general description

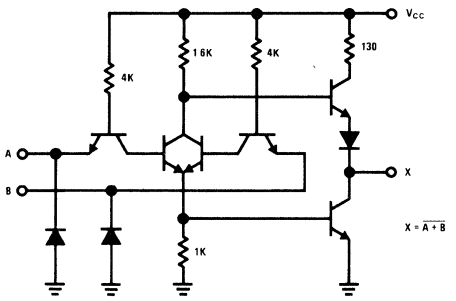
The DM5402/DM7402 is a quad 2-input NOR gate utilizing TTL (Transistor-Transistor Logic) to achieve high speed at nominal power dissipation. It is completely compatible with other Series 54/74 devices.

features

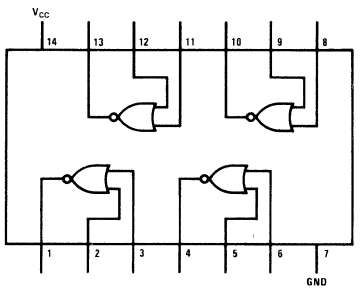
- Input Clamping Diodes
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation
  - DM5402 4.5V to 5.5V
  - DM7402 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 14 mW per gate

schematic and connection diagrams

DM5402/DM7402 (each gate)

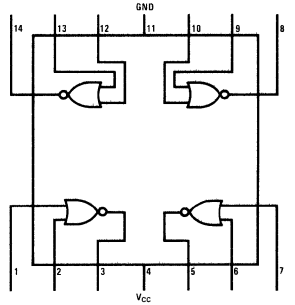


DM5402/DM7402
Dual-In-Line Package



TOP VIEW

DM5402
Flat Package



TOP VIEW

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7402	0°C to 70°C
DM5402	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V T_A = 25°C I_{IN} = −12 mA		−1.0	−1.5	V
Logical "1" Input Voltage	DM5402 DM7402	V_{CC} = 4.5V V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5402 DM7402	V_{CC} = 4.5V V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM5402 DM7402	V_{CC} = 4.5V V_{CC} = 4.75V V_{IN} = 0.8V, I_{OUT} = −400μA	2.4			V
Logical "0" Output Voltage	DM5402 DM7402	V_{CC} = 4.5V V_{CC} = 4.75V V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	DM5402 DM7402	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 2.4V			40	μA
Logical "1" Input Current	DM5402 DM7402	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5402 DM7402	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 0.4V		−1.0	−1.6	mA
Output Short Circuit Current (Note 2)	DM5402 DM7402	V_{CC} = 5.5V V_{CC} = 5.25V V_{OUT} = 0	−20 −18	−32	−55	mA
Supply Current-Logical "0" (each gate)	DM5402 DM7402	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 5.0V		3.6	6.3	mA
Supply Current-Logical "1" (each gate)	DM5402 DM7402	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 0V		2.0	3.6	mA
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF	3	9	15	ns
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF	5	13	22	ns

Note 1: Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7402 and −55°C to +125°C for the DM5402 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Only one output at a time should be short circuited.

Series 54/74

DM5404/DM7404(SN5404/SN7404) hex inverter

general description

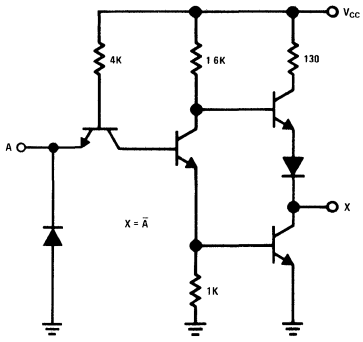
The DM5404/DM7404 is a hex inverter utilizing TTL to achieve high speed at nominal power dissipation. It is totally compatible with other Series 54/74 devices.

features

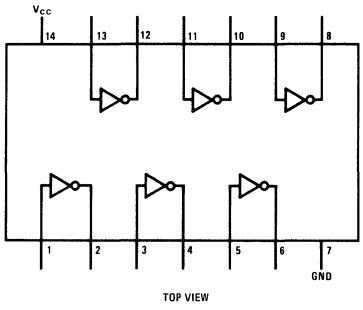
- Input clamping diodes
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation
  - DM5404 4.5V to 5.5V
  - DM7404 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams

DM5404/DM7404

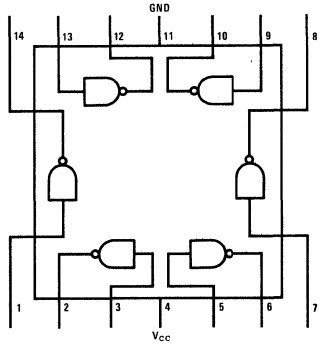


DM5404/DM7404
Dual-In-Line Package



TOP VIEW

DM5404
Flat Package



TOP VIEW

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7404	0°C to 70°C
DM5404	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input diode clamp voltage		V_{CC} = 5.0V, I_{IN} = −12 mA	T_A = 25°C			−1.5	V
Logical "1" Input Voltage	DM5404	V_{CC} = 4.5V		2.0			V
	DM7404	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5404	V_{CC} = 4.5V				0.8	V
	DM7404	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5404	V_{CC} = 4.5V	V_{IN} = 0.8V, I_{OUT} = −400 μA	2.4			V
	DM7404	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5404	V_{CC} = 4.5V	V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
	DM7404	V_{CC} = 4.75V					
Logical "1" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7404	V_{CC} = 5.25V					
Logical "1" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7404	V_{CC} = 5.25V					
Logical "0" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM7404	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM5404	V_{CC} = 5.5V	V_{OUT} = 0	−20	−30	−55	mA
	DM7404	V_{CC} = 5.25V		−18			
Supply Current - Logical "0" (each gate)	DM5404	V_{CC} = 5.5V	V_{IN} = 5.0V		3.0	5.1	mA
	DM7404	V_{CC} = 5.25V					
Supply Current - Logical "1" (each gate)	DM5404	V_{CC} = 5.5V	V_{IN} = 0		1.0	1.8	mA
	DM7404	V_{CC} = 5.25V					
Propagation Delay to a Logical "1", t_{pd1}		T_A = 25°C, N = 10	V_{CC} = 5.0V, C = 50 pF	5	16	22	ns
Propagation Delay to a Logical "0" t_{pd0}		T_A = 25°C, N = 10	V_{CC} = 5.0V, C = 50 pF	3	9	15	ns

Note 1. Min/Max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7404, and −55°C to +125°C for the DM5404, unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2. Only one output at a time should be short circuited.

Series 54/74

DM5406/DM7406,DM5416/DM7416 (SN5406/SN7406,SN5416/SN7416) hex inverter buffers/drivers

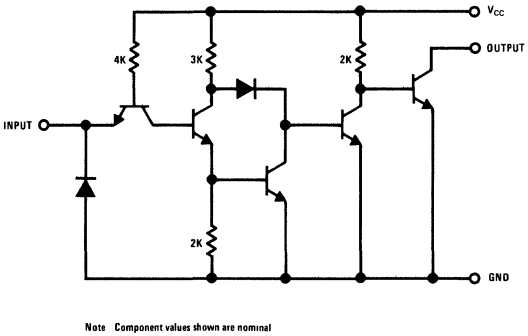
general description

These TTL hex inverter buffers/drivers are fully compatible for use with TTL and DTL logic circuits. Each inverter features high-voltage, open-collector outputs (DM5406/DM7406 30 volts minimum breakdown and DM5416/DM7416 15 volts minimum breakdown). These inverters also feature high sink current capability. (DM5406, DM5416 30 mA and DM7406, DM7416 40 mA).

features

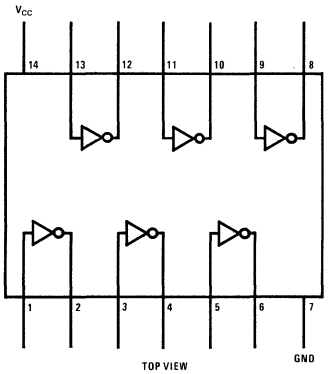
- Input clamp diodes
- High voltage open-collector outputs
  - DM5406/DM7406 30V
  - DM5416/DM7416 15V
- High sink current capability
  - DM5406, DM5416 30 mA
  - DM7406, DM7416 40 mA
- 15 ns typical propagation delay time

schematic and connection diagrams



Note Component values shown are nominal

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage		7.0V
Input Voltage		5 5V
Output Voltage	DM5406/DM7406	30V
	DM5416/DM7416	15V
Storage Temperature Range		−65°C to +150°C
Lead Temperature, (Soldering, 10 Sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM5406,DM5416	4.5	5.5	V
DM7406,DM7416	4.75	5.25	V
Temperature (T_A)			
DM5406,DM5416	−55	+125	°C
DM7406,DM7416	0	70	°C
Output Sink Current			
DM5406,DM5416		30	mA
DM7406,DM7416		40	mA

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2			V
Logical "0" Input Voltage				0 8	V
Output Breakdown Voltage					
DM5406/DM7406	V_{CC} = Max, I_{OFF} = 250 μA, V_{IN} = 0.8V	30			V
DM5416/DM7416	V_{CC} = Max, I_{OFF} = 250 μA, V_{IN} = 0 8V	15			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = Max			0 7	V
	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Supply Current — Logical "1"	V_{CC} = Max, V_{IN} = 0V		30	42	mA
Logical "0"	V_{CC} = Max, V_{IN} = 5V		27	38	mA
Input Clamp Voltage	V_{CC} = 5 0V, I_{IN} = −12 mA, T_A = 25°C			−1 5	V
Propagation Delay to a Logical "0", t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		15	23	ns
Propagation Delay to a Logical "1", t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		10	15	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the operation of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5406, DM5416 and across the 0°C to 70°C range for the DM7406,DM7416. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Series 54/74

DM5407/DM7407,DM5417/DM7417 (SN5407/SN7407,SN5417/SN7417) hex buffers/drivers

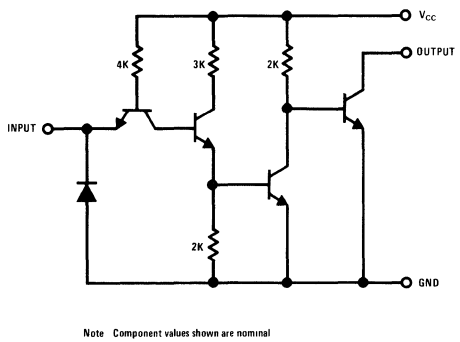
general description

These TTL hex buffers/drivers are fully compatible for use with TTL and DTL logic circuits. Each buffer features high-voltage, open-collector outputs (DM5407/DM7407 30V minimum breakdown and DM5417/DM7417 15V minimum breakdown). These buffers also feature high sink current capability (DM5407, DM5417 30 mA and DM7407, DM7417 40 mA).

features

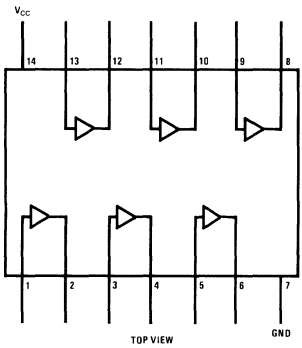
- Input clamp diodes
- High voltage open-collector outputs
  - DM5407/DM7407 30V
  - DM5417/DM7417 15V
- High sink current capability
  - DM5407,DM5417 30 mA
  - DM7407,DM7417 40 mA
- 14 ns typical propagation delay time
- 145 mW typical power dissipation

schematic and connection diagrams



Note Component values shown are nominal

Dual-In-Line and Flat Package



absolute maximum ratings (Note 1)

Supply Voltage		7.0V
Input Voltage		5.5V
Output Voltage	DM5407/DM7407	30V
	DM5417/DM7417	15V
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5407,DM5417	4.5	5 5	V
DM7407,DM7417	4 75	5.25	V
Temperature (T_A)			
DM5407,DM5417	−55	+125	°C
DM7407,DM7417	0	70	°C
Output Sink Current			
DM5407,DM5417		30	mA
DM7407,DM7417		40	mA

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2			V
Logical "0" Input Voltage				0 8	V
Output Breakdown Voltage					
DM5407/DM7407	V_{CC} = Max, I_{OFF} = 250μA, V_{IN} = 2 0V	30			V
DM5417/DM7417	V_{CC} = Max, I_{OFF} = 250μA, V_{IN} = 2 0V	15			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = Max			0 7	V
	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max V_{IN} = 2 4V			40	μA
	V_{CC} = Max V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max V_{IN} = 0 4V			−1 6	mA
Supply Current — Logical "1"	V_{CC} = Max V_{IN} = 5 0V		29	41	mA
Logical "0"	V_{CC} = Max V_{IN} = 0V		21	30	mA
Input Clamp Voltage	V_{CC} = 5 0V I_{IN} = −12 mA, T_A = 25°C			−1 5	V
Propagation Delay to a Logical "0", t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		20	30	ns
Propagation Delay to a Logical "1", t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		6	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the operation of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5407, DM5417 and across the 0°C to 70°C range for the DM7407, DM7417. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Series 54/74

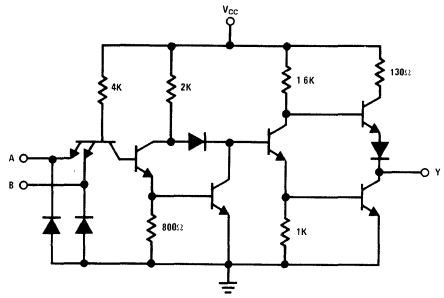
DM5408/DM7408(SN5408/SN7408) quad 2-input AND gate
DM5409/DM7409(SN5409/SN7409) quad 2-input AND gate (open collector)

general description

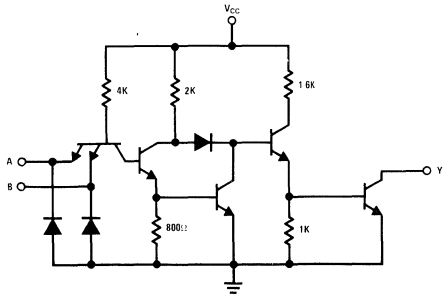
The DM5408/DM7408 and DM5409/DM7409 provide the non-inverting AND function in the popular quad 2-input pin configuration.

schematic and connection diagrams

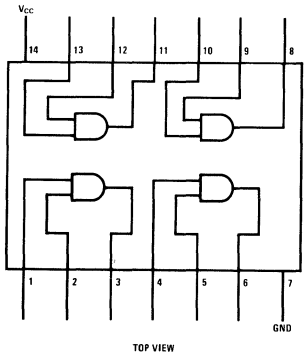
DM5408, DM7408



DM5409, DM7409



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage(V_{CC})			
DM5408, DM5409	4.5	5.5	V
DM7408, DM7409	4.75	5.25	V
Temperature (T_A)			
DM5408, DM5409	−55	+125	°C
DM7408, DM7409	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage (DM5408 / DM7408)	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = −800 μA	2.4			V
Logical "1" Output Current (DM5409 / DM7409)	V_{CC} = Min, V_{OUT} = 5.5V, V_{IN} = 2.0V			250	μA
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max (DM5408)	−20		−55	mA
	V_{CC} = Max (DM7408)	−18		−55	mA
Supply Current — Logical "1" (each device)	V_{CC} = Max, V_{IN} = 5V		11	21	mA
Logical "0"	V_{CC} = Max, V_{IN} = 0V		20	33	mA
Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Propagation Delay to a Logical "0" from DM5408/DM7408 Any Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C		14	19	ns
Propagation Delay to a Logical "0" from DM5409/DM7409 Any Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C		15	24	ns
Propagation Delay to a Logical "1" from DM5408/DM7408 Any Input to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		13	27	ns
Propagation Delay to a Logical "1" From DM5409/DM7409 Any Input to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		17	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5408, DM5409 and across the 0°C to 70°C range for the DM7408, DM7409 All typicals are given for V_{CC} = 5 0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

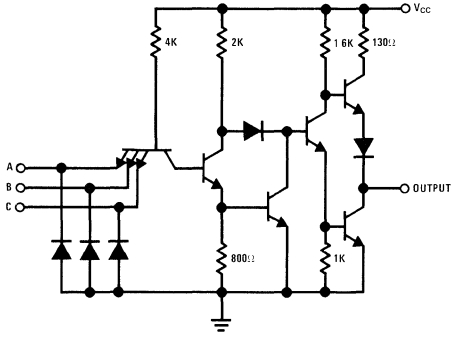
Series 54/74

DM5411/DM7411(SN5411/SN7411)
3-input positive AND gate

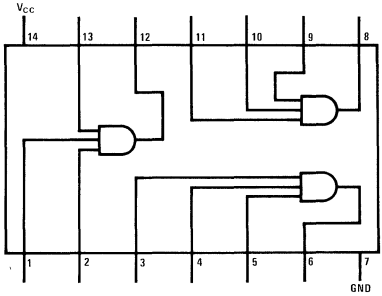
general description

The DM5411/DM7411 provides the AND function for the triple 3-input gate. Its pin-out is the same as the DM5410/DM7410.

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5411	4.5	5.5	V
DM7411	4.75	5.25	V
Temperature (T_A)			
DM5411	−55	+125	°C
DM7411	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = −800 μA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max DM5411	−20		−55	mA
	V_{CC} = Max DM7411	−18		−55	mA
Supply Current — Logical "1" (each device)	V_{CC} = Max, V_{IN} = 5V			15	mA
Logical "0"	V_{CC} = Max, V_{IN} = 0V			22	mA
Input Clamp Voltage	V_{CC} = 5 0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Propagation Delay to a Logical "0" from Any Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF		14	19	ns
Propagation Delay to a Logical "1" from Any Input to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF		13	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5411 and across the 0°C to 70°C range for the DM7411 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM5413/DM7413 (SN5413/SN7413) dual Schmitt-trigger

general description

The DM5413/DM7413 is a dual Schmitt-trigger with input gating. It differs from a conventional dual 4-input gate in that instead of having a single threshold voltage, the DM5413/DM7413 has different thresholds for positive-and negative-going inputs. When the output is in the logical "0" state an input must be lowered to 0.9 volts typically before the output changes state. Conversely in order to return to the logical "0" state the input must rise to 1.7V typically. This hysteresis is extremely beneficial in applications where slow rise and fall time signals are prevalent.

features

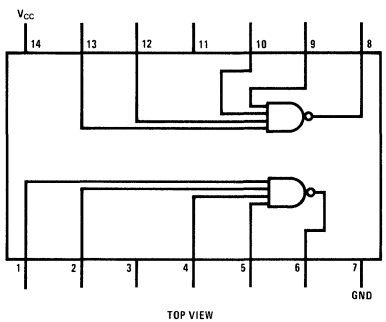
- Series 54/74 compatible
- 800 mV hysteresis typ. – higher noise immunity
- Operation from very slow ramp voltages
- Temperature compensated design
- Typical propagation delay – 17 ns
- Typical power dissipation 42 mW per function

applications

- Pulse shaper
- Threshold detector

logic and connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range		
DM5413	DM5413	−55°C to +125°C
DM7413	DM7413	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{T+} Positive-Going Threshold Voltage		V_{CC} = 5V		1.5	1.7	2.0	V
V_{T-} Negative-Going Threshold Voltage		V_{CC} = 5V		0.6	0.9	1.1	V
$V_{T+} - V_{T-}$ Hysteresis		V_{CC} = 5V		0 4	0 8		V
I_{T+} Input Current at Positive-Going Threshold		V_{CC} = 5V, $V_{IN} = V_{T+}$			−0.65		mA
I_{T-} Input Current at Negative-Going Threshold		V_{CC} = 5V, $V_{IN} = V_{T-}$			−0.85		mA
Logical "1" Output Voltage	DM5413 / DM7413	V_{CC} = 4.5V / V_{CC} = 4 75V	I_{OUT} = −800μA, V_{IN} = 0 6V	2 4			V
Logical "0" Output Voltage	DM5413 / DM7413	V_{CC} = 4 5V / V_{CC} = 4.75V	I_{OUT} = 16 mA, V_{IN} = 2 0V			0 4	V
Logical "1" Input Current	DM5413 / DM7413	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			40	μA
	DM5413 / DM7413	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	DM5413 / DM7413	V_{CC} = 5.5V / V_{CC} = 5 25V	V_{IN} = 0 4V		−1	−1.6	mA
Output Short Circuit Current (Note 3)	DM5413 / DM7413	V_{CC} = 5.5V / V_{CC} = 5.25V		−18		−55	mA
Supply Current − Logical "1" (Each Device)	DM5413 / DM7413	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 0V		14	23	mA
Logical "0"	DM5413 / DM7413	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 4 5V		20	32	mA
Input Clamp Voltage		V_{CC} = 5 0V, I_{IN} = −12 mA, T_A = 25°C				−1 5	V
Propagation Delay to a Logical "0" from any Input to Output, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	50 pF Load	5	15	22	ns
Propagation Delay to a Logical "1" from Any Input to Output, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	50 pF Load	5	18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5413 and across the 0°C to 70°C range for the DM7413 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

Series 54/74

DM5426/DM7426(SN5426/SN7426) quad 2-input TTL-MOS interface gate

general description

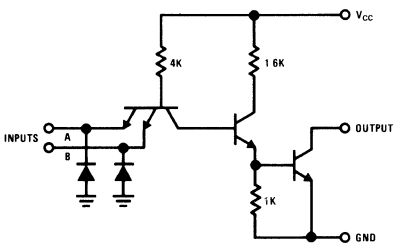
These Series 54/74 compatible gates are high output voltage versions of the DM5403 (SN5403), DM7403 (SN7403). Their open-collector outputs may be "pulled-up" to +15 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 15 volts.

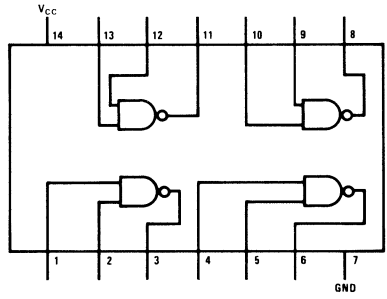
features

- 15V standoff voltage
- Pin compatible with DM5403/DM7403

schematic and connection diagrams

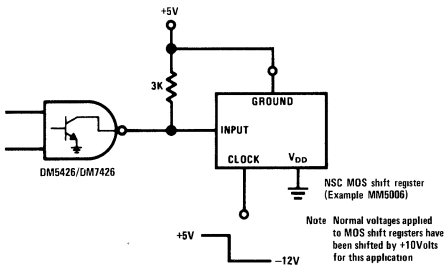


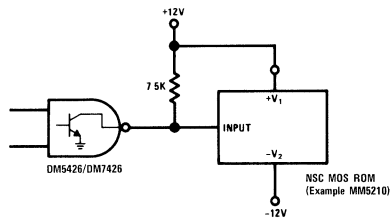
Dual-In-Line Package



TOP VIEW

typical applications





absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Temperature Range	
DM5426	−55°C to 125°C
DM7426	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	$V_{CC} = \frac{4.5V}{4.75V}$	2.0			V
Logical "0" Input Voltage	$V_{CC} = \frac{4.5V}{4.75V}$			0.8	V
Logical "1" Output Current	$V_{CC} = \frac{4.5V}{4.75V}$ V_{IN} = 0.8V V_{OUT} = 12V			50	μA
Logical "1" Output Breakdown Voltage	$V_{CC} = \frac{4.5V}{4.75V}$ V_{IN} = 0V I_{OUT} = 1 mA	15			V
Logical "0" Output Voltage	$V_{CC} = \frac{4.5V}{4.75V}$ V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 2.4V			40	μA
Logical "1" Input Current	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 5.5V			1	mA
Logical "0" Input Current	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "0" (Each Gate)	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 5.0V		3.0	5.1	mA
Supply Current — Logical "1" (Each Gate)	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

Note 1: Min/Max units apply across the guaranteed temperature range −25°C to +125°C for the DM5426 and across the 0°C to +70°C for the DM7426 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Series 54/74

DM5430/DM7430(SN5430/SN7430) 8-input gate

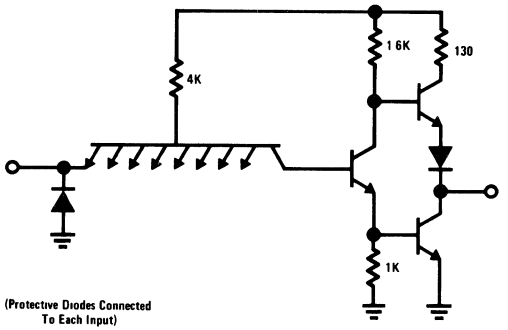
general description

Employing TTL (Transistor-Transistor Logic) to achieve high speed at moderate power dissipation, the DM5430/DM7430 provides the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuit include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature.

features

- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

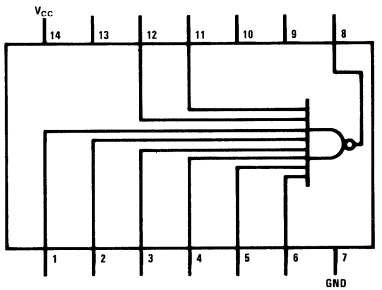
schematic and connection diagrams



(Protective Diodes Connected To Each Input)

DM5430/DM7430

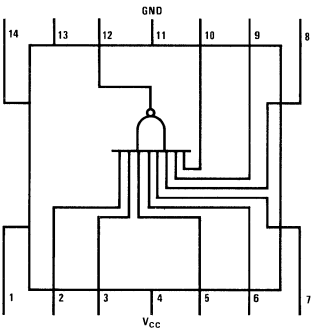
Dual-In-Line Package



TOP VIEW

DM5430

Flat Package



TOP VIEW

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5430	4.75	5.25	V
DM7430	4 75	5.25	V
Temperature (T_A)			
DM5430	−55	+125	°C
DM7430	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current	V_{CC} = Max, V_{IN} = 0V	−18		−55	mA
Supply Current—Logical "0"	V_{CC} = Max, V_{IN} = 5.0V			5.1	mA
Supply Current—Logical "1"	V_{CC} = Max, V_{IN} = 0V			1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			15	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			29	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5430 and across the 0°C to 70°C range for the DM7430. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Series 54/74

DM5432/DM7432(SN5432/SN7432) quad 2-input OR gate

general description

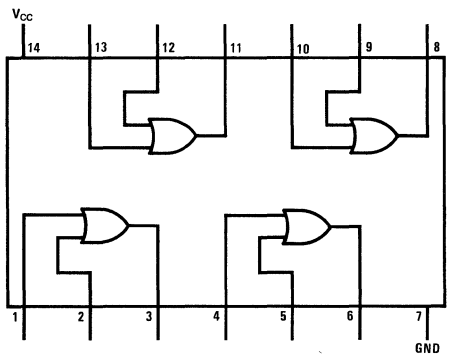
The DM5432/DM7432 (SN5432/SN7432) is a quad 2-input OR gate utilizing TTL (Transistor-Transistor Logic) to provide the basic functions used in the implementation of digital integrated circuit systems. The device is completely compatible with all other Series 54/74 devices.

features

- Popular digital logic block
- Saves inverter function when sign inversion is not needed

logic and connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7032	−55°C to 125°C
DM8032	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5432 DM7432	V_{CC} = 4.5V V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5432 DM7432	V_{CC} = 4.5V V_{CC} = 4.75V			8	V
Logical "1" Output Voltage	DM5432 DM7432	V_{CC} = 4.5V V_{CC} = 4.75V V_{IN} = 2.0V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5432 DM7432	V_{CC} = 4.5V V_{CC} = 4.75V V_{IN} = 8V, I_{OUT} = 16 mA			4	V
Logical "1" Input Current	DM5432 DM7432	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 2.4V			40	μA
	DM5432 DM7432	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5432 DM7432	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 0.4V		−1.0	−1.6	mA
Output Short Circuit Current (Note 3)	DM5432 DM7432	V_{CC} = 5.5V V_{CC} = 5.25V	−20 −18	−32	−55	mA
Supply Current – Logical "1" (Each Device)	DM5432 DM7432	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 5.0V Each Gate			4.4	mA
Logical "0"	DM5432 DM7432	V_{CC} = 5.5V V_{CC} = 5.25V V_{IN} = 0V Each Gate			8.8	mA
Input Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	5	15	22	ns
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	5	12	18	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5432 and across the 0°C to 70°C range for the DM7432. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM5437/DM7437(SN5437/SN7437) quad 2-input NAND buffer
DM5438/DM7438(SN5438/SN7438) quad 2-input NAND buffer (open collector)

general description

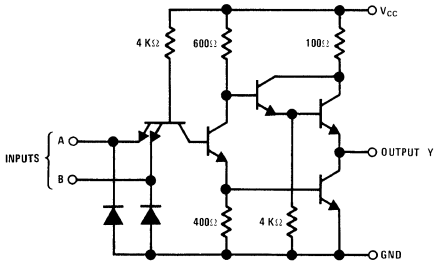
These are quad two-input NAND buffers. The DM5437/DM7437 has a normal TTL "Darlington" output configuration whereas the DM5438/DM7438 has an open-collector. Aside from the output, the circuitry is identical.

features

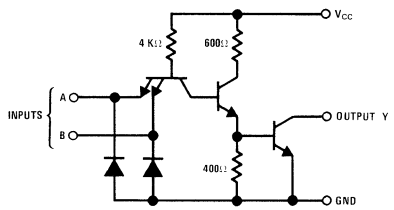
- Series 54/74 TTL and DTL compatible
- Input clamping diodes
- Typical noise immunity 1V
- Fan Out 30

schematic and connection diagrams

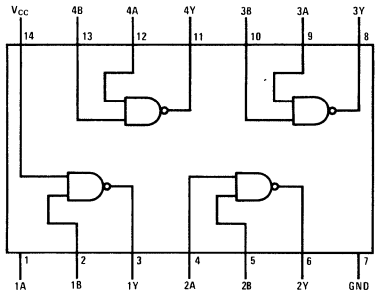
DM5437/DM7437



DM5438/DM7438



Dual-In-Line and Flat Package



TOP VIEW †

POSITIVE LOGIC $Y = \overline{AB}$

†Pin assignments for these circuits are the same for all packages

absolute maximum ratings (Note 1)

V_{CC}	7 0V
Input Voltage	5 5V
Output Voltage	5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM5437,DM5438	4.5	5.5	V
DM7437,DM7438	4 75	5.25	V
Temperature (T_A)			
DM5437, DM5438	−55	+125	°C
DM7437, DM7438	0	70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		V_{CC} = Min	2 0			V
Logical "0" Input Voltage		V_{CC} = Min			0 8	V
Logical "1" Output Voltage	DM5437 / DM7437	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = 4 2 mA	2 4			V
Logical "1" Output Current	DM5438 / DM7438	V_{CC} = Min, V_{IN} = 0 8V, V_{OUT} = 5 5V			250 0	μA
Logical "0" Output Voltage		V_{CC} = Min, V_{IN} = 2 0V, I_{OUT} = 48 mA			0 4	V
Logical "1" Input Current		V_{CC} = Max, V_{IN} = 2 4V V_{IN} = 5 5V			40 0 1 0	μA mA
Logical "0" Input Current		V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Output Short Circuit Current (Note 3)	DM5437 / DM7437	V_{CC} = Max	−20 0		−70 0	mA
Supply Current — Logical "1" (each device)	DM5437,38 / DM7437,38	V_{CC} = Max, All Inputs at 0V		9 5	15 5 8 5	mA mA
Logical "0"	DM5437 38 / DM7437,38	V_{CC} = Max All Inputs at 5V		34	54 0	mA
Input Clamp Voltage		V_{CC} = Min, T_A = 25°C, I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" t_{pd0}	DM5437 / DM7437	V_{CC} = 5 0V, T_A = 25°C		9	15 0	ns
Propagation Delay to a Logical "0" t_{pd0}	DM5438 / DM7438	V_{CC} = 5 0V, T_A = 25°C		11	18 0	ns
Propagation Delay to a Logical "1" t_{pd1}	DM5437 / DM7437	V_{CC} = 5 0V, T_A = 25°C		13	22 0	ns
Propagation Delay to a Logical "1" t_{pd1}	DM5438 / DM7438	V_{CC} = 5 0V, T_A = 25°C		14	22 0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5437, DM5438 and across the 0°C to 70°C range for the DM7437, DM7438 All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54/74

DM5440/DM7440(SN5440/SN7440) dual 4-input buffer

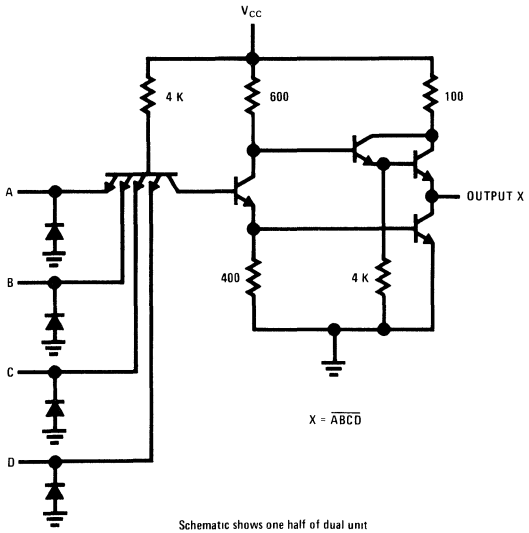
general description

Employing TTL (Transistor-Transistor-Logic) the DM5440/DM7440 buffer is used when the high fan-out is desirable. In addition to driving a large number of TTL inputs, this buffer can be used to drive lines between equipments, to operate small relays and lamps (50 mA), and to act as a clock driver for synchronous logic systems. It is completely compatible with other Series 74 devices.

features

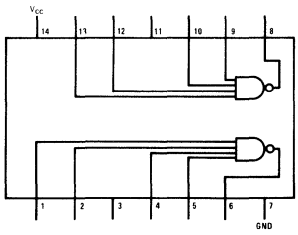
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 30
- Diode Clamps on Inputs

schematic and connection diagrams



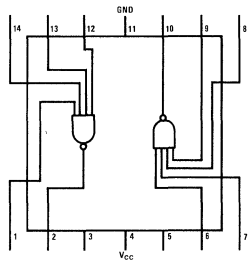
Schematic shows one half of dual unit

DM5440/DM7440
Dual-In-Line Package



TOP VIEW

DM5440
Flat Package



TOP VIEW

absolute maximum ratings

V_{CC}	7.0V
Input Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Fan-Out	30
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5440	4 75	5.25	V
DM7440	4 75	5.25	V
Temperature (T_A)			
DM5440	−55	+125	°C
DM7440	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = −12 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V, I_{OUT} = 48 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = Max, V_{IN} = 0V	−24.0	−55	−70.0	mA
Supply Current — Logical "0" (Note 3)	V_{CC} = Max, V_{IN} = 5.0V, 25°C		8.6	11.4	mA
Supply Current — Logical "1" (Note 3)	V_{CC} = Max, V_{IN} = 0V, 25°C		2.0	3.6	mA
Propagation Delay Time to Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF F.O. = 30		10	15	ns
Propagation Delay Time to Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF F.O. = 30		8	25	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5440 and across the 0°C to 70°C range for the DM7440 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

Note 3: Each gate.

Series 54/74

DM5441A/DM7441A (SN5441A/SN7441A) BCD to decimal decoder/nixie* driver

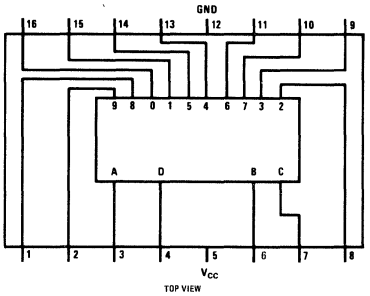
general description

The DM5441A/DM7441A is monolithic binary-coded-decimal to decimal decoder. The BCD number to be decoded is applied to the four input lines; and the unique output corresponding to the decimal equivalent of the input number falls to a logical 0 level. Outputs are designed to drive gas-filled-readout (Nixie*) tubes but are also able to operate with other low current lamps and relays.

An over-range feature provides that if binary numbers between 10 and 15 are applied to the input the least significant bit of these numbers (0 through 5) will be decoded on the output.

connection diagram

Dual-In-Line and Flat Package

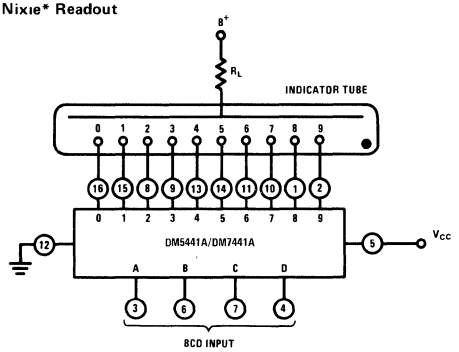


logic table

INPUT D	C	B	A	LOW OUTPUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
(OVER RANGE)				
1	0	1	0	0
1	0	1	1	1
1	1	0	0	2
1	1	0	1	3
1	1	1	0	4
1	1	1	1	5

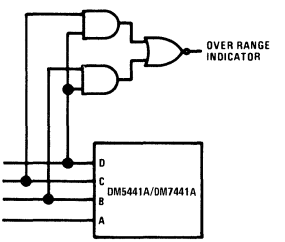
typical applications

Nixie* Readout



Note: Values for B+ and R_L are as specified by the tube manufacturer.

Over-Range Decoding



*Trademark of Burroughs Corporation

absolute maximum ratings

Supply Voltage (V_{CC})		7.0V
Output Voltage		70V
Input Voltage		5.5V
Operating Temperature Range	DM5441A	−55°C to +125°C
	DM7441A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
Logical 1 Input Voltage	DM5441A	V_{CC} = 4.5V			2.0			V
	DM7441A	V_{CC} = 4.75V						
Logical 0 Input Voltage	DM5441A	V_{CC} = 4.5V					0.8	V
	DM7441A	V_{CC} = 4.75V						
Logical 1 Input Current (all inputs)	DM5441A	V_{CC} = 5.5V	V_{IN} = 2.4V			3	40	μA
	DM7441A	V_{CC} = 5.25V						
Logical 1 Input Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 5.5V				1	mA
	DM7441A	V_{CC} = 5.25V						
Logical 0 Input Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.0	−1.6	mA
	DM7441A	V_{CC} = 5.25V						
Supply Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 0.0V			21	36	mA
	DM7441A	V_{CC} = 5.25V						
Logical 1 Output Breakdown	DM5441A	V_{CC} = 5.5V	I_{OUT} = 1.0 mA		70	85		V
	DM7441A	V_{CC} = 5.25V						
Logical 1 Output Current	DM5441A	V_{CC} = 5.5V	V_{OUT} = 50V	125°			60	μA
				70°			40	
	DM7441A	V_{CC} = 5.25V		25°			1.8	
				0°			1.8	
				−55°			1.8	
Logical 0 Output Voltage	DM5441A	V_{CC} = 4.5V	I_{OUT} = 7 mA	125°			3.0	V
				70°			2.5	
	DM7441A	V_{CC} = 4.75V		25°		1.4	2.5	
				0°			2.5	
				−55°			2.5	

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5441A, and the 0°C to +70°C temperature range for the DM7441A.

Note 2: All typicals apply at 25°C for V_{CC} = 5V.

Series 54/74

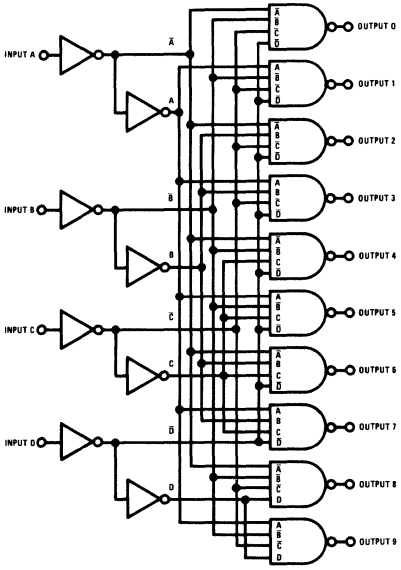
DM5442/DM7442 (SN5442/SN7442) BCD-to-decimal decoder

general description

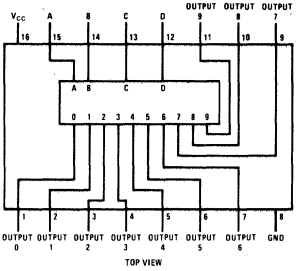
The DM5442/DM7442 utilizes Series 54/74 compatible circuitry to decode a four-bit BCD number to one-of-ten decimal outputs. These ten decimal outputs are capable of driving 10 standard TTL loads each.

The decoding logic is designed such that when binary numbers between 10 and 15 are applied to the inputs, no outputs are enabled.

logic and connection diagrams



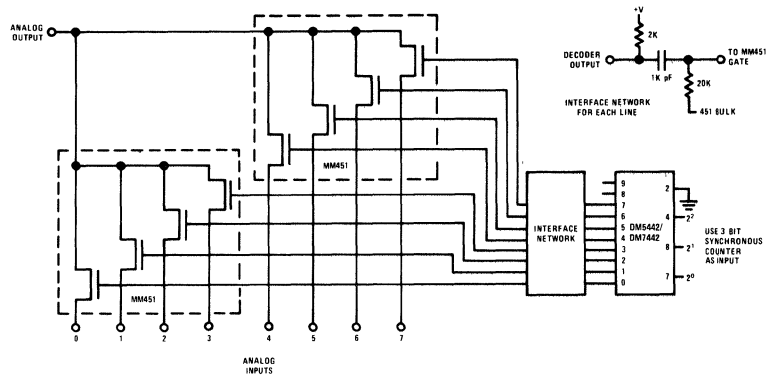
Dual-In-Line and Flat Package



logic table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

typical application



absolute maximum ratings

Supply Voltage	+7V
Input Voltage	+5.5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM5442	−55°C to +125°C
DM7442	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5442	V_{CC} = 4.5V	2.0			V
	DM7442	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM5442	V_{CC} = 4.5V			0.8	V
	DM7442	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM5442	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM7442	V_{CC} = 4.75V, I_{OUT} = −400 μA				
Logical "0" Output Voltage	DM5442	V_{CC} = 4.5V, I_{OUT} = 16 mA			0.4	V
	DM7442	V_{CC} = 4.75V, I_{OUT} = 16 mA				
Logical "1" Input Current	DM5442	V_{CC} = 5.5V, V_{IN} = 2.4			40	μA
	DM7442	V_{CC} = 5.25V, V_{IN} = 2.4				
Logical "1" Input Current	DM5442	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM7442	V_{CC} = 5.25V, V_{IN} = 5.5V				
Logical "0" Input Current	DM5442	V_{CC} = 5.5V, V_{IN} = 0.4V		−1.0	−1.6	mA
	DM7442	V_{CC} = 5.25V, V_{IN} = 0.4V				
Input Clamp Diode (All Inputs)	DM5442	V_{CC} = 5.5V, I_{IN} = −12 mA		−1.0	−1.5	V
	DM7442	V_{CC} = 5.25V, I_{IN} = −12 mA				
Output Short Circuit Current (Note 2)	DM5442	V_{CC} = 5.5V, V_{OUT} = 0V	−20	−32	−55	mA
	DM7442	V_{CC} = 5.25V, V_{OUT} = 0V	−18			
Power Supply Current	DM5442	V_{CC} = 5.5V		28	56	mA
	DM7442	V_{CC} = 5.25V				
Propagation Delay Time to a Logical "0" (2 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	10	23	30	ns
Propagation Delay Time to a Logical "1" (2 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	8	17	25	ns
Propagation Delay Time to a Logical "0" (3 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	12	24	35	ns
Propagation Delay Time to a Logical "1" (3 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	12	26	35	ns

Note 1: Min/max limits apply across the guaranteed operating temperature range −55°C to +125°C for DM5442 and 0°C to 70°C for the DM7442 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2 Only one output may be shorted at a time

Series 54/74

DM5445/DM7445(SN5445/SN7445)
DM54145/DM74145(SN54145/SN74145)
BCD-to-decimal decoder/drivers

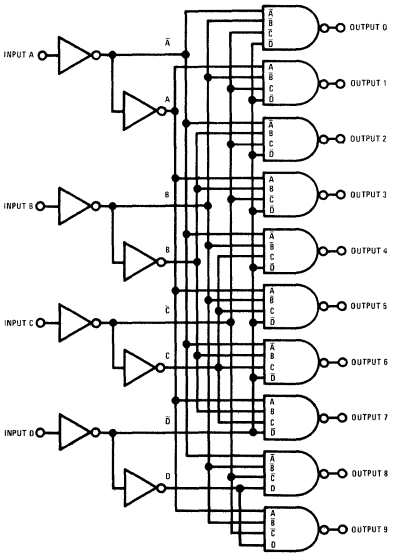
general description

The DM5442/DM7442 and DM54145/DM74145 BCD-to-decimal decoder/drivers are fully compatible for use with TTL or DTL logic circuits. Each circuit features full decoding of all valid BCD input conditions (0 to 9) ensuring that all outputs will be off for any invalid input condition. Each output transistor is capable of sinking 80 mA. In the off condition each transistor can withstand high breakdown voltages (DM5445/DM7445 = 30V and DM54145/DM74145 = 15V).

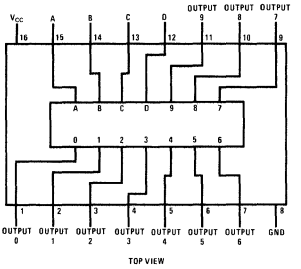
features

- 210 mW typical power dissipation
- 30 ns maximum propagation delay
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line and Flat Package



truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage	DM5445/DM7445	30V
	DM54145/DM74145	15V
Operating Temperature Range		
	DM5445,DM54145	−55°C to +125°C
	DM7445,DM74145	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5445,DM54145	4 5	5.5	V
DM7445,DM74145	4 75	5 25	V

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage		2			V
Logic "0" Input Voltage				0 8	
Output Breakdown Voltage	V_{CC} = Max, I_{OFF} = 250 μA	30			V
	V_{CC} = Max, I_{OFF} = 250 μA	15			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 80 mA		0 5	0 9	V
	V_{CC} = Min, I_{OUT} = 20 mA		0 2	0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Supply Current	V_{CC} = Max		42	62	mA
	V_{CC} = Max		42	70	mA
Input Clamp Voltage	V_{CC} = 5 0, T_A = 25°C, I_{IN} = −12 mA			-1 5	V
Propagation Delay to a Logical "0", t_{pd0}	V_{CC} = 5 0, T_A = 25°C, C_L = 15 pF, R_L = 100Ω		17	30	ns
Propagation Delay to a Logical "1"	V_{CC} = 5 0, T_A = 25°C, C_L = 15 pF, R_L = 100Ω		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5445, DM54145 and across the 0°C to 70°C range for the DM7445,DM74145 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Series 54/74

DM5450/DM7450(SN5450/SN7450) expandable dual 2-wide 2-input AND-OR-INVERT gate
DM5451/DM7451(SN5451/SN7451) dual 2-wide 2-input AND-OR-INVERT gate
DM5453/DM7453(SN5453/SN7453) expandable 4-wide 2-input AND-OR-INVERT gate
DM5454/DM7454(SN5454/SN7454) 4-wide 2-input AND-OR-INVERT gate
DM5460/DM7460(SN5460/SN7460) dual 4-input expander

general description

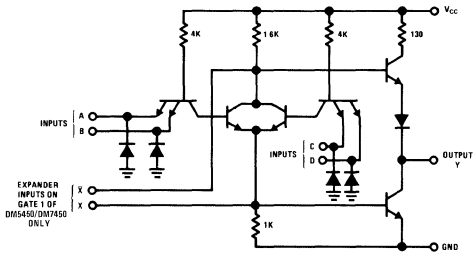
The devices described in this data sheet employ TTL to achieve high speed at moderate power dissipation. They are consolidated onto one sheet since they perform the AND-OR-INVERT function with only differing numbers of AND inputs and OR terms. Characteristics include high noise immunity, low output impedance, good capacitance drive capability, and minimal variation in switching time with temperature. The gates are compatible with and interchangeable with Series 54/74 devices.

features

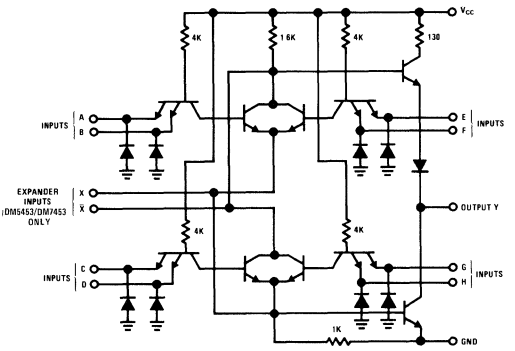
- Input Clamping Diodes
- Typical Noise Immunity 1 Volt
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Average Propagation Delay 13 ns
- Average Power Dissipation 14 mW/ gate

schematic diagrams

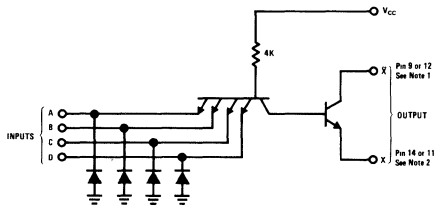
DM5450/DM7450, DM5451/DM7471 (each gate)



DM5453/DM7453, DM5454/DM7454



DM5460/DM7460 (each gate)



NOTES 1 Connect pin 9 or 12 to pin 12 of DM5450/DM7450 or DM5453/DM7453
2 Connect pin 14 or 11 to pin 11 of DM5450/DM7450 or DM5453/DM7453

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54XX	4.75	5.25	V
DM74XX	4 75	5.25	V
Temperature (T_A)			
DM54XX	−55	+125	°C
DM74XX	0	70	°C

electrical characteristics (Notes 1, 3) (DM5450/DM7450, DM5451/DM7451, DM5453/DM7453, DM5454/DM7454)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			− 1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = Max, V_{IN} = 0V	−18		−55	mA
Supply Current — Logical "0" (Each Gate)	V_{CC} = Max, V_{IN} = 5.0V		3.7	6.5	mA
Supply Current — Logical "1" (Each Gate)	V_{CC} = Max, V_{IN} = 0V		2.0	3.6	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			15	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			25	ns
Propagation Delay Time to Logical "0" Level (through DM5450/DM7450 or DM5453/DM7453)	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			20	ns
Propagation Delay Time to Logical "1" Level (through DM5450/DM7450 or DM5453/DM7453)	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			34	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54XX and across the 0°C to 70°C range for the DM74XX. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

Note 3: Measurements made with expandable inputs open

electrical characteristics (Note 1) (DM5460/DM7460)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Diode Clamp Voltage	V_{CC} = 5.0V I_{IN} = −12 mA	T_A = 25°C			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min $R_{V_{CC}\text{ to COLLECTOR}}$ = 1 1 kΩ,	$V_{EMITTER}$ = 1V, T_A = 0°C	2			V
Logical "0" Input Voltage	V_{CC} = Min $R_{EMITTER\text{ to GRD}}$ = 1.2 kΩ, T_A = 0°C	$V_{COLLECTOR}$ = 4 5V, $I_{COLLECTOR}$ = 0.27 mA,			0 8	V
Logical "0" Output Voltage (With Respect to Emitter)	V_{CC} = Min $V_{EMITTER}$ = 1V, T_A = 0°C	V_{IN} = 2V, $R_{V_{CC}\text{ to COLLECTOR}}$ = 1.1 kΩ,			0.4	V
Logical "1" Output Current	V_{CC} = Min $V_{COLLECTOR}$ = 4.5V, T_A = 0°C	V_{IN} = 0 8V, $R_{EMITTER\text{ to GRD}}$ = 1.2 kΩ,			270	μA
Logical "0" Output Current	V_{CC} = Min $V_{EMITTER}$ = 1V	V_{IN} = 2V,	−0.43			mA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0.4V			−1.6	mA
Logical "1" Input Current	V_{CC} = Max V_{CC} = Max	V_{IN} = 2 4V V_{IN} = 5 5V			40 1	μA mA
Logical "0" Supply Current (Each Gate)	V_{CC} = 5.25V, $V_{EMITTER}$ = 0.85V	V_{IN} = 5V,		0.6	1 25	mA
Logical "1" Supply Current (Each Gate)	V_{CC} = 5.25V, $V_{EMITTER}$ = 0.85V	V_{IN} = 0		1.0	1.8	mA

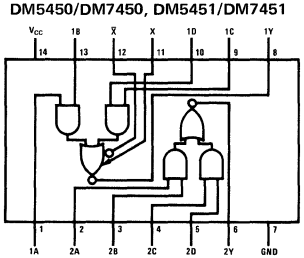
(DM5450/DM7450, DM5453/DM7453 only) using expander inputs, T_A = 0°C for 74XX and T_A = −55°C for 54XX

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Expander Current	V_{CC} = Min I_{SINK} = 16 mA	$V_{PIN\ 11\text{ to PIN }12}$ = 0.4V			3.1	mA
Base-Emitter Voltage of Output Transistor (Q)	V_{CC} = Min $I_{PIN\ 11}$ = 0 62 mA,	I_{SINK} = 16 mA, $R_{PIN\ 11\text{ to PIN }12}$ = 0			1	V
Logical "1" Output Voltage	V_{CC} = Min $I_{PIN\ 11}$ = 0.27 mA,	I_{LOAD} = −400 μA, $I_{PIN\ 12}$ = −0.27 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min $I_{PIN\ 11}$ = 0.43 mA,	I_{SINK} = 16 mA, $R_{PIN\ 11\text{ to }12}$ = 130Ω			0.4	V

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54XX and across the 0°C to 70°C range for the DM74XX All typicals are given for V_{CC} = 5 0V and T_A = 25°C

connection diagrams (Dual-In-Line and Flat Packages)

DM5450/DM7450, DM5451/DM7451



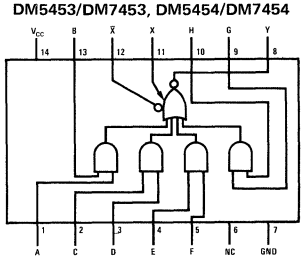
$Y = \overline{(AB) + (CD) + X}$ X = X = ABCD from DM7460

Note 1 Expander nodes X and $\bar{X}$ are on the DM7450 only If not used, leave open

Note 2 Make no external connection to pins 11 and 12 of the DM7451

Note 3 A total of four expander gates may be connected to the DM7450 expandable gate

DM5453/DM7453, DM5454/DM7454



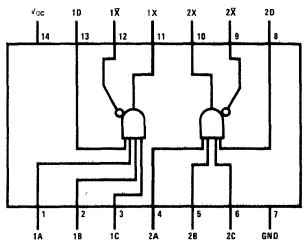
$Y = \overline{(AB) + (CD) + (EF) + (GH) + X}$ X = ABCD from DM7460

Note 1 Expander nodes X and $\bar{X}$ are on the DM7453 only If not used, leave open

Note 2 Make no external connection to pins 11 and 12 of the DM7454

Note 3 A total of four expander gates may be connected to the DM7453 expandable gate

DM5460/DM7460



X = ABCD

Note 1 Connect Pin 9 or 12 to pin 12 of DM7450 or DM7453

Note 2 Connect Pin 10 or 11 to pin 11 of DM7450 or DM7453

Series 54/74

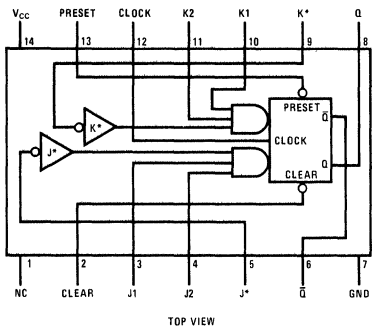
DM5470/DM7470(SN5470/SN7470)
edge-triggered JK flip flop

general description

The DM5470/DM7470 is an edge-triggered J-K flip flop featuring gated inputs, direct clear and preset inputs. Information is transferred to the outputs on the positive-going edge of the clock pulse.

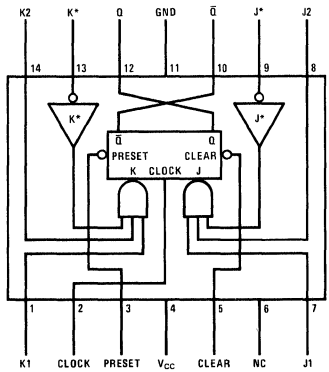
connection diagrams

Dual-In-Line Package



TOP VIEW

Flat Package



TOP VIEW

POSITIVE LOGIC LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET OR CLEAR FUNCTION CAN OCCUR ONLY WHEN CLOCK INPUT IS LOW

truth table

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Note 1 $J = J1 \cdot J2 \cdot \overline{J^*}$
Note 2. $K = K1 \cdot K2 \cdot \overline{K^*}$
Note 3. t_n = Bit time after clock pulse
Note 4 t_{n+1} = Bit time after clock pulse
Note 5 If inputs J* or K* are not used they must be grounded
Note 6. NC - No Internal Connection

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5470	4.5	5.5	V
DM7470	4.75	5.25	V
Temperature (T_A)			
DM5470	−55	+125	°C
DM7470	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0 8	V
Logical "1" Output Voltage	V_{CC} = Min	I_{LOAD} = −400 μA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min,	I_{SINK} = 16 mA			0 4	V
Logical "1" Input Current at J_1, J_2, J*, K_1, K_2, K*, Clock	V_{CC} = Max,	V_{IN} = 2 4V			40	μA
Logical "1" Input Current at Preset or Clear	V_{CC} = Max,	V_{IN} = 2 4V			80	μA
Logical "1" Input Current (Any Input)	V_{CC} = Max,	V_{IN} = 5 5V			1	mA
Logical "0" Input Current at J_1, J_2, J*, K_1, K_2, K*, Clock	V_{CC} = Max,	V_{IN} = 0 4V	−1 6			mA
Logical "0" Input Current at Preset and Clear	V_{CC} = Max,	V_{IN} = 0 4V			−3 2	μA
Output Short Circuit Current (Note 3)	V_{CC} = Max,	V_O = 0V	−20 −18		−57	mA
Supply Current (each device)	V_{CC} = Max,	V_{IN} = 5V			26	mA
Input Clamp Voltage	V_{CC} = Min,	I_{IN} = −12 mA	−1 5			V
Propagation Delay to a Logical "0" from Clear or Preset to Output, t_{pd0}	V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 400Ω			50	ns
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}	V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 400Ω			50	ns
Propagation Delay to a Logical "1" from Clear or Preset to Output, t_{pd1}	V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 400Ω			50	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}	V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 400Ω			50	ns
Maximum Clock Frequency	V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 400Ω	20			MHz
t_{SETUP}, Min Input Setup Time	C_L = 50 pF,	R_L = 400Ω			20	ns
t_{HOLD}, Min Input Hold Time	C_L = 50 pF,	R_L = 400Ω			5	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5470 and across the 0°C to +70°C range for the DM7470. All typicals are given for V_{CC} = 5 0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

Series 54/74

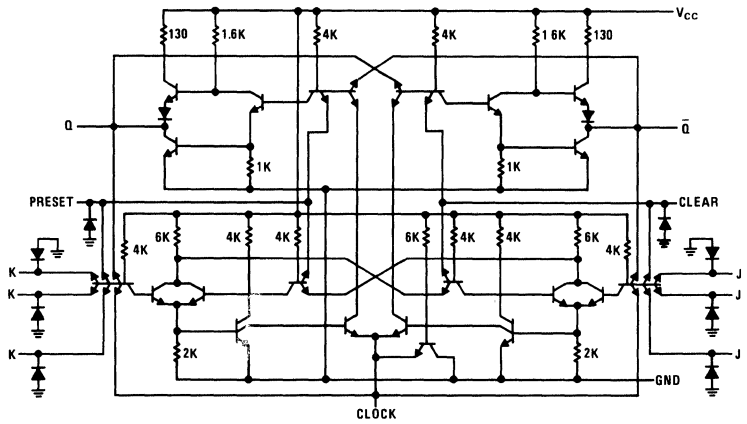
DM5472/DM7472(SN5472/SN7472)
JK master/slave flip flop

general description

The DM5472/DM7472 is a single flip flop with gating used to perform logic on the J and K inputs. Separate PRESET and CLEAR inputs override the clock and permit the flip flop to be directly set to either state. The flip flop is termed Master-Slave since the J and K information is loaded into the Master section when the clock voltage rises, and is transferred to the Slave section and outputs when the clock voltage falls.

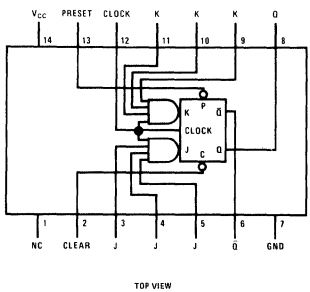
The device also features a special clock line clamp to reduce ringing and prevent false clocking.

schematic and connection diagrams



DM5472/DM7472

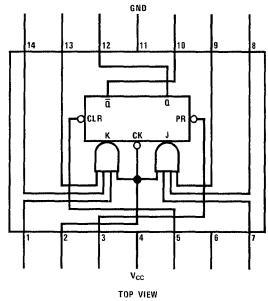
Dual-In-Line Package



TOP VIEW

DM5472

Flat Package



TOP VIEW

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7472	0°C to 70°C
DM5472	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Clock Line Clamp Voltage	DM5472	V_{CC} = 5.5V, I_{CLOCK} = −10 mA			−0.5	V
	DM7472	V_{CC} = 5.25V, I_{CLOCK} = −10 mA			−0.5	V
Logical "1" Input Voltage	DM5472	V_{CC} = 4.5V	2.0			V
	DM7472	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5472	V_{CC} = 4.5V			0.8	V
	DM7472	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM5472	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM7472	V_{CC} = 4.75V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5472	V_{CC} = 4.5V, I_{OUT} = 16 mA			0.4	V
	DM7472	V_{CC} = 4.75V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	DM5472	V_{CC} = 5.5V, V_{IN} = 2.4V				
	DM7472	V_{CC} = 5.25V, V_{IN} = 2.4V				
J or K				10	40	μA
CLEAR or PRESET				20	80	μA
CLOCK				<0	80	μA
Logical "1" Input Current	DM5472	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM7472	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5472	V_{CC} = 5.5V, V_{IN} = 0.4V				
	DM7472	V_{CC} = 5.25V, V_{IN} = 0.4V				
J or K					−1.6	mA
CLEAR, PRESET, or CLOCK					−3.2	mA
Output Short Circuit Current	DM5472	V_{CC} = 5.5V, V_{OUT} = 0	−20		−55	mA
	DM7472	V_{CC} = 5.25V, V_{OUT} = 0	−18		−55	mA
Supply Current	DM5472	V_{CC} = 5.5V		9	17	mA
	DM7472	V_{CC} = 5.25V		9	17	mA
Minimum Allowable Clock Pulse Width		V_{CC} = 5.0V T_A = 25°C			20	ns
Toggle Frequency		V_{CC} = 5.0V T_A = 25°C	15	27		MHz
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF	15	26	45	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF	10	17	30	ns
Propagation Delay Time to a Logical "0" from CLEAR or PRESET		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF			40	ns
Propagation Delay Time to a Logical "1" from CLEAR or PRESET		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF			25	ns
Time after negative-going clock transition that J or K information must be held, t_{hold}		V_{CC} = 5.0V T_A = 25°C			−5	ns
Time prior to negative-going clock transition that J or K information must be set, t_{setup}		V_{CC} = 5.0V T_A = 25°C	Clock pulse width			ns
Clock Voltage Fall Time		V_{CC} = 5.0V T_A = 25°C			150	ns
Clock Skew ($t_{pd\,min} - t_{hold\,max}$)		V_{CC} = 5.0V T_A = 25°C	15			ns

Note 1: Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7472 and −55°C to +125°C for the DM5472 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Series 54/74

DM5473/DM7473(SN5473/SN7473)
DM5476/DM7476(SN5476/SN7476)
DM54107/DM74107(SN54107/SN74107)
dual JK master/slave flip flops

general description

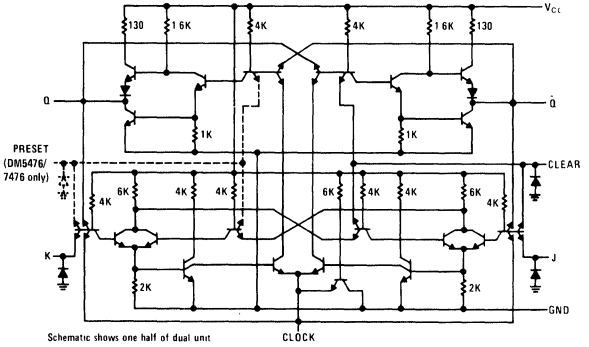
The flip flops described herein are TTL (Transistor-Transistor Logic) dual JK Master/Slave flip flops. Asynchronous CLEAR inputs are provided on the DM5473/DM7473 and DM54107/DM74107 flip flops; and PRESET and CLEAR inputs are available on each of the DM5476/DM7476 flip flops. The latter devices are supplied in a 16 pin package. The devices are totally monolithic and designed for use in high speed control and counting applications, where economy is required, and multiple data inputs are not required. These devices meet all of the electrical and mechanical requirements of the equivalent Series 54/74 devices.

features

- High Speed of Operation — 25 MHz toggling
- Optimum Power Dissipation — 45 mW/ff
- High Noise Immunity — 1V
- Guaranteed Clock Skew — 15 ns

The devices also feature a special clock line clamp to reduce ringing and prevent false clocking. In addition, the usual speed-power efficiency and high output drive-capability normally gained with TTL circuits are retained.

schematic and connection diagrams



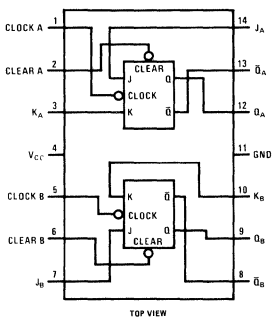
Schematic shows one half of dual unit

truth table

(Each Flip Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

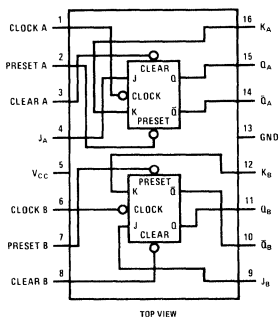
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

Dual-In-Line and Flat Package



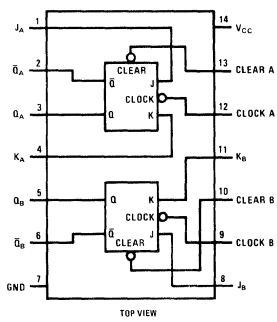
DM5473/DM7473

Dual-In-Line and Flat Package



DM5476/DM7476

Dual-In-Line Package



DM54107/DM74107

absolute maximum ratings

Supply Voltage	+7V
Input Voltage	5.5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM5473, DM5476, DM54107	−55°C to +125°C
DM7473, DM7476, DM74107	0°C to +70°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Clock Line Clamp Voltage	DM5473, DM5476, DM54107	V_{CC} = 5 5V, I_{CLOCK} = −10 mA		−3	−0 5	V
	DM7473, DM7476, DM74107	V_{CC} = 5 25V, I_{CLOCK} = −10 mA		−3	−0 5	V
Input Diode Clamp (J, K, Preset, Clear)		V_{CC} = 5 0V, T_A = 25°C, I_{IN} = −12 mA			−1 5	V
Logical "1" Input Voltage	DM5473, DM5476, DM54107	V_{CC} = 4 5V	2 0			V
	DM7473, DM7476, DM74107	V_{CC} = 4 75V	2 0			V
Logical "0" Input Voltage	DM5473, DM5476, DM54107	V_{CC} = 4 5V			0 80	V
	DM7473, DM7476, DM74107	V_{CC} = 4.75V			0 80	V
Logical "1" Output Voltage	DM5473, DM5476, DM54107	V_{CC} = 4 5V, I_{OUT} = −400 μA	2 4	3 3		V
	DM7473, DM7476, DM74107	V_{CC} = 4 75V, I_{OUT} = −400 μA	2 4	3 3		V
Logical "0" Output Voltage	DM5473, DM5476, DM54107	V_{CC} = 4 5V, I_{OUT} = 16 0 mA		0 20	0 40	V
	DM7473, DM7476, DM74107	V_{CC} = 4 75V, I_{OUT} = 16 0 mA		0 20	0 40	V
Logical "0" Input Current	DM5473, DM5476, DM54107	V_{CC} = 5 5V, V_{IN} = 0 40V, J or K		−1 0	−1 6	mA
		V_{CC} = 5 5V, V_{IN} = 0 40V, Clear, Preset or Clock		−2 0	−3 2	mA
	DM7473, DM7476, DM74107	V_{CC} = 5 25V, V_{IN} = 0 40V, J or K		−1 0	−1 6	mA
		V_{CC} = 5 25V, V_{IN} = 0 40V, Clear, Preset or Clock		−2 0	−3 2	mA
Logical "1" Input Current	DM5473, DM5476, DM54107	V_{CC} = 5 5V, V_{IN} = 2 4V, J or K		10	40	μA
		V_{CC} = 5 5V, V_{IN} = 2 4V, Clear, Preset		20	80	μA
		V_{CC} = 5 5V, V_{IN} = 2 4V, Clock		<0	80	μA
	DM7473, DM7476, DM74107	V_{CC} = 5 25V, V_{IN} = 2 4V, J or K		10	40	μA
		V_{CC} = 5 25V, V_{IN} = 2 4V, Clear, Preset		20	80	μA
		V_{CC} = 5 25V, V_{IN} = 2 4V, Clock		<0	80	μA
Logical "1" Input Current	DM5473, DM5476, DM54107	V_{CC} = 5 5V, V_{IN} = 5 5V			1	mA
	DM7473, DM7476, DM74107	V_{CC} = 5 25V, V_{IN} = 5 5V			1	mA
Output Short Current (Note 2)	DM5473, DM5476, DM54107	V_{CC} = 5 5V, V_{OUT} = 0V	−20		−55	mA
	DM7473, DM7476, DM74107	V_{CC} = 5 25V, V_{OUT} = 0V	−18		−55	mA
Power Supply Current (each flip-flop)	DM5473, DM5476, DM54107	V_{CC} = 5 5V, V_{IN} = 5 0V		9	17	mA
	DM7473, DM7476, DM74107	V_{CC} = 5 25V, V_{IN} = 5 0V		9	17	mA
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5 0V, T_A = 25°C			20	ns
Toggle Frequency		V_{CC} = 5 0V, T_A = 25°C	15	25		MHz
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	15	26	45	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	10	17	30	ns
Propagation Delay Time to a Logical "0" from Clear, or Preset		V_{CC} = 5 0V, T_A = 25°C	12	23	40	ns
Propagation Delay Time to a Logical "1" from Clear, or Preset		V_{CC} = 5 0V, T_A = 25°C	7	14	25	ns
Time after Negative going Clock Transition that J or K information must be held, t_{hold}		V_{CC} = 5 0V, T_A = 25°C			−5	ns
Clock Skew ($t_{pd\ min} - t_{hold\ max}$)		V_{CC} = 5 0V, T_A = 25°C	15			ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5473, DM5476, DM54107 and 0°C to 70°C for the DM7473, DM7476, DM74107 unless specified All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 2: Only one output may be shorted at a time

Note 3: The flip flop will always recognize a 20 ns pulse, never recognize a 5 ns pulse

Note 4: No maximum rise and fall times are imposed upon clock or J and K waveforms However, very slow transitions which allow an input to remain in the threshold region can cause noise problems

Note 5: See explanation given under "Device Operation"

Note 6: J and K information will register properly even though the information is removed 5 ns before the clock pulse voltage falls However when this occurs it must be assured that the Logical "1" clock pulse level and the desired J and K information occur simultaneously for at least 20 ns

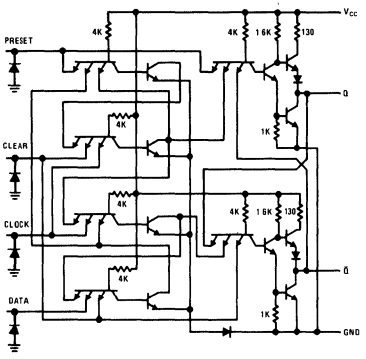
Series 54/74

DM5474/DM7474 (SN5474/SN7474) dual D flip flop

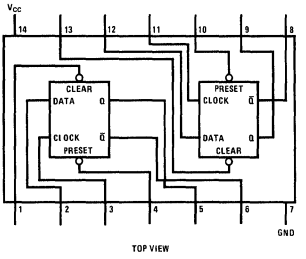
general description

The DM5474/DM7474 dual D flip flops are designed for use where the flexibility of two inputs, such as on a JK or an RS flip flop, are not required. If only a single input (two logic combinations) can be utilized, then an extra input is superfluous. The DM5474/DM7474 have only a single DATA input. The logical level applied to this DATA input is transferred to the Q output when the clock pulse voltage rises to a logical 1. It is only necessary to set-up information on the DATA input several nanoseconds before the clock pulse voltage rises; likewise it is only necessary to hold that information several nanoseconds after the clock pulse voltage reaches the logical 1 level. DATA information is then free to change in preparation for the next clock pulse. Since only one pin is used for data entry, fully asynchronous (both PRESET and CLEAR) capability can be provided in a 14 pin dual-in-line package.

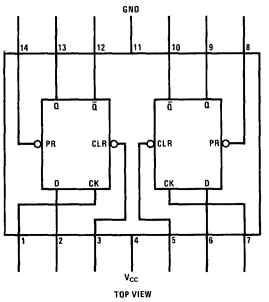
schematic and connection diagrams



DM5474/DM7474
Dual-In-Line Package



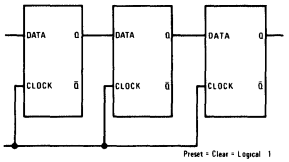
DM5474
Flat Package



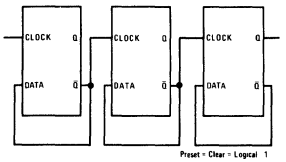
Note A logical 0 on CLEAR sets Q to a logical 0
A logical 0 on PRESET sets Q to a logical 1

typical applications

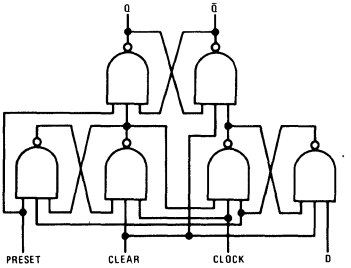
shift register



ripple counter (divide-by-2^n)



block diagram (each flip flop)



absolute maximum ratings

Supply Voltage		+7V
Input Voltage		5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM5474	−55°C to +125°C
	DM7474	0°C to +70°C
Lead Temperature (soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION			MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5 0V, I_{OUT} = −12 mA, T_A = 25°C					−1 5	V
Logical "1" Input Voltage	DM5474	V_{CC} = 4 5V			2 0			V
	DM7474	V_{CC} = 4 75V						
Logical "0" Input Voltage	DM5474	V_{CC} = 4.5V					0 80	V
	DM7474	V_{CC} = 4 75V						
Logical "1" Output Voltage	DM5474	V_{CC} = 4 5V	I_{OUT} = −400 μA		2 4	3.3		V
	DM7474	V_{CC} = 4 75V						
Logical "0" Output Voltage	DM5474	V_{CC} = 4 5V	I_{OUT} = 16 0 mA			0 15	0.4	V
	DM7474	V_{CC} = 4 75V						
Logical "0" Input Current	DM5474	V_{CC} = 5 5V	V_{IN} = 0 40V	Data or Preset		−1 0	−1.6	mA
	DM7474	V_{CC} = 5 25V		Clear or Clock		−2 0	−3.2	mA
Logical "1" Input Current	DM5474	V_{CC} = 5 5V	V_{IN} = 2 4V	Data or Preset			40.0	μA
	DM7474	V_{CC} = 5 25V		Clear or Clock			80 0	μA
Logical "1" Input Current	DM5474	V_{CC} = 5 5V	V_{IN} = 5 5V				1 0	mA
	DM7474	V_{CC} = 5 25V						
Output Short Current (Note 2)	DM5474	V_{CC} = 5 5V	V_{OUT} = 0V		−20 0		−55 0	mA
	DM7474	V_{CC} = 5 25V			−18 0			
Power Supply Current (each flip-flop)		V_{CC} = 5 0V, V_{IN} = 5 0V				8 2	13 0	mA
Maximum Clock Frequency		V_{CC} = 5 0V, T_A = 25°C	C = 50 pF		15 0	25 0		MHz
Propagation Delay Time to a Logical "0" from Clock — t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		13 0	22 0	45 0	ns
Propagation Delay Time to a Logical "1" from Clock — t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		10 0	16 0	30 0	ns
Propagation Delay Time to a Logical "0" from Clear, or Preset — t_{pd0}		V_{CC} = 5 0V, T_A = 25°C					40 0	ns
Propagation Delay Time to a Logical "1" from Clear, or Preset — t_{pd1}		V_{CC} = 5 0V, T_A = 25°C					25 0	ns
Time Prior to Clock Pulse that Data Information Must be Present — $t_{set\ up}$		V_{CC} = 5 0V, T_A = 25°C, C = 50 pF		Logical "1"		15.0	20 0	ns
				Logical "0"		15 0	20 0	ns
Time After Clock Pulse that Data Information Must be Held — t_{hold}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		Logical "1"		−5 0	0	ns
				Logical "0"		0.6	3 0	ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for DM5474 and 0°C to 70°C for DM7474 unless otherwise specified All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 2. Only one output may be shorted at a time

Series 54/74

DM5475/DM7475(SN5475/SN7475) quad latch

general description

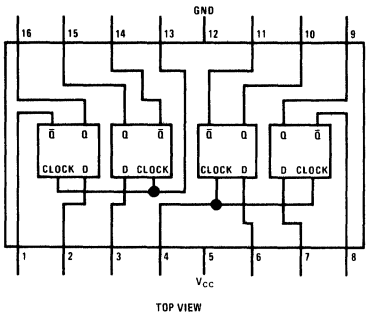
The DM5475/DM7475 is a four-bit storage element utilizing latch-connected gates to perform the memory function. TTL circuitry is employed providing fast speed and high noise immunity.

The information bits to be stored are applied to the D inputs. If the CLOCK input is in the logical 1 state, the Q output will follow the information applied to the corresponding D input. When the CLOCK is taken to the logical 0 state, whatever binary state was present on the D input at the time of this transition will be stored on the Q output. $\overline{Q}$ is also provided for added flexibility.

Two separate clock input lines are provided, each controlling two latches, so that other applications—such as a two-phase flip-flop—can be performed.

logic and connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

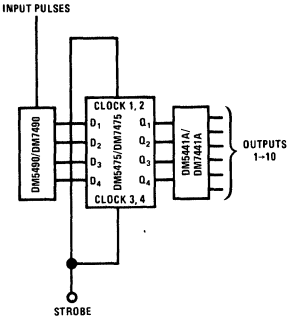
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

t_n = time previous to negative going clock transition

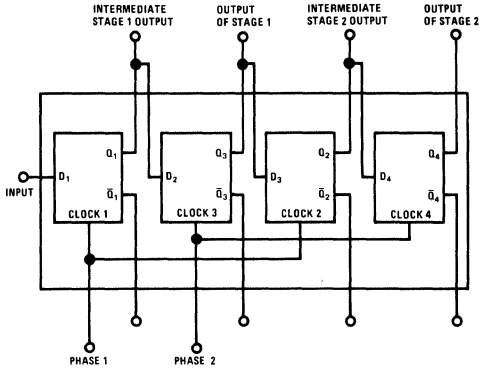
t_{n+1} = time after negative-going clock transition

typical applications

Buffer Storage for Indicators



Dual Rank Shift Register



absolute maximum ratings

Supply Voltage		+7V
Input Voltage		5.5V
Fanout		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM5475	−55°C to +125°C
	DM7475	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V I_{OUT} = −12 mA, T_A = 25°C		−.95	−1.5	V
Logical "1" Input Voltage	DM5475	V_{CC} = 4.5V	2.0			V
	DM7475	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM5475	V_{CC} = 4.5V			0.8	V
	DM7475	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM5475	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM7475	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM5475	V_{CC} = 4.5V, I_{OUT} = 16 mA			0.4	V
	DM7475	V_{CC} = 4.75V				
Logical "1" Input Current	DM5475	V_{CC} = 5.5V, V_{IN} = 2.4V, D			80	μA
	DM7475	V_{CC} = 5.25V, CLOCK			80	μA
Logical "1" Input Current	DM5475	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM7475	V_{CC} = 5.25V				
Logical "0" Input Current	DM5475	V_{CC} = 5.5V, V_{IN} = 0.4V, D		−2.1	−3.2	mA
	DM7475	V_{CC} = 5.25V, CLOCK		−2.1	−3.2	mA
Output Short Current (Note 2)	DM5475	V_{CC} = 5.5V, V_{OUT} = 0V	−20	−32	−55	mA
	DM7475	V_{CC} = 5.25V	−18			
Supply Current	DM5475	V_{CC} = 5.5V		32	46	mA
	DM7475	V_{CC} = 5.25V			50	mA
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	3	7	15	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	10	16	30	ns
Setup Time for a Logical "1", t_{s1}		V_{CC} = 5.0V, T_A = 25°C		10	20	ns
Setup Time for a Logical "0", t_{s0}		V_{CC} = 5.0V, T_A = 25°C		12	25	ns

Note 1: These specifications apply across the −55°C to +125°C temperature range for the DM5475 and the 0°C to +70°C temperature range for the DM7475 unless otherwise specified. Typicals apply only to 25°C @ V_{CC} = 5.0V.

Note 2: Only one output should be shorted at a time.

Series 54/74

DM5483/DM7483 (SN5483/SN7483)
4-bit binary full adder and dual single-bit binary full adder

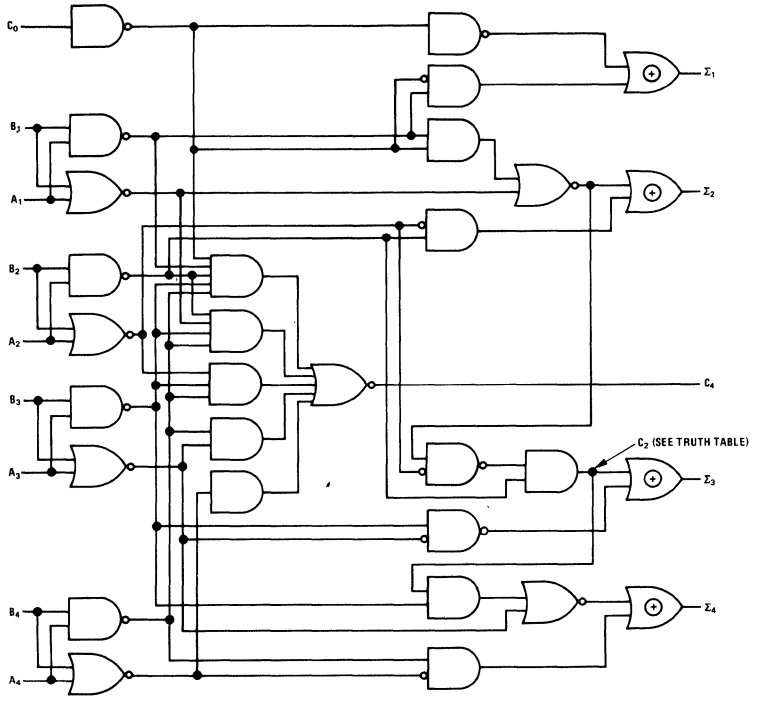
general description

The DM5483/DM7483 binary full adder adds two four-bit binary numbers. A carry input is included and four Σ outputs are provided along with the resultant carry. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Typical propagation delay from Carry-input to Carry output is 12 ns

The device can also be used as a dual single-bit binary full adder. (See application.) In this application the Σ_2 output is used as the CARRY output for BIT 1, and the $A_3 B_3$ inputs are used as the CARRY input for Bit 2.

It is completely compatible with other Series 54/74 devices

logic diagram



absolute maximum ratings

V_{CC}		7V
Input Voltage		5.5V
Operating Temperature Range	DM7483	0°C to 70°C
	DM5483	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
Logical "1" Input Voltage	DM5483	V_{CC} = 4.5V		2.0			V
	DM7483	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5483	V_{CC} = 4.5V				0.8	V
	DM7483	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5483	V_{CC} = 4.5V	V_{IN} = 0.8V, I_{OUT} = −400 μA (Note 3)	2.4			V
	DM7483	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5483	V_{CC} = 4.5V	V_{IN} = 2.0V, I_{OUT} = 16 mA (Note 3)			0.4	V
	DM7483	V_{CC} = 4.75V					
Logical "1" Input Current (all inputs)	DM5483	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM7483	V_{CC} = 5.25V					
Logical "1" Input Current	DM5483	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7483	V_{CC} = 5.25V					
Logical "0" Input Current (all inputs)	DM5483	V_{CC} = 5.5V	V_{IN} = 0.4V			−3.2	mA
	DM7483	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2) (except C_4)	DM5483	V_{CC} = 5.5V		−20		−55	mA
	DM7483	V_{CC} = 5.25V		−18			
Output Short Circuit Current (for C_4)	DM5483	V_{CC} = 5.5V		−27		−70	mA
	DM7483	V_{CC} = 5.25V					
Supply Current	DM5483	V_{CC} = 5.5V			58	79	mA
	DM7483	V_{CC} = 5.25V					

switching characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITION	MIN	TYP	MAX	UNITS
t_{pd1}	C_{IN}	Σ_1	N = 10, C = 50 pF		23	34	ns
t_{pd0}			N = 10, C = 50 pF		20	34	ns
t_{pd1}	C_{IN}	Σ_2	N = 10, C = 50 pF		24	35	ns
t_{pd0}			N = 10, C = 50 pF		22	35	ns
t_{pd1}	C_{IN}	Σ_3	N = 10, C = 50 pF		30	50	ns
t_{pd0}			N = 10, C = 50 pF		24	40	ns
t_{pd1}	C_{IN}	Σ_4	N = 10, C = 50 pF		30	50	ns
t_{pd0}			N = 10, C = 50 pF		28	50	ns
t_{pd1}	C_{IN}	C_4	N = 5, C = 15 pF		12	20	ns
t_{pd0}			N = 5, C = 15 pF		12	20	ns
t_{pd1}	A_2 or B_2	Σ_2	N = 10, C = 50 pF			40	ns
t_{pd0}			N = 10, C = 50 pF			35	ns
t_{pd1}	A_4 or B_4	Σ_4	N = 10, C = 50 pF			40	ns
t_{pd0}			N = 10, C = 50 pF			35	ns

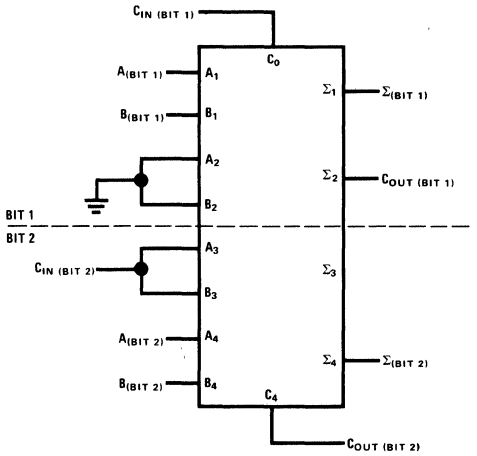
Note 1: Min/Max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7483 and −55°C to +125°C for the DM5483 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 2: Only one output at a time should be short circuited.

Note 3: For C_4 output, $I_{OUT(1)}$ = −200 μA, $I_{OUT(0)}$ = 8 mA

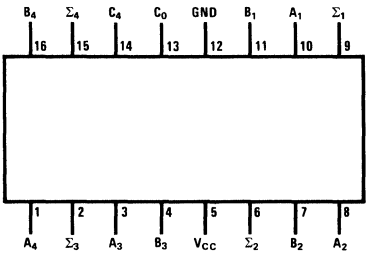
typical application

Connect the DM5483/DM7483 in the following manner to implement a dual single-bit full adder.



connection diagram

Dual-In-Line and Flat Package



truth table (See Note 1)

INPUT							OUTPUT					
							WHEN C_{in} = 0			WHEN C_{in} = 1		
							WHEN C_2 = 0			WHEN C_2 = 1		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note 1: Input conditions at A_1, A_2, B_1, B_2, and C_{in} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

Series 54/74

DM5486/DM7486(SN5486/SN7486) quad EXCLUSIVE-OR gate

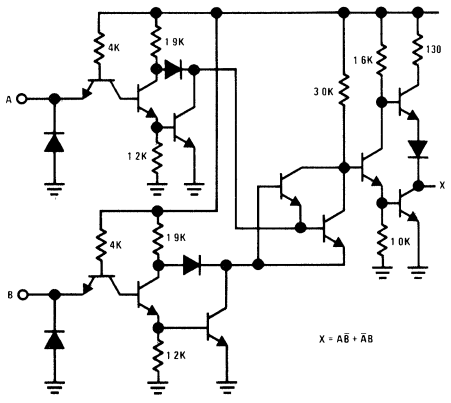
general description

The DM5486/DM7486 utilizes TTL (Transistor-Transistor Logic) to provide four exclusive-OR gates in one package. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The device is completely compatible with other Series 54/74 devices.

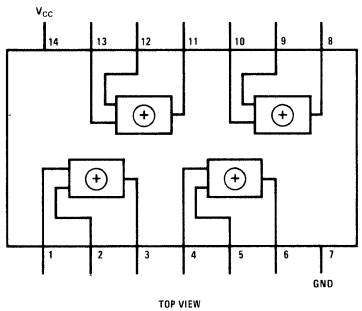
features

- Input clamp diodes
- Typical noise immunity 1V
- Average propagation delay 15 ns
- Average power dissipation 40 mW per gate

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

V_{CC}		7.0V
Input Voltage		5.5V
Operating Temperature Range	DM7486	0°C to 70°C
	DM5486	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Fan Out		10
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
Logical "1" Input Voltage	DM5486	V_{CC} = 4.5V		2.0			V
	DM7486	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5486	V_{CC} = 4.5V				0.8	V
	DM7486	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5486	V_{CC} = 4.5V		2.4			V
	DM7486	V_{CC} = 4.75V, Input Conditions 0.8V & 2.0V or 2.0V & .8V, I_{OUT} = −400 μA					
Logical "0" Output Voltage	DM5486	V_{CC} = 4.5V				0.4	V
	DM7486	V_{CC} = 4.75V, Input Conditions 0.8V & 0.8V or 2.0V & 2.0V, I_{OUT} = 16 mA					
Logical "1" Input Current	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 2.4V				40	μA
Logical "1" Input Current	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
Logical "0" Input Current	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 0.4V				−1.6	mA
Output Short Circuit Current (Note 2)	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 0V		−18.0		−55	mA
Supply Current Logical "0" (Each Gate)	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V Both Inputs Logical "1" (Worst Case)			9.0	14.2	mA
Supply Current Logical "1" (Each Gate)	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, One Input Logical "1", One Input Logical "0"			7.0	10.5	mA
Propagation Delay Time to Logical "0", t_{pd0} (Note 3)		V_{CC} = 5.0V, T_A = 25°C, F.O. = 10 C_o = 50 pF	Inv.	7	12	20	ns
			Non-Inv	7	12	20	ns
Propagation Delay Time to Logical "1", t_{pd1} (Note 3)		V_{CC} = 5.0V, T_A = 25°C, F.O. = 10 C_o = 50 pF	Inv	10	19	30	ns
			Non Inv	8	14.5	23	ns

Note 1. Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7486 and −55°C to +125°C for the DM5486 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2. Not more than one output should be shorted at a time.

Note 3. For explanation of the inverting and non-inverting specs, see the AC test circuit and AC waveforms.

Series 54/74

DM5488/DM7488(SN5488/SN7488)
256-bit read only memory

general description

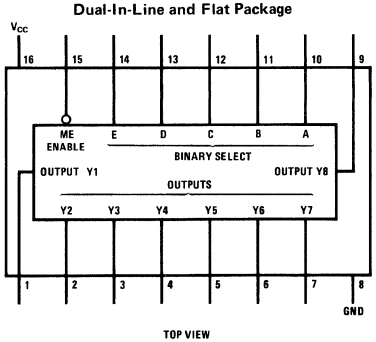
The DM5488/DM7488 is a custom-programmed 256-bit read-only memory organized as 32 8-bit words. A 5-bit input code selects the appropriate word which then appears on the eight outputs. An enable input overrides the address inputs and turns off all eight output transistors.

features

- Organized as 32 8-bit words
- Open collector outputs provide expansion to greater numbers of words
- On-chip decoding
- 30 ns typical access time
- 250 mW typical power dissipation
- Input clamp diodes

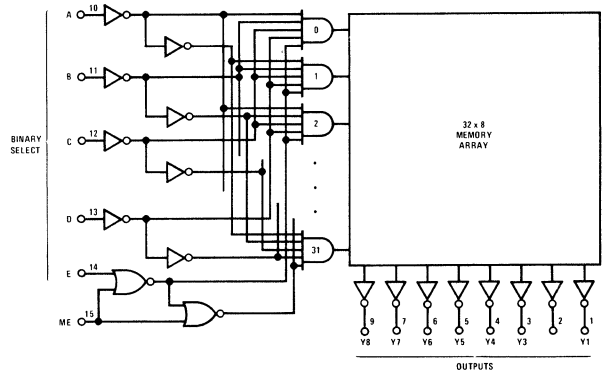
connection diagram

Dual-In-Line and Flat Package



TOP VIEW

block diagram



absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM5488	−55°C to +125°C
	DM7488	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5488	V_{CC} = 4.5V		2.0			V
	DM7488	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5488	V_{CC} = 4.5V				0.8	V
	DM7488	V_{CC} = 4.75V					
Logical "1" Output Current	DM5488	V_{CC} = 5.5V	V_O = 5.5V			100	μA
	DM7488	V_{CC} = 5.25V				40	μA
Logical "0" Output Voltage	DM5488	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM7488	V_{CC} = 4.75V					
Logical "1" Input Current	DM5488	V_{CC} = 5.5V	V_I = 2 4V			40	μA
	DM7488	V_{CC} = 5.25V					
	DM5488	V_{CC} = 5.5V	V_I = 5.5V			1	mA
	DM7488	V_{CC} = 5.25V					
Logical "0" Input Current	DM5488	V_{CC} = 5.5V	V_I = 0.4V			−1.6	mA
	DM7488	V_{CC} = 5 25V					
Supply Current	DM5488	V_{CC} = 5.5V			50	80	mA
	DM7488	V_{CC} = 5.25V					
Input Clamp Voltage	DM5488	V_{CC} = 4.5V	I_I = −12 mA			−1.5	V
	DM7488	V_{CC} = 4.75V					
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C_L = 15 pF		32	50	ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C_L = 15 pF		34	50	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C_L = 15 pF		28	50	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C_L = 15 pF		27	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5488 and across the 0°C to 70°C range for the DM7488. All typicals are given for V_{CC} = 5 0V and T_A = 25°C.

truth tables

DM5488A/DM7488A SINE LOOK-UP TABLE

A pattern has been generated for the DM5488/DM7488. The AA pattern provides a sine table. The 5-bit input code linearly divides 90° into 32 equal segments. Each 8-bit output is therefore the sine of the angle applied.

EXAMPLE: Input 11010 means 26/32 of 90°, or about 73°. The corresponding output 11110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about .95, which is close to the sine of 73°. Rounding-off has not been employed, since without rounding-off it is possible to extend the accuracy with additional ROMs.

	INPUTS						OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
2	0	0	0	1	0	0	0	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	0	1	0	0	1	0	1
4	0	0	1	0	0	0	0	0	1	1	0	0	0	1
5	0	0	1	0	1	0	0	0	1	1	1	1	1	0
6	0	0	1	1	0	0	0	1	0	0	1	0	1	0
7	0	0	1	1	1	0	0	1	0	1	0	1	1	0
8	0	1	0	0	0	0	0	1	1	0	0	0	0	1
9	0	1	0	0	1	0	0	1	1	0	1	1	0	1
10	0	1	0	1	0	0	0	1	1	1	1	0	0	0
11	0	1	0	1	1	0	1	0	0	0	0	0	1	1
12	0	1	1	0	0	0	1	0	0	0	1	1	1	0
13	0	1	1	0	1	0	1	0	0	1	1	0	0	0
14	0	1	1	1	0	0	1	0	1	0	0	0	1	0
15	0	1	1	1	1	0	1	0	1	0	1	0	1	1
16	1	0	0	0	0	0	1	0	1	1	0	1	0	1
17	1	0	0	0	1	0	1	0	1	1	1	1	0	1
18	1	0	0	1	0	0	1	1	0	0	0	1	0	1
19	1	0	0	1	1	0	1	1	0	0	1	1	0	1
20	1	0	1	0	0	0	1	1	0	1	0	1	0	0
21	1	0	1	0	1	0	1	1	0	1	1	0	1	1
22	1	0	1	1	0	0	1	1	1	0	0	0	0	1
23	1	0	1	1	1	0	1	1	1	0	0	1	1	1
24	1	1	0	0	0	0	1	1	1	0	1	1	0	0
25	1	1	0	0	1	0	1	1	1	1	0	0	0	1
26	1	1	0	1	0	0	1	1	1	1	0	1	0	0
27	1	1	0	1	1	0	1	1	1	1	1	0	0	0
28	1	1	1	0	0	0	1	1	1	1	1	0	1	1
29	1	1	1	0	1	0	1	1	1	1	1	1	0	1
30	1	1	1	1	0	0	1	1	1	1	1	1	1	0
31	1	1	1	1	1	0	1	1	1	1	1	1	1	1
All	X	X	X	X	X	1	1	1	1	1	1	1	1	1

X = Don't Care

truth tables (cont.)

DM5488/DM7488 TRUTH TABLE

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits). The customer does this by filling out the truth table on this data sheet, and sending it in with his purchase order.

	INPUTS						OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
All	X	X	X	X	X	1	1	1	1	1	1	1	1	1

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits) The customer does this by filling out the truth table on this data sheet, and sending it in with his purchase order

X = Don't Care
Notice This sheet must be completed and signed by an authorized representative of the customer's company before an order can be entered

To be used by National only

_____ Part Number

_____ S O Number

_____ Date Received

Authorized Representative _____ Date _____

Company _____

Desired Part ☐ DM5488 ☐ DM7488

Series 54/74

DM5489/DM7489 (SN5489/SN7489)
64-bit random access read/write memory

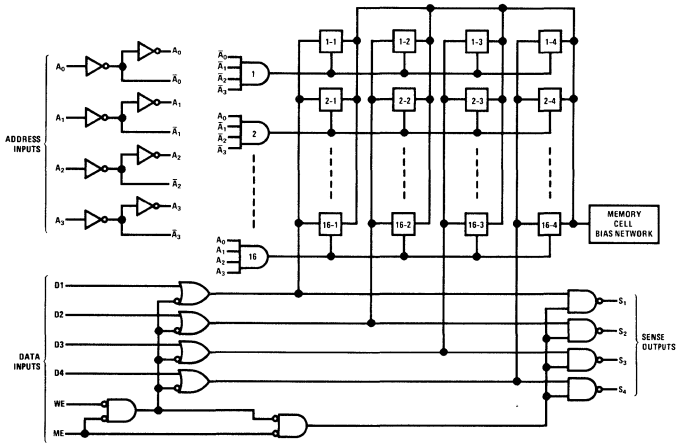
general description

The DM5489/DM7489 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

features

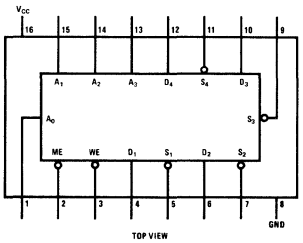
- Series 54/74 compatible
- Organized as 16 4-bit words
- Typical access from chip enable 20 ns
- Typical access time 40 ns
- Typical power dissipation 400 mW
- Open collector outputs to permit "wire OR" capability

block diagram



connection diagram

Dual-In-Line Package



truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM5489	−55°C to +125°C
DM7489	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5489	V_{CC} = 4.5V		2.0			V
	DM7489	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5489	V_{CC} = 4.5V				0.8	V
	DM7489	V_{CC} = 4.75V					
Logical "1" Output Current	DM5489	V_{CC} = 5.5V	V_O = 5.25V			100	μA
	DM7489	V_{CC} = 5.25V				20	μA
Logical "0" Output Voltage	DM5489	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM7489	V_{CC} = 4.75V					
Logical "1" Input Current	DM5489	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7489	V_{CC} = 5.25V					
	DM5489	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7489	V_{CC} = 5.25V					
Logical "0" Input Current	DM5489	V_{CC} = 5.5V				−1.6	mA
	DM7489	V_{CC} = 5.25V					
Supply Current	DM5489	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM7489	V_{CC} = 5.25V					
Input Clamp Voltage	DM5489	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM7489	V_{CC} = 4.75V					
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C			29	60	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C			16	30	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C			37	60	ns
Propagation Delay to a Logical "1" from Enable to Output to, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C			33	50	ns
Output Capacitance		V_O = 2.0V, f = 1 MHz			6		pF
Input Capacitance		V_{IN} = 2.0V, f = 1 MHz			4		pF
Write Enable Pulse Width				40	23		ns
Setup Time, Data Input with respect to Write Enable				0	−15		ns
Hold Time, Data Input				0	−14		ns
Setup Time, Address Input				0	−17		ns
Hold Time, Address Input				5	−7		ns
Sense Recovery Time After Writing					40	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5489 and across the 0°C to 70°C range for the DM7489. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Series 54/74

DM5490/DM7490(SN5490/SN7490) decade counter
DM5492/DM7492(SN5492/SN7492) divide-by-12 counter
DM5493/DM7493(SN5493/SN7493) 4 -bit binary counter

general description

These TTL (Transistor-Transistor-Logic) monolithic counters are capable of counting pulses at a guaranteed frequency of 20 MHz. Gating is provided to reset the counters to the more popular states. Characteristics include high speed at moderate power dissipation, high noise immunity, and minimal variation in performance over temperature. These circuits are completely compatible with other series 54/74 devices.

To provide greater flexibility, the counters may be used in any of the modes as follows:

DM5490/DM7490

1. BCD decade counter—connect the A output to the BD input. This is the normal mode of operation.
2. Symmetrical divide-by-ten operation—connect the D output to the A input. When pulses are then applied to the BD input, a symmetrical waveform one tenth of the applied frequency will appear at the A output.
3. Divide-by-five operation—if no external connections are made a frequency division of five will result between the BD input and the D output. This allows the flip flop A to be used to divide-by-two if desired.

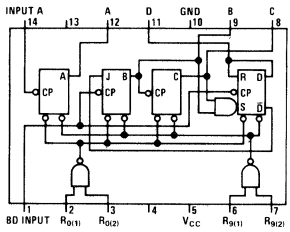
DM5492/DM7492

1. When used as a divide-by-twelve counter output A is connected to the BC input. In this mode outputs A, C, and D provide divisions by 2, 6, and 12 respectively.
2. When the connection is not made between A and BC, and when an input frequency is applied to the BC input, a frequency division of 3 and 6 results on the C and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.

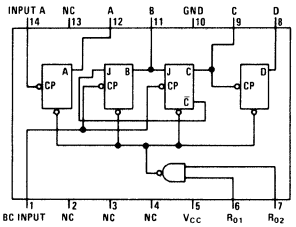
DM5493/DM7493

1. When used as a four-bit binary counter, output A is connected to the B input. In this mode outputs A, B, C, and D provide divisions by 2, 4, 8, and 16 respectively.
2. When the connection is not made between A and B and when an input frequency is applied to the B input, a frequency division of 2, 4 and 8 results on the B, C, and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.

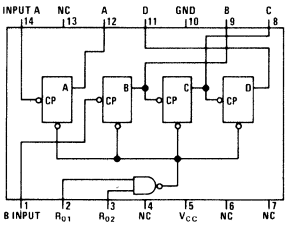
logic and connection diagrams (Dual-In-Line and Flat Packages)



DM5490/DM7490



DM5492/DM7492



DM5493/DM7493

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DM5490, DM5492, DM5493	−55°C to +125°C
DM7490, DM7492, DM7493	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA		−1.0	−1.5	mA
Logical "1" Input Voltage	DM5490, 92, 93	V_{CC} = 4.5V		2.0			V
	DM7490, 92, 93	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5490, 92, 93	V_{CC} = 4.5V				.8	V
	DM7490, 92, 93	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5490, 92, 93	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM7490, 92, 93	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5490, 92, 93	V_{CC} = 4.5V	I_{OUT} = 16 mA		.2	.4	V
	DM7490, 92, 93	V_{CC} = 4.75V					
Logical "1" Input Current	DM5490, 92, 93	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7490, 92, 93	V_{CC} = 5.25V					
Output Short Circuit Current	DM5490, 92, 93	V_{CC} = 5 5V	(Note 2)	20		55	mA
	DM7490, 92, 93	V_{CC} = 5.25V		18		55	
DM5490/DM7490							
Logical "1" Input Current	DM5490	V_{CC} = 5.5V	V_{IN} = 2.4V				
	DM7490	V_{CC} = 5 25V					
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$						40	μA
A						80	μA
BD						160	μA
Logical "0" Input Current	DM5490	V_{CC} = 5.5V	V_{IN} = .4V				
	DM7490	V_{CC} 5.25V					
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$						1.6	mA
A						3.2	mA
BD						6 4	mA
Supply Current	DM5490	V_{CC} = 5.5V			32	45	mA
	DM7490	V_{CC} = 5.25V					
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16	35	ns
	B				35	60	ns
	C				50	80	ns
	D				35	60	ns
Propagation Delay Time to a Logical "0" Level From Input to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19	35	ns
	B				35	60	ns
	C				50	80	ns
	D				35	60	ns
Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C		15	8		ns
DM5492/DM7492							
Logical "1" Input Current	DM5492	V_{CC} = 5.5V	V_{IN} = 2.4V				
	DM7492	V_{CC} = 5.25V					
$R_{0(1)}$, $R_{0(2)}$						40	μA
A						80	μA
BC						160	μA

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DM5492/DM7492 (Continued)							
Logical "0" Input Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$						1.6	mA
A						3.2	mA
BC						6.4	mA
Supply Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} (R_0) = 4.5V		30	43	mA
Maximum Input Frequency		V_{CC} = 5.0V, F O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input A to Output	A / B / C / D	F O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16 35 35 50	35 60 60 80	ns ns ns ns
Propagation Delay Time to a Logical "0" Level From Input A to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19 35 35 50	35 60 60 80	ns ns ns ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns
DM5493/DM7493							
Logical "1" Input Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$						40	μA
A, B						80	μA
Logical "0" Input Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$						1.6	mA
A, B						3.2	mA
Supply Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V			30	43	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16 35 50 65	35 60 80 100	ns ns ns ns
Propagation Delay Time to a Logical "0" Level From Input to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19 35 50 64	35 60 80 100	ns ns ns ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5490, DM5492 and DM5493 and 0°C to 70°C for the DM7490, DM7492 and DM7493 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Only one output may be shorted at a time.

Note 3: The flip flop will always recognize a 15 ns pulse.

BCD count sequence

DM5490/DM7490

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET OPERATION

To reset the counter to the BCD count of zero, both Reset 0 inputs must be at logical "1" levels while at least one Reset 9 input is at a logical "0" level.

To reset the counter to the BCD count of nine, both Reset 9 inputs must be at logical "1" levels; while at least one Reset 0 input is at a logical "0".

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs and at least one of the Reset 9 inputs must be at a logical "0" for proper counting.
3 For ÷ 10 counting, connect the A output to the BD input.

count sequence

DM5492/DM7492

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

RESET OPERATION

To reset the counter to the count of zero, both Reset 0 inputs must be at logical "1" levels.

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs must be at a logical "0" for proper counting.
3. For ÷12 counting, connect the A output to the BC input.

DM5493/DM7493

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

RESET OPERATION

To reset the counter to the count of zero, both Reset 0 inputs must be at logical "1" levels.

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs must be at a logical "0" for proper counting.
3. For ÷16 counting, connect the A output to the B input.

Series 54/74

DM5495/DM7495(SN5495/SN7495)
4-bit right-shift/left-shift register

general description

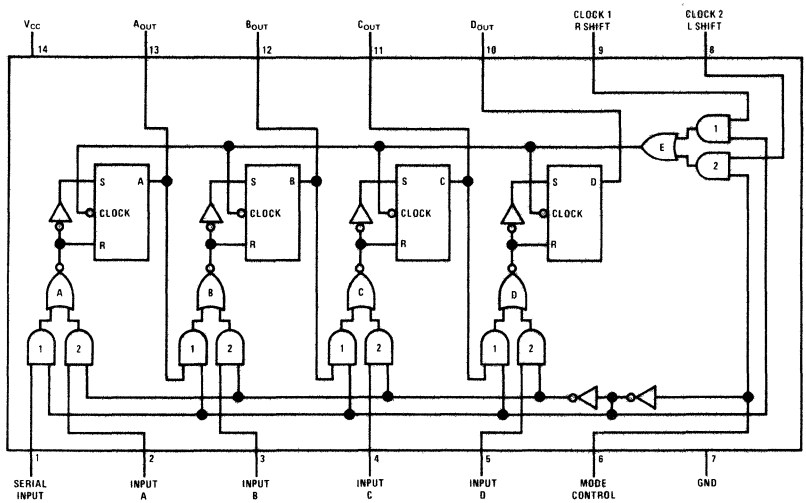
The DM5495/DM7495 is a TTL (Transistor-Transistor Logic) monolithic four-bit parallel-in parallel-out shift register employing four R-S master-slave flip flops, internal clock buffers and control gating for either right-shift or left-shift operation. Separate clocks are provided for right-shift and left-shift operation. A mode control input enables right-shift or left-shift operation, depending on whether its input is a zero or one respectively. Data transfer occurs on the negative transition of the clock pulse. The three modes of operation are explained on the following pages.

features

- Input Clamping Diodes
- Typical Noise Immunity 1.0V
- High Clock Rate 35 MHz

logic and connection diagram

Dual-In-Line and Flat Package



POSITIVE LOGIC
MODE CONTROL = 0 FOR RIGHT SHIFT
MODE CONTROL = 1 FOR LEFT SHIFT OR PARALLEL LOAD

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM5495	−55°C to +125°C
	DM7495	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5495	V_{CC} = 4.5V	2			V
	DM7495	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM5495	V_{CC} = 4.5V			0.8	V
	DM7495	V_{CC} = 4.75				
Logical "1" Output Voltage	DM5495	V_{CC} = 4.5V	2.4			V
	DM7495	V_{CC} = 4.75V, I_{load} = −400 μA				
Logical "0" Output Voltage	DM5495	V_{CC} = 4.5V			0.4	V
	DM7495	V_{CC} = 4.75V, I_{sink} = 16 mA				
Logical "0" Input Current (at any Input Except Mode Control)	DM5495	V_{CC} = 5.5V			−1.6	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 0.4V				
Logical "0" Input Current at Mode Control	DM5495	V_{CC} = 5.5V			−3.2	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 0.4V				
Logical "1" Input Current (at any Input Except Mode Control)	DM5495	V_{CC} = 5.5V			40	μA
	DM7495	V_{CC} = 5.25V, V_{IN} = 2.4V				
	DM5495	V_{CC} = 5.5V			1	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 5.5V				
Logical "1" Input Current at Mode Control	DM5495	V_{CC} = 5.5V			80	μA
	DM7495	V_{CC} = 5.25V, V_{IN} = 2.4V				
	DM5495	V_{CC} = 5.5V			1	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 5.5V				
Short-Circuit Output Current (Note 2)	DM5495	V_{CC} = 5.5V	−18		−57	mA
	DM7495	V_{CC} = 5.25V				
Supply Current	DM5495	V_{CC} = 5.5V		50	80	mA
	DM7495	V_{CC} = 5.25V				
Input Diode Clamp Voltage		T_A = 25°C, I_{IN} = −12 mA, V_{CC} = 5.0V			−1.5	V

switching characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Shift Frequency	C_L = 50 pF, R_L = 400Ω	20	35		MHz
Propagation Delay Time to Logical "1" Level from Clock 1 or 2 to Outputs	C_L = 50 pF, R_L = 400Ω		26	35	ns
Propagation Delay Time to Logical "0" from Clock 1 or 2 to Outputs	C_L = 50 pF, R_L = 400Ω		24	35	ns

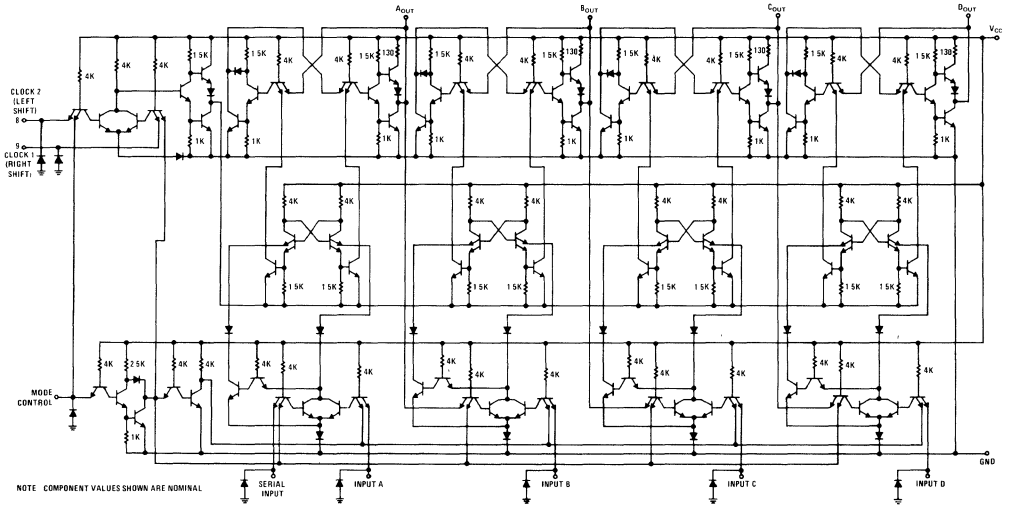
Note 1: Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5495 and 0°C to 70°C for the DM7495 unless otherwise specified. All typicals are given for T_A = 25°C and V_{CC} = 5.0V.

Note 2: Not more than one output should be shorted at a time.

recommended operating conditions

OPERATING CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	DM5495	4.5	5	5.5	V
	DM7495	4.75	5	5.25	V
Clock Pulse Width, $t_{p\ (clock)}$		15	10		ns
Setup Time Required at Serial, A,B,C, or D Inputs, t_{setup}		20	10		ns
Hold Time Required at Serial, A,B,C, or D Inputs, t_{hold}		0	-10		ns
Logical "0" Level Setup Time Required at Mode Control $t_{A(0)}$ (With Respect to Clock 1 Input)		20			ns
Logical "1" Level Setup Time Required at Mode Control $t_{B(1)}$ (With Respect to Clock 2 Input)		15			ns
Logical "0" Level Setup Time Required at Mode Control $t_{C(0)}$ (With Respect to Clock 2 Input)		10			ns
Logical "1" Level Setup Time Required at Mode Control $t_{D(1)}$ (With Respect to Clock 1 Input)		10			ns

schematic diagram



Series 54/74

DM5496/DM7496(SN5496/SN7496)

5-bit parallel-in/parallel-out shift register

general description

The DM5496/DM7496 may be used as a serial-to-parallel converter, parallel-to-serial converter, or storage register. Inputs and outputs of the five R-S master-slave flip-flops are accessible, permitting parallel-in/parallel-out and serial-in/serial-out operation, as well as serial/parallel conversions.

features

- Typical propagation delay of 25 ns
- Minimum clock pulse width of 35 ns
- Fanout of 10
- Multifunction capability
- Expansion to N bits as register or converter.

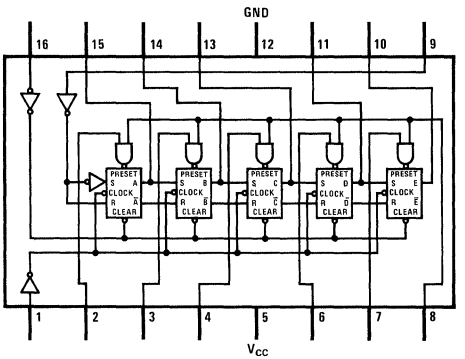
operation

A logical "0" voltage applied to the clear input simultaneously sets all flip-flops to the "0" state independent of the clock input state. Any flip-flops may be set independently to "1" by "1" inputs on the common preset input and on the preset inputs of the specific flip-flops to be set. Preset is also independent of clock state.

Information is transferred to the output pins when the clock input goes from a logical "0" to a logical "1". The clear input must be at "1" and the preset input at "0" when clocking occurs. Since the flip-flops are R-S master-slave type, the proper information must appear at the R-S inputs before the clock edge rises. The serial input provides this information to the first flip-flop and the flip-flop outputs provide the information to the remaining R-S inputs.

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Supply Voltage	7 0V
Input Voltage	5 5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5496	4 5	5 5	V
DM7496	4 75	5 25	V
Temperature (T_A)			
DM5496	−55	+125	°C
DM7496	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −400 μA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current					
Preset Enable Input (Pin 8)	V_{CC} = Max, V_{IN} = 2 4V			200	μV
	V_{CC} = Max, V_{IN} = 5 5V			1.0	mA
All Other Inputs	V_{CC} = Max, V_{IN} = 2 4V			40	μV
	V_{CC} = Max, V_{IN} = 5 5V			1 0	mA
Logical "0" Input Current					
Preset Enable Input (Pin 8)	V_{CC} = Max, V_{IN} = 0 4V			−8 0	mA
All Other Inputs	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_{OUT} = 0 DM5496	−20		−55	mA
	V_{CC} = Max, V_{OUT} = 0 DM7496	−18		−55	mA
Supply Current — Logical "1" (Each Device)					
Supply Current - Logical "0"	V_{CC} = Max DM5496		48	68	mA
	V_{CC} = Max DM7496		48	79	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		25	40	ns
Propagation Delay to a Logical "0" from Clear to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω			55	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		25	40	ns
Propagation Delay to a Logical "1" from Preset or Preset Enable to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		25	35	ns
Maximum Clock Frequency	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	10			MHz
Width of Clock Pulse, $t_{p(CLOCK)}$	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	35			ns
Width of Clear Pulse, $t_{p(CLEAR)}$	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	30			ns
Width of Preset Pulse, $t_{p(PRESET)}$	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	30			ns
Serial Input Setup Time, t_{SETUP}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	30			ns
Serial Input Hold Time, t_{HOLD}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5496 and across the 0°C to 70°C range for the DM7496 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54/74

DM54121/DM74121 (SN54121/SN74121) monostable multivibrator

general description

The DM54121/DM74121 TTL monostable multivibrator features DC triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1V per second, providing the circuit with an excellent noise immunity of typically 1.2V. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 30 ns to 40 seconds by choosing appropriate timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(OUT)} = C_T R_T \log_e 2$.

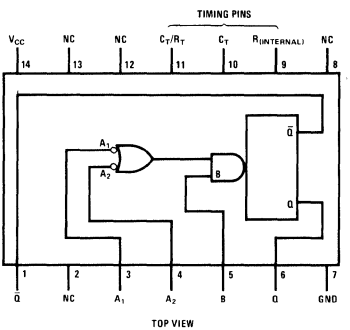
Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse width jitter is allowed.

features

- Series 54/74 compatibility
- DC triggering
- Schmitt trigger inputs
- Positive-going or negative-going triggering
- Pulse width variation from 30 ns to 40 sec
- Pulse width virtually independent of V_{CC} and temperature
- Typical power dissipation
  90 mW (50% duty cycle)
  65 mW (Quiescent state)
- Output pulse width independent of input pulse width

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

t_n INPUT			t_{n+1} INPUT			OUTPUT
A_1	A_2	B	A_1	A_2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

NOTES

t_n = Time before input transition
t_{n+1} = Time after input transition
x = Don't care

absolute maximum ratings (Note 1)

V_{CC}	7 0V
Input Voltage	5.5V
Operating Temperature Range DM54121	−55°C to +125°C
DM74121	0°C to 75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		LIMITS (Note 2) MIN	TYP	MAX	UNITS
Positive-Going Threshold Voltage at A Input, V_{T+}	DM54121	V_{CC} = 4 5V			1.4	2	V
	DM74121	V_{CC} = 4.75V					
Negative Going Threshold Voltage at A Input, V_{T-}	DM54121	V_{CC} = 4 5V		0 8	1.4		V
	DM74121	V_{CC} = 4 75V					
Positive-Going Threshold Voltage at B Input, V_{T+}	DM54121	V_{CC} = 4 5V			1 55	2	V
	DM74121	V_{CC} = 4 75V					
Negative-Going Threshold Voltage at B Input, V_{T-}	DM54121	V_{CC} = 4 5V		0 8	1 35		V
	DM74121	V_{CC} = 4 75V					
Logical "0" Output Voltage, $V_{OUT(0)}$	DM54121	V_{CC} = 4 5V	I_{SINK} = 16 mA		0.23	0 4	V
	DM74121	V_{CC} = 4 75V					
Logical "1" Output Voltage, $V_{OUT(1)}$	DM54121	V_{CC} = 4 5V	I_{LOAD} = −400 μA	2.4	3 3		V
	DM74121	V_{CC} = 4 75V					
Logical "0" Level Input Current at A1 or A2, $I_{IN(0)}$	DM54121	V_{CC} = 5 5V	V_{IN} = 0 4V		−1	−1.6	mA
	DM74121	V_{CC} = 5 25V					
Logical "0" Level Input Current at B, $I_{IN(0)}$	DM54121	V_{CC} = 5.5V	V_{IN} = 0 4V		−2	−3 2	mA
	DM74121	V_{CC} = 5 25V					
Logical "1" Level Input Current at A1 or A2, $I_{IN(1)}$	DM54121	V_{CC} = 5 5V	V_{IN} = 2.4V		1 5	40	μA
	DM74121	V_{CC} = 5.25V	V_{IN} = 5.5V		0 02	1	mA
Logical "1" Level Input Current at B, $I_{IN(1)}$	DM54121	V_{CC} = 5 5V	V_{IN} = 2 4V		3	40	μA
	DM74121	V_{CC} = 5.25V	V_{IN} = 5 5V		0 05	1	mA
Short Circuit Output Current at Q or $\overline{Q}$, I_{OS} (Note 3)	DM54121	V_{CC} = 5 5V		−20		−55	mA
	DM74121	V_{CC} = 5 25V		−18		−55	mA
Power Supply Current in Quiescent (Unfired) State, I_{CC}	DM54121	V_{CC} = 5 5V			13	25	mA
	DM74121	V_{CC} = 5 25V					
Power Supply Current in Fired State, I_{CC}	DM54121	V_{CC} = 5 5V			23	40	mA
	DM74121	V_{CC} = 5 25V					

switching characteristics V_{CC} = 5V, T_A = 25°C

	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" Level from B Input to Q Output, t_{pd1}	C_L = 15 pF, C_T = 80 pF, R_T = Internal	15	25	55	ns
Propagation Delay Time to Logical "1" Level from A1/A2 Inputs to Q Output, t_{pd1}	C_L = 15 pF, C_T = 80 pF, R_T = Internal	25	34	70	ns
Propagation Delay Time to Logical "0" Level from B Input to $\overline{Q}$ Output, t_{pd0}	C_L = 15 pF, C_T = 80 pF	20	32	65	ns
Propagation Delay Time to Logical "0" Level from A1/A2 Inputs to $\overline{Q}$ Output, t_{pd0}	C_L = 15 pF, C_T = 80 pF	30	39	80	ns
Pulse Width Obtained Using Internal Timing Resistor, $t_{p(OUT)}$	C_L = 15 pF, C_T = 80 pF, R_T = Open, Pin 9 to V_{CC}	70	110	150	ns
Pulse Width Obtained with Zero Timing Capacitance, $t_{p(OUT)}$	C_L = 15 pF, C_T = 0, R_T = Open, Pin 9 to V_{CC}	17	23	50	ns
Pulse Width Obtained Using External Timing Resistor, $t_{p(OUT)}$	C_L = 15 pF, C_T = 100 pF, R_T = 10 kΩ, Pin 9 Open	600	700	800	ns
Pulse Width Obtained Using External Timing Resistor, $t_{p(OUT)}$	C_L = 15 pF, C_T = 1 μF, R_T = 10 kΩ, Pin 9 Open	6	7	8	ms
Minimum Duration of Trigger Pulse, t_{HOLD}	C_L = 15 pF, C_T = 80 pF, R_T = Open, Pin 9 to V_{CC}		22	50	ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54121 and across the 0°C to 70°C range for the DM74121 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3 Only one output at a time should be shorted

Series 54/74

DM54150/DM74150(SN54150/SN74150)
16-line to 1-line multiplexer

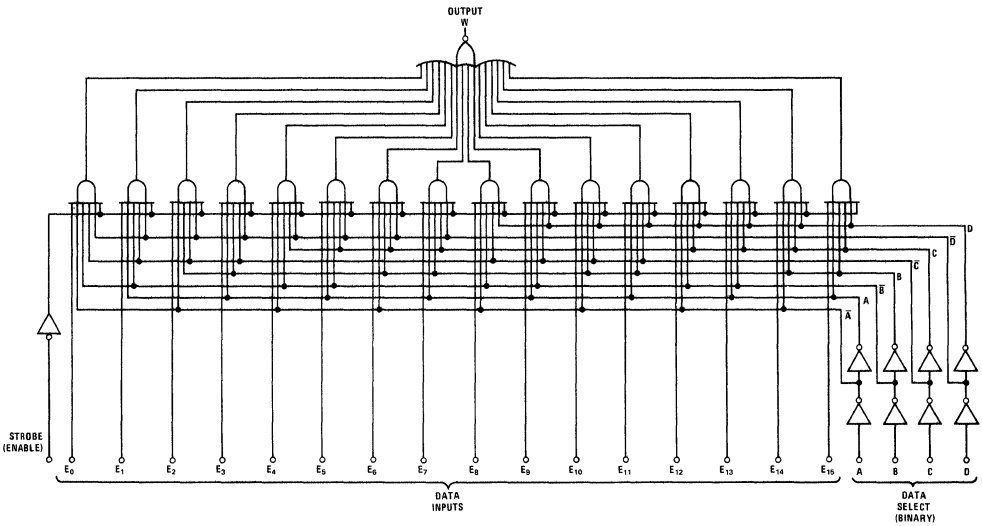
general description

The DM54150/DM74150 multiplexes sixteen digital lines to one output. A four-bit code determines the particular one-of-sixteen inputs which is routed to the output. The data is inverted from input to output. A strobe override places the output in the logical 1 state.

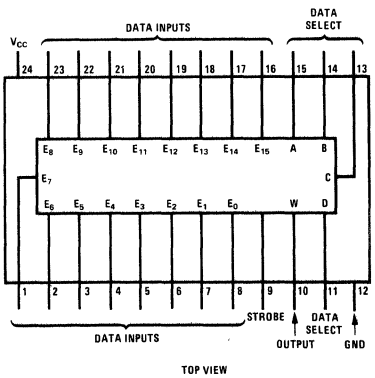
features

- Typical propagation delay 10 ns
- Typical power dissipation 225 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54150	4.5	5.5	V
DM74150	4 75	5.25	V
Temperature (T_A)			
DM54150	−55	+125	°C
DM74150	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V I_{OUT} = −800 μA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V I_{OUT} = +16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V V_{IN} = 5.5V			40 1.0	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current DM54150 DM74150	V_{CC} = Max, V_{OUT} = 0V (Note 3)	−20 −18		−55 −55	mA mA
Supply Current	V_{CC} = Max, V_{IN} = 4.5V			68	mA
Input Diode Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA T_A = 25°C			−1.5	V
t_{pd0} Propagation Delay to a Logical "0" from Data Select Inputs to Output	V_{CC} = 5.0V C_L = 50 pF T_A = 25°C R_L = 400Ω		22	33	ns
t_{pd1} Propagation Delay to a Logical "1" from Data Select Inputs to Output	V_{CC} = 5.0V T_A = 25°C		21	35	ns
t_{pd0} Propagation Delay to a Logical "0" from Strobe to Output	V_{CC} = 5.0V T_A = 25°C		21	30	ns
t_{pd1} Propagation Delay to a Logical "1" from Strobe to Output	V_{CC} = 5 0V T_A = 25°C		15.5	24	ns
t_{pd0} Propagation Delay to a Logical "0" from Data Inputs to Output	V_{CC} = 5.0V T_A = 25°C		8.5	14	ns
t_{pd1} Propagation Delay to a Logical "1" from Data Inputs to Output	V_{CC} = 5.0V T_A = 25°C		13	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54150 and across the 0°C to 70°C range for the DM74150. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

truth table

INPUTS																			OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

Series 54/74

DM54151/DM74151 (SN54151/SN74151)
8-channel digital multiplexer

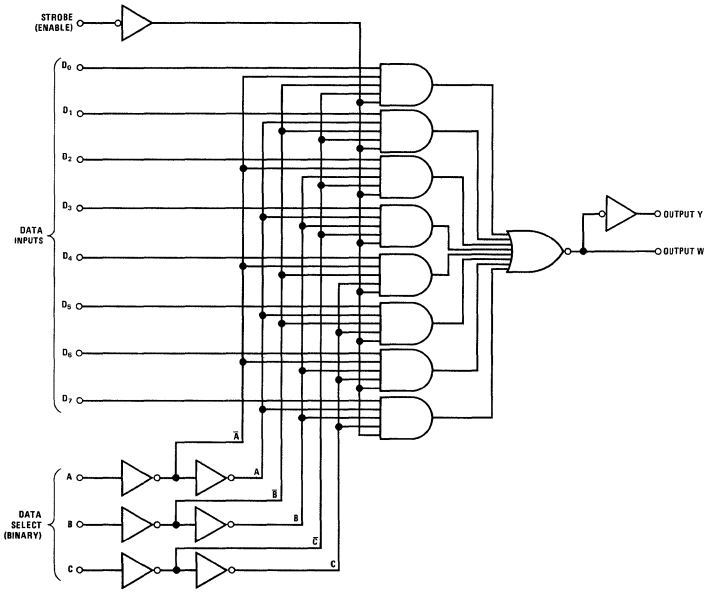
general description

The DM54151/DM74151 multiplexes digital signals from eight lines to one line. Two outputs provide either true or complement information. Three select lines determine which of the eight input lines are routed to the output. A strobe input is provided which when taken to the logical "1" state overrides all other inputs and places the outputs in a defined state.

features

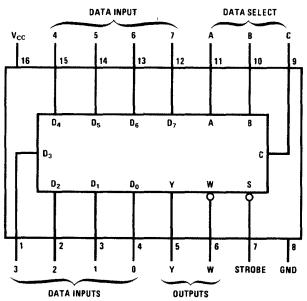
- Performs parallel-to-serial conversion
- Strobe override
- 15 ns typical propagation delay
- 135 mW typical power dissipation

logic diagram



connection diagram

Dual-In-Line and Flat Package



truth table

INPUTS											OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM54151	−55°C to +125°C
	DM74151	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54151	V_{CC} = 4.5V		2			V
	DM74151	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM54151	V_{CC} = 4.5V				0.8	V
	DM74151	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM54151	V_{CC} = 4.5V	I_O = −800 μA	2.4			V
	DM74151	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM54151	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM74151	V_{CC} = 4.75V					
Logical "1" Input Current	DM54151	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM74151	V_{CC} = 5.25V					
	DM54151	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM74151	V_{CC} = 5.25V					
Logical "0" Input Current	DM54151	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM74151	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM54151	V_{CC} = 5.5V		−20		−55	mA
	DM74151	V_{CC} = 5.25V		−18		−55	
Supply Current	DM54151	V_{CC} = 5.5V			27	48	mA
	DM74151	V_{CC} = 5.25V					
Input Clamp Voltage	DM54151	V_{CC} = 4.5V	T_A = 25°C, I_{IN} = −12 mA			−1.5	V
	DM74151	V_{CC} = 4.75V					
Propagation Delay to a Logical "0" to W, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	From Data Input		10	14	ns
			From Data Select		16	33	ns
			From Strobe (DM54151)		19	30	ns
Propagation Delay to a Logical "0" to Y, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	From Data Input		18	24	ns
			From Data Select		23	30	ns
			From Strobe (DM54151)		19	30	ns
Propagation Delay to a Logical "1" to W, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	From Data Input		11	20	ns
			From Data Select		16	35	ns
			From Strobe (DM54151)		11	24	ns
Propagation Delay to a Logical "1" to Y, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	From Data Input		17	29	ns
			From Data Select		23	52	ns
			From Strobe (DM54151)		25	52	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54151 and across the 0°C to 70°C range for the DM74151. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM54153/DM74153(SN54153/SN74153) dual 4:1 multiplexer

general description

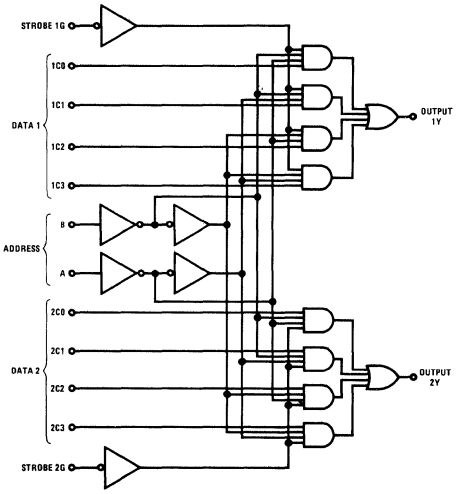
The DM54153/DM74153 is a dual four-line to one-line multiplexer. The device acts as a double-pole four-throw switch. Two SELECT lines determine which of the four inputs is chosen; however the same input of both four-line sections will be selected.

features

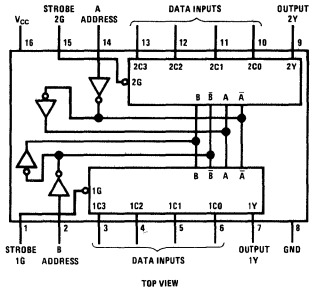
- Input diode clamps
- Propagation delay 20 ns typical
- Power dissipation 170 mW typical
- Series 54/74 compatible.

The DM54153 is characterized for operation over the full military temperature range of −55°C to +125°C; the DM74153 is characterized for operation from 0°C to 70°C.

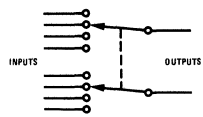
logic and connection diagrams



Dual-In-Line and Flat Package



Analogous to DP4T Switch



truth table

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

X = DON'T CARE

absolute maximum ratings (Note 1)

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DM54153	−55°C to +125°C
DM74153	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−1.5	V
Logical "1" Input Voltage	DM54153	V_{CC} = 4.5V		2.0			V
	DM74153	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM54153	V_{CC} = 4.5V				0.8	V
	DM74153	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM54153	V_{CC} = 4.5V	I_{OUT} = −800 μA	2.4	3.2		V
	DM74153	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM54153	V_{CC} = 4.5V	I_{OUT} = 16 mA		0.2	0.4	V
	DM74153	V_{CC} = 4.75V					
Logical "1" Input Current	DM54153	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM74153	V_{CC} = 5.25V					
			V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	DM54153	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM74153	V_{CC} = 5.25V					
Short-Circuit Output Current (Note 3)	DM54153	V_{CC} = 5.5V	V_{OUT} = 0V	−20		−55	mA
	DM74153	V_{CC} = 5.25V		−18		−57	
Supply Current	DM54153	V_{CC} = 5.5V	All inputs at GND		34	52	mA
	DM74153	V_{CC} = 5.25V			34	60	
Propagation Delay from Data to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF			15	23	ns
t_{pd0}					12	18	ns
Propagation Delay from Address to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF			20	34	ns
t_{pd0}					20	34	ns
Propagation Delay from Stobe to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF			19	30	ns
t_{pd0}					17	23	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54153 and across the 0°C to 70°C range for the DM74153 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM54154/DM74154 (SN54154/SN74154) 4-line to 16-line decoder/demultiplexer

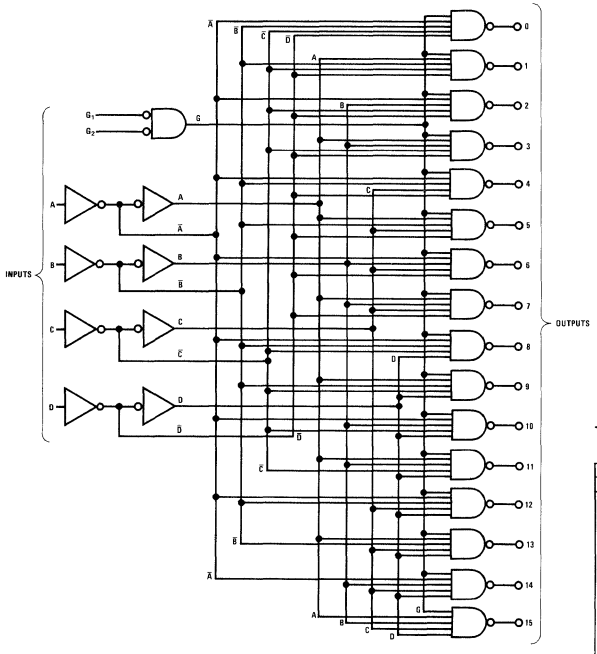
general description

The DM54154/DM74154 is a TTL monolithic 4-line-to-16-line decoder which allows decoding of a 4 bit binary coded input into one of 16 separate outputs The device is provided with two strobe lines, both of which have to be in the low state in order to perform the decoding function, if either of the strobes is high, all 16 outputs will remain high The device can be used as a demultiplexer by passing information from one of the strobes (the other being low) to an output selected by the 4 line input address

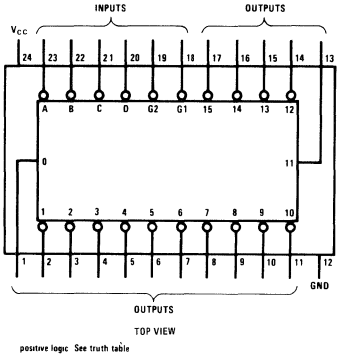
features

- All inputs contain clamp diodes
- Unit performs as a one line to 16 line demultiplexer
- Unit performs as a decoder of a 4 bit binary input to 1 of 16 outputs
- Typical propagation delay is 20 ns from inputs and 17 ns from strobe

logic and connection diagrams



Dual-In-Line and Flat Package



positive logic See truth table

truth table

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

absolute maximum ratings

V_{CC}	7.0V
Input Voltage	5 5V
Operating Temperature Range	
DM54154	−55°C to +125°C
DM74154	0°C to 75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

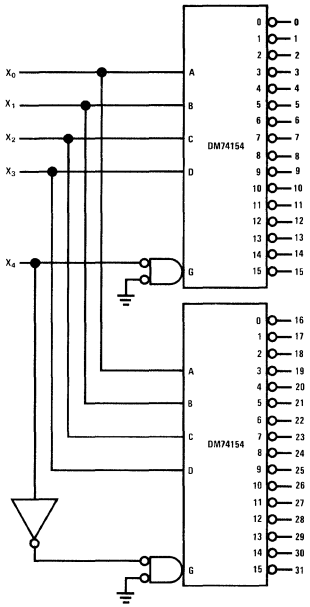
electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM54154	V_{CC} = 4 5V	2.0			V
	DM74154	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM54154	V_{CC} = 4.5V			0 8	V
	DM74154	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM54154	V_{CC} = 4.5V	2.4	3.4		V
	DM74154	V_{CC} = 4.75V, I_{OUT} = −800 μA				
Logical "0" Output Voltage	DM54154	V_{CC} = 4.5V		0.25	0 4	V
	DM74154	V_{CC} = 4.75V, I_{OUT} = 16 mA				
Logical "1" Input Current	DM54154	V_{CC} = 5.5V			40	μA
	DM74154	V_{CC} = 5 25V, V_{IN} = 2.4V				
Logical "1" Input Current	DM54154	V_{CC} = 5 5V			1	mA
	DM74154	V_{CC} = 5.25V, V_{IN} = 5.5V				
Logical "0" Input Current	DM54154	V_{CC} = 5.5V			−1.6	mA
	DM74154	V_{CC} = 5.25V, V_{IN} = 0.4V				
Short Circuit Current	DM54154	V_{CC} = 5.5V	−20	−30	−55	mA
	DM74154	V_{CC} = 5.25V	−18		−57	mA
Supply Current	DM54154	V_{CC} = 5.5V		34	49	mA
	DM74154	V_{CC} = 5 25V		34	56	
Propagation Delay Time to Logical "1" from A,B,C or D		V_{CC} = 5 0V, C_L = 15 pF, R_L = 400Ω		18	36	ns
Propagation Delay Time to Logical "0" from A,B,C or D		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		21	33	ns
Propagation Delay Time to Logical "1" from Strobe		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		17	30	ns
Propagation Delay Time to Logical "0" from Strobe		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		18	27	ns

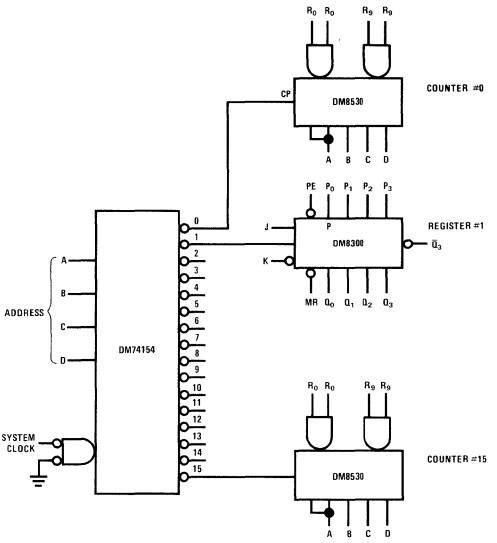
Note 1: Min/Max limits apply across the guaranteed temperature range unless otherwise specified. All typicals are given for V_{CC} = 5 0V and T_A = 25°C Min/Max apply to absolute values

typical applications

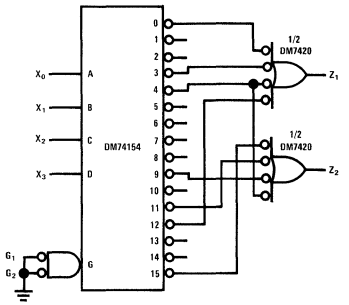
DM74154 Expanded to Perform
1 Out of 32 Decode Function



Demultiplexing System Clock



DM74154 Used as a Minterm
Generator



$Z_1 = \bar{X}_0\bar{X}_1\bar{X}_2\bar{X}_3 + X_0X_1\bar{X}_2\bar{X}_3 + \bar{X}_0\bar{X}_1X_2\bar{X}_3 + \bar{X}_0X_1X_2X_3$

$Z_2 = \bar{X}_0\bar{X}_1X_2\bar{X}_3 + X_0\bar{X}_1\bar{X}_2X_3 + X_0X_1\bar{X}_2X_3 + X_0X_1X_2X_3$

Series 54/74

DM54155/DM74155(SN54155/SN74155)
DM54156/DM74156(SN54156/SN74156)
dual 2:4 demultiplexers

general description

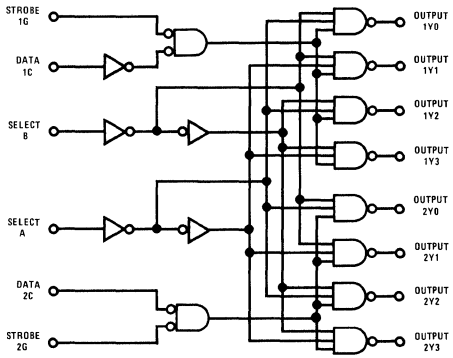
The DM54155/DM74155 and DM54156/DM74156 are monolithic transistor-transistor-logic (TTL) circuits featuring dual 1 line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8 line decoder or 1-to-8-line demultiplexer without external gating. See the truth tables for more details.

The DM54155/DM74155 has normal TTL "totem-pole" outputs. The DM54156/DM74156 has open collector outputs, but is otherwise identical to the DM54155/DM74155.

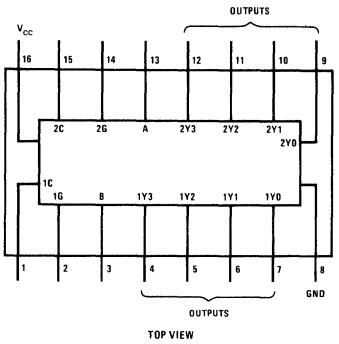
features

- 125 mW typical power dissipation
- 17 ns typical propagation delay for the DM54155/DM74155, 18 ns for the DM54156/DM74156
- Pin compatible with SN54155/SN74155 and SN54156/SN74156

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

truth tables

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together

‡G = inputs 1G and 2G connected together

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5.5V
Operating Temperature Range	DM54155,DM54156	−55°C to +125°C
	DM74155,DM74156	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54155,DM54156	V_{CC} = 4 5V		2 0			V
	DM74155,DM74156	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM54155,DM54156	V_{CC} = 4 5V				0 8	V
	DM74155,DM74156	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM54155	V_{CC} = 4 5V	I_{OUT} = −800 μA	2 4			V
	DM74155	V_{CC} = 4 75V					
Logical "1" Output Current	DM54156	V_{CC} = 5 5V	V_{OUT} = 5 5V			250	μA
	DM74156	V_{CC} = 5 25V					
Logical "0" Output Voltage	DM54155,DM54156	V_{CC} = 4 5V	I_{OUT} = 16 mA			0 4	V
	DM74155,DM74156	V_{CC} = 4 75V					
Logical "1" Input Current	DM54155,DM54156	V_{CC} = 5 5V	V_{IN} = 2 4V			40	μA
	DM74155,DM74156	V_{CC} = 5 25V					
	DM54155,DM54156	V_{CC} = 5 5V	V_{IN} = 5 5V			1	mA
	DM74155,DM74156	V_{CC} = 5 25V					
Logical "0" Input Current	DM54155,DM54156	V_{CC} = 5 5V	V_{IN} = 0 4V		−1 0	−1 6	mA
	DM74155,DM74156	V_{CC} = 5 25V					
Output Short Circuit Current (Note 3)	DM54155,DM54156	V_{CC} = 5 5V	V_{OUT} = 0V	−20			
	DM74155,DM74156	V_{CC} = 5 25V	V_{OUT} = 0V	−18	−32	−55	mA
Supply Current	DM54155,DM54156	V_{CC} = 5 5V			25	40	mA
	DM74155,DM74156	V_{CC} = 5 25V					
Input Clamp Voltage	DM54155,DM54156	V_{CC} = 5 5V	I_{IN} = −12 mA		−1 0	−1 5	V
	DM74155,DM74156	V_{CC} = 5 25V					

switching characteristics V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM INPUT	TO OUTPUT	LEVELS OF LOGIC	TEST CONDITIONS	DM54155/DM74155			DM54156/DM74156			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd1}	A, B, 2C, 1G, or 2G	Y	2	C_L = 50 pF, R_L = 400Ω		14	21		17	26	ns
t_{pd0}	A, B, 2C 1G, or 2G	Y	2			19	30		19	30	ns
t_{pd1}	A or B	Y	3			18	27		22	33	ns
t_{pd0}	A or B	Y	3			17	26		18	27	ns
t_{pd1}	1C	Y	3			18	27		21	32	ns
t_{pd0}	1C	Y	3			17	26		18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54155,DM54156 and across the 0°C to 70°C range for the DM74155,DM74156. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM54166/DM74166(SN54166/SN74166) 8-bit shift register

general description

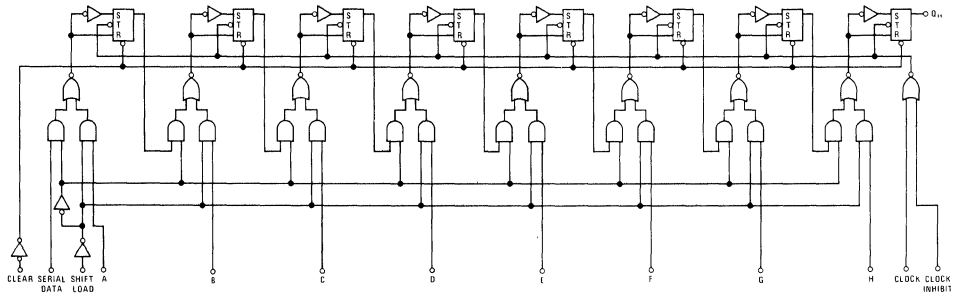
The DM54166/DM74166 is a parallel-in serial-in, serial-out eight-bit shift register containing a gated Clock, and overriding Clear. The parallel-in or serial-in modes are determined by the Shift/Load input. The truth table below indicates the operation.

During parallel loading shifting is prohibited. Clocking is accomplished on the rising edge of the clock pulse through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the inputs high inhibits clocking. To prevent false clocking the clock inhibit input should be taken high only when the clock input is high.

features

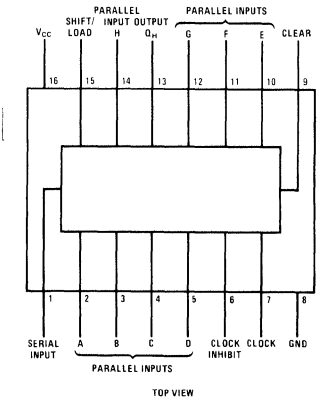
- Shift Frequency 35 MHz
- Power Dissipation 360 mW

logic diagram



connection diagram

Dual-In-Line and Flat Package



truth table

SHIFT LOAD	FUNCTION
1	Serial In Serial Out
0	Parallel In Serial Out

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54166	4 5	5 5	V
DM74166	4.75	5 25	V
Temperature (T_A)			
DM54166	−55	+125	°C
DM74166	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0 8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = −800 μA, V_{IL} = 0 8V	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = 16 mA, V_{IL} = 0 8V			0 4	V
Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2 4V			40	μA
Input Current at Max Input Voltage	V_{CC} = Max	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0 4V	−1 6			mA
Output Short Circuit Current (Note 3)	V_{CC} = Max		−20 −18		−57	mA
Supply Current	V_{CC} = Max				104 116	mA
Input Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA	−1 5			V
Propagation Delay to a Logical "0" from Clear to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			35	ns
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			30	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			26	ns
Maximum Clock Frequency	V_{CC} = 5 0V, T_A = 25°C		25	35		MHz
Minimum Clock and Clear Pulse Width	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	20			ns
Data Setup Time	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	20			ns
Mode Control Setup Time t_{SETUP}	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	30			ns
Hold Time at Any Input, t_{HOLD}	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	0			ns

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54166 and across the 0°C to +70°C range for the DM74166 All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54/74

DM54180/DM74180(SN54180/SN74180)
8-bit odd/even parity generator/checker

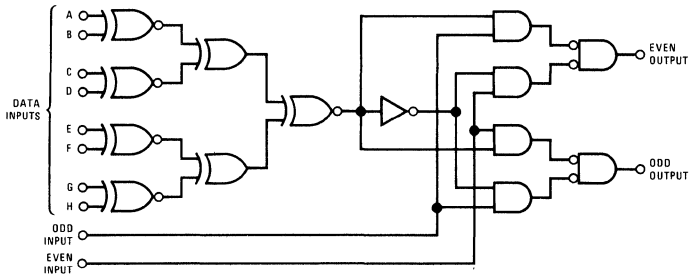
general description

The DM54180/DM74180 can both generate and check parity on eight bits of information Separate inputs are provided which perform a two-fold purpose. They can be used to gate the outputs to a known state regardless of the conditions on the data inputs; and in addition they can be used for convenient expansion of longer words.

features

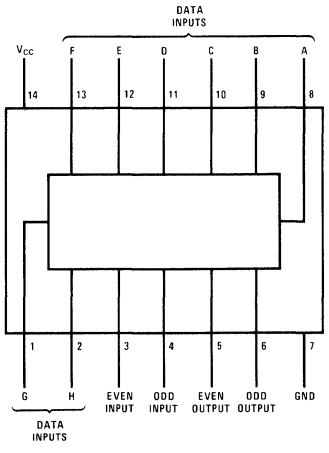
- Typical propagation delay 30 ns
- Typical power dissipation 180 mW
- Ease of expansion

logic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

NUMBER OF BIT "1"S AT DATA INPUTS	INPUTS		OUTPUTS	
	EVEN	ODD	EVEN	ODD
Even Number	1	0	1	0
Odd Number	1	0	0	1
Even Number	0	1	0	1
Odd Number	0	1	1	0
Even or Odd	1	1	0	0
Even or Odd	0	0	1	1

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54180	4 5	5 5	V
DM74180	4 75	5 25	V
Temperature (T_A)			
DM54180	−55	+125	°C
DM74180	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2 0			V
Logical "0" Input Voltage	V_{CC} = Min				0 8	V
Logical "1" Output Voltage	V_{CC} = Min	I_{OUT} = −800 μA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min	I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max					
At Each Data Inputs (A to H)		V_{IN} = 2 4V			40	μA
		V_{IN} = 5 5V			1 0	mA
At Even or Odd Input		V_{IN} = 2 4V			80	μA
		V_{IN} = 5 5V			1 0	mA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0 4V				
At Each Data Inputs (A to H)					−1 6	mA
At Even or Odd Input					−3 2	
Output Short Circuit Current (Note 3) DM54180	V_{CC} = Max	V_{OUT} = 0V	−20		−55	mA
DM74180			−18		−55	
Supply Current (Each Device) DM54180	V_{CC} = Max			36 6	49	mA
DM74180				36 6	56	
Input Diode Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA, T_A = 25°C			−1 5	V
Parameter: From Input / To Output						
t_{pd1} Data / Even	Odd Input Grounded	V_{CC} = 5 0V, T_A = 25°C		40	60	ns
t_{pd0} Data / Even				45	68	ns
t_{pd1} Data / Odd				32	48	ns
t_{pd0} Data / Odd				25	38	ns
t_{pd1} Data / Even	Even Input Grounded	C_L = 50 pF, F O = 10		32	48	ns
t_{pd0} Data / Even				25	38	ns
t_{pd1} Data / Odd				40	60	ns
t_{pd0} Data / Odd				45	68	ns
t_{pd1} Even or Odd / Even or Odd				13	20	ns
t_{pd0} Even or Odd / Even or Odd				8	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54180, and across the 0°C to 70°C range for the DM74180 All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54/74

DM54181/DM74181(SN54181/SN74181) arithmetic logic unit

general description

The DM54181/DM74181 (SN54181/SN74181) is a high-speed arithmetic logic unit (ALU)/function generator that has a complexity of 75 equivalent gates on a monolithic chip This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S_0, S_1, S_2, S_3) and include addition, subtraction, decrement, and straight transfer When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the device for fast, simultaneous carry generation with a group carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) for the four bits in the package.

High speed arithmetic operations can be performed for up to N-bit words when the DM54181/DM74181 is used in conjunction with the DM54182/DM74182.

For example, the typical addition time for the DM54181/DM74181 is 24 ns for four bits. When expanding to 16-bit addition with the DM54182/DM74182, only 13 ns further delay is added so that the total addition time is 37 ns, or 2.3 ns per bit. One DM54182/DM74182 is needed for every 16 bits (four DM54181/DM74181 circuits).

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry. The typical delay for the ripple carry is 12 ns for four bits. With a typical addition time of 24 ns for four bits, addition of two 8-bit words is accomplished typically in 36 ns when employing the ripple carry.

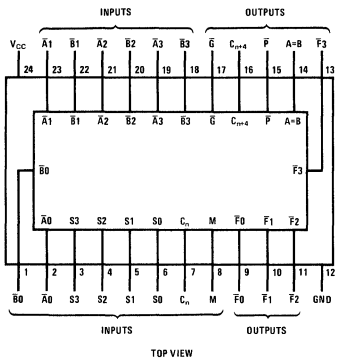
The DM54181 and DM54182 are characterized for operation over the full military temperature range of −55°C to 125°C; the DM74181 and DM74182 are characterized for operation from 0°C to 70°C.

features

- Full look-ahead for high-speed operations on long words
- Input clamping diodes minimize transmission-line effects
- Darlington outputs reduce turn-off time
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - plus ten other logical operations
- 24 ns typical add time for four bits
- 12 ns typical carry time for four bits

connection diagram and table

Dual-In-Line Package



TOP VIEW

DM54181/DM74181
PIN DESIGNATIONS

DESIGNATION	PIN NOS	FUNCTION	DESIGNATION	PIN NOS	FUNCTION
$\overline{A}_3,\overline{A}_2,\overline{A}_1,\overline{A}_0$	19, 21, 23, 2	Word A Inputs	A=B	14	Comparator Output
$\overline{B}_3,\overline{B}_2,\overline{B}_1,\overline{B}_0$	18, 20, 22 1	Word B Inputs	$\overline{P}$	15	Carry Propagate Output
$\overline{S}_3,\overline{S}_2,\overline{S}_1,\overline{S}_0$	3, 4, 5, 6	Function Select Inputs	C_{n+4}	16	Carry Output
C_n	7	Carry Input	$\overline{G}$	17	Carry Generate Output
M	8	Mode Control Input	V_{CC}	24	Supply Voltage
$\overline{F}_3,\overline{F}_2,\overline{F}_1,\overline{F}_0$	13, 11, 10, 9	Function Outputs	GND	12	GROUND

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5 5V
Operating Temperature Range	DM54181	−55°C to 125°C
	DM74181	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54181	V_{CC} = 4 5 V		2			V
	DM74181	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM54181	V_{CC} = 4 5V				0 8	V
	DM74181	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM54181	V_{CC} = 4 5V	V_{IH} = 2V, V_{IL} = 0 8V				
	DM74181	V_{CC} = 4 75V	I_{OUT} = −800 μA	2 4			V
Logical "0" Output Voltage	DM54181	V_{CC} = 4 5V	V_{IH} = 2V, V_{IL} = 0 8V				
	DM74181	V_{CC} = 4 75V	I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current (Mode Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V				40	μA
Logical "1" Input Current (Any $\overline{A}$ or $\overline{B}$ Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V	V_{IN} = 2 4V			120	μA
Logical "1" Input Current (Any S Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V				160	μA
Logical "1" Input Current (Carry Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V				200	μA
Logical "1" Input Current (Any Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Logical "0" Input Current (Mode Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V			−1	−1 6	mA
Logical "0" Input Current (Any $\overline{A}$ or $\overline{B}$ Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V			−3	−4 8	mA
Logical "0" Input Current (Any S Input)	DM54181	V_{CC} = 5 5V	V_{IN} = 0 4V				
	DM74181	V_{CC} = 5 25V			−3 9	−6 4	mA
Logical "0" Input Current (Carry Input)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V			−4 8	−8	mA
Output Short Circuit Current (Note 3)	DM54181	V_{CC} = 5 5V					
	DM74181	V_{CC} = 5 25V	V_{OUT} = 0V	−20 −18		−55 −57	mA
Supply Current − (GND All $\overline{B}_S$ & C_n, Other Inputs HIGH)	DM54181	V_{CC} = 5 5V			88	127	mA
	DM74181	V_{CC} = 5 25V			88	140	mA
GND All $\overline{A}_S$, $\overline{B}_S$ & C_n, Other Inputs HIGH	DM54181	V_{CC} = 5 5V			92	135	mA
	DM74181	V_{CC} = 5 25V			92	150	mA
Input Clamp Voltage	DM54181	V_{CC} = 4 5V					
	DM74181	V_{CC} = 4 75V	I_{IN} = −12 mA		−1	−1 5	V
Propagation Delay to a Logical "0" from C_n to C_{n+4}, t_{pd0}		V_{CC} = 5 0V T_A = 25°C	Diff Mode (Note 4)		14	19	ns
Propagation Delay to a Logical "1" from C_n to C_{n+4}, t_{pd1}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		9	18	ns
Propagation Delay to a Logical "0" from C_n to Any $\overline{F}$, t_{pd0}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		13	18	ns
Propagation Delay to a Logical "1" from C_n to Any $\overline{F}$, t_{pd1}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		11	19	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to $\overline{G}$, t_{pd0}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		15	25	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ or $\overline{B}$ to $\overline{G}$, t_{pd1}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		12	25	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to $\overline{P}$, t_{pd0}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		17	25	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ or $\overline{B}$ to $\overline{P}$, t_{pd1}		V_{CC} = 5 0V T_A = 25°C	Diff Mode		11	25	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to $\overline{F}$, t_{pd0}		V_{CC} = 5 0V T_A = 25 C	Diff Mode		14	34	ns

electrical characteristics (cont.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay to a Logical "1" from Any $\overline{A}$ or $\overline{B}$ to $\overline{F}$, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Diff Mode		14	48	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Logic Mode M = 4 5V (Note 5)		14	34	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ to $\overline{B}$ to Any $\overline{F}$, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Logic Mode M = 4 5V		16	48	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ to $\overline{B}$ to A=B, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Diff Mode		26	48	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to A=B, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Diff Mode		25	50	ns
Propagation Delay to a Logical "0" from C_n to C_{n+4}, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Sum Mode (Note 6)		14	19	ns
Propagation Delay to a Logical "1" from C_n to C_{n+4}, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Sum Mode		9	18	ns
Propagation Delay to a Logical "0" from C_n to Any $\overline{F}$, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Sum Mode		13	18	ns
Propagation Delay to a Logical "1" from C_n to Any $\overline{F}$, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Sum Mode		12	19	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to $\overline{G}$, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Sum Mode		16	19	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ or $\overline{B}$ to $\overline{G}$, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Sum Mode		13	19	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ or $\overline{B}$ to $\overline{P}$, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Sum Mode		17	25	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ or $\overline{B}$ to $\overline{P}$, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Sum Mode		12	19	ns
Propagation Delay to a Logical "0" from Any $\overline{A}$ to $\overline{B}$ to Any $\overline{F}$, t_{pd0}	V_{CC} = 5V, T_A = 25°C	Sum Mode		15	32	ns
Propagation Delay to a Logical "1" from Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$, t_{pd1}	V_{CC} = 5V, T_A = 25°C	Sum Mode		14	42	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54181 and across the 0°C to 70°C range for the DM74181 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

Note 4: Diff Mode $S_1 = S_2$ = 4 5V, $S_0 = S_3$ = M = 0V

Note 5: Logic Mode $S_1 = S_2$ = M = 4 5V, $S_0 = S_3$ = 0V

Note 6: Sum Mode $S_0 = S_3$ = 4 5V, $S_1 = S_2$ = M = 0V.

truth table

TABLE OF ARITHMETIC OPERATIONS

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOW LEVELS ACTIVE	HIGH LEVELS ACTIVE
L	L	L	L	F = A minus 1	F = A
L	L	L	H	F = AB minus 1	F = A+B
L	L	H	L	F = A$\overline{B}$ minus 1	F = A+$\overline{B}$
L	L	H	H	F = minus 1 (2's complement)	F = minus 1 (2's complement)
L	H	L	L	F = A plus [A+$\overline{B}$]	F = A plus A$\overline{B}$
L	H	L	H	F = AB plus [A+$\overline{B}$]	F = [A+B] plus A$\overline{B}$
L	H	H	L	F = A minus B minus 1	F = A minus B minus 1
L	H	H	H	F = A+$\overline{B}$	F = A$\overline{B}$ minus 1
H	L	L	L	F = A plus [A+B]	F = A plus AB
H	L	L	H	F = A plus B	F = A plus B
H	L	H	L	F = A$\overline{B}$ plus [A+B]	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = A+B	F = AB minus 1
H	H	L	L	F = A plus A†	F = A plus A†
H	H	L	H	F = AB plus A	F = [A+B] plus A
H	H	H	L	F = A$\overline{B}$ plus A	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

With mode control (M) and C_n low

†Each bit is shifted to the next more significant position

mode of operation

The DM54181/DM74181 has been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR, and OR functions.

The DM54181/DM74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs

The DM54181/DM74181 will accommodate active-high or active-low data if the input carry and output carry are reinterpreted.

Active-high data: No input carry, $C_n = 1$ (HIGH logic level)
No output carry, $C_{n+4} = 1$ (HIGH logic level)

Active-low data: No input carry, $C_n = 0$ (HIGH logic level)
No output carry, $C_{n+4} = 0$ (HIGH logic level)

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A–B–1 which requires an end-around or forced carry to provide A–B.

The DM54181/DM74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs ($\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$) so that when two words of equal magnitude are applied at the $\overline{A}$ and $\overline{B}$ inputs, it will assume a high-level state to indicate equality (A = B). The device should be in the subtract mode when performing this comparison. The A= B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

Active-high data: $C_{n+4} = 1$ (HIGH logic level) $A \geq B$
$C_{n+4} = 0$ (LOW logic level) $A < B$

Active-low data: $C_{n+4} = 1$ (LOW logic level) $A > B$
$C_{n+4} = 0$ (HIGH logic level) $A \leq B$

truth table (cont.)

TABLE OF LOGIC FUNCTIONS

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	NEGATIVE LOGIC	POSITIVE LOGIC
L	L	L	L	$F = \overline{A}$	$F = \overline{A}$
L	L	L	H	$F = \overline{AB}$	$F = \overline{A+B}$
L	L	H	L	$F = \overline{A}+B$	$F = \overline{AB}$
L	L	H	H	F = Logical 1	F = Logical 0
L	H	L	L	$F = \overline{A+B}$	$F = \overline{AB}$
L	H	L	H	$F = \overline{B}$	$F = \overline{B}$
L	H	H	L	$F = \overline{A \oplus B}$	$F = A \oplus B$
L	H	H	H	$F = A+\overline{B}$	$F = A\overline{B}$
H	L	L	L	$F = \overline{A}B$	$F = \overline{A}+B$
H	L	L	H	$F = A \oplus B$	$F = \overline{A \oplus B}$
H	L	H	L	F = B	F = B
H	L	H	H	F = A+B	F = AB
H	H	L	L	F = Logical 0	F = Logical 1
H	H	L	H	$F = A\overline{B}$	$F = A+\overline{B}$
H	H	H	L	F = AB	F = A+B
H	H	H	H	F = A	F = A

With mode control (M) HIGH C_n irrelevant
For positive logic logical 1 = HIGH Voltage
logical 0 = LOW Voltage
For negative logic logical 1 = LOW Voltage
logical 0 = HIGH Voltage

switching parameter measurement information

$\overline{\text{DIFF}}$ MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = 4.5V, S0 = S3 = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PHL} t_{PLH}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

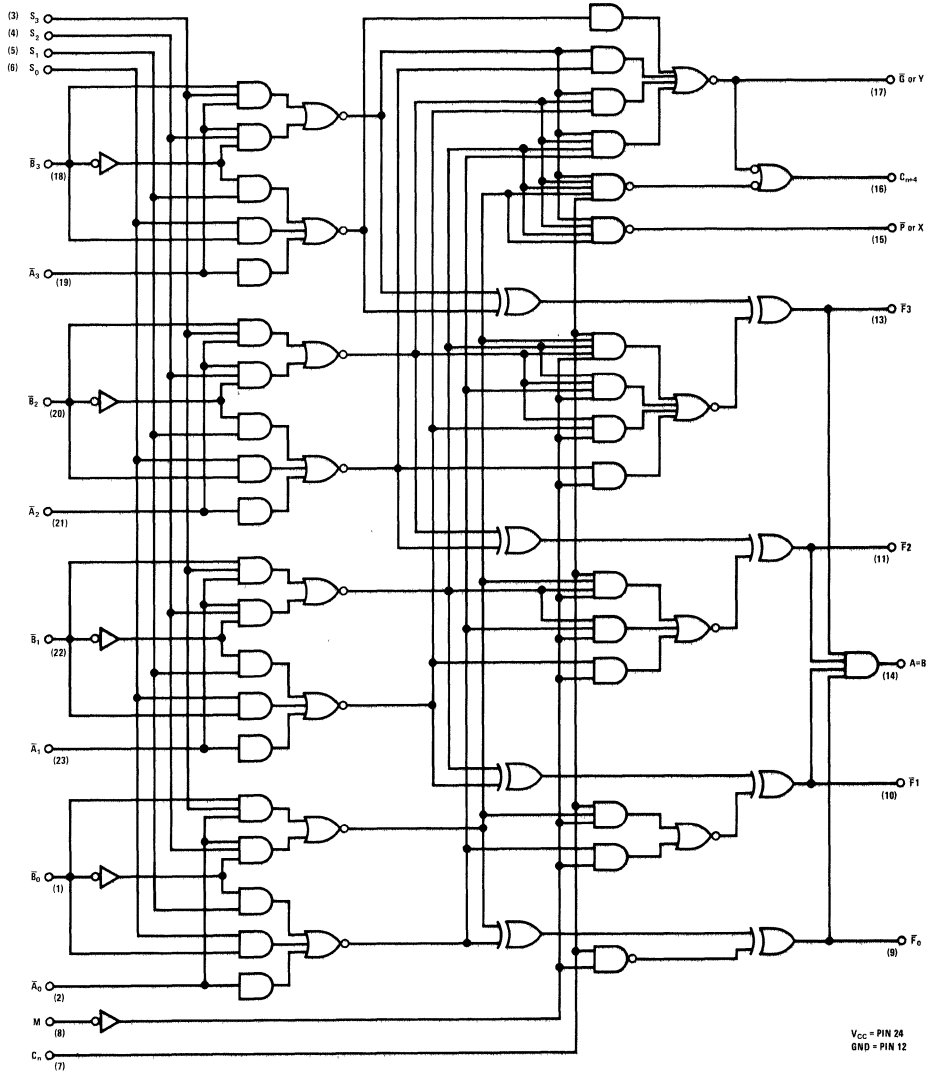
$\overline{\text{SUM}}$ MODE TEST TABLE
FUNCTION INPUTS S0 = S3 = 4.5V, S1 = S2 = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE
FUNCTION INPUTS S1 = S2 = M = 4.5V, S0 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

logic diagram



Series 54/74

DM54182/DM74182 (SN54182/SN74182) look-ahead carry generator

general description

The DM54182/DM74182 (SN54182/SN74182) is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 ns delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table.

High speed arithmetic operations can be performed for up to N-bit words when the DM54181/DM74181 is used in conjunction with the DM54182/DM74182.

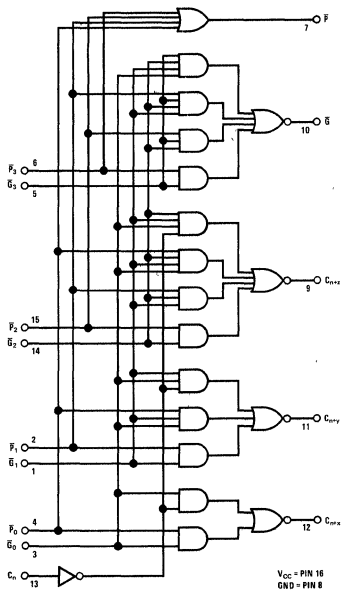
For example, the typical addition time for the DM54181/DM74181 is 24 ns for four bits. When expanding to 16-bit addition with the DM54182/DM74182, only 13 ns further delay is added so that the total addition time is 37 ns, or 2.3 ns per bit. One DM54182/DM74182 is needed for every 16 bits (four DM54181/DM74181 circuits).

Carry inputs and outputs of the DM54181/DM74181 are in their true form and the carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) are in negated form; therefore, the carry (input, outputs, generate, and propagate) functions of the look-ahead circuit are implemented in the compatible forms. Reinterpretations of carry functions at the DM54181/DM74181 are also applicable and compatible with the look-ahead package. Logic equations are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

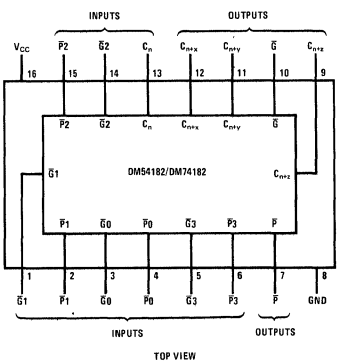
Inputs of the DM54182/DM74182 are diode-clamped to minimize transmission-line effects, and Darlington outputs are employed to improve turn-off times and reduce propagation delay times. Typically, the average carry time is 13 ns, and power dissipation is typically 180 mW or 11 mW per gate.

logic diagram



connection diagram and table

Dual-In-Line Package



TOP VIEW

DM54182/DM74182
PIN DESIGNATIONS

DESIGNATION	PIN NOS	FUNCTION	DESIGNATION	PIN NOS	FUNCTION
$\overline{G}_0,\overline{G}_1,\overline{G}_2,\overline{G}_3$	3, 1, 14, 5	Active LOW Carry Generate Inputs	$\overline{G}$	10	Active LOW Carry Generate Output
$\overline{P}_0,\overline{P}_1,\overline{P}_2,\overline{P}_3$	4, 2 15, 6	Active LOW Carry Propagate Inputs	$\overline{P}$	7	Active LOW Carry Propagate Output
C_n	13	Carry Input	V_{CC}	16	Supply Voltage
C_{n+x}, C_{n+y} C_{n+z}	12, 11 9	Carry Outputs	GND	8	GROUND

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5 5V
Operating Temperature Range	DM54182	−55°C to 125°C
	DM74182	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54182 / DM74182	V_{CC} = 4 5V / V_{CC} = 4 75V		2 0			V
Logical "0" Input Voltage	DM54182 / DM74182	V_{CC} = 4 5V / V_{CC} = 4 75V				0 8	V
Logical "1" Output Voltage	DM54182 / DM74182	V_{CC} = 4 5V / V_{CC} = 4.75V	I_O = −800 μA	2 4			V
Logical "0" Output Voltage	DM54182 / DM74182	V_{CC} = 4 5V / V_{CC} = 4 75V	I_O = 16 mA			0 4	V
Logical "1" Input Current (C_n Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			80	μA
Logical "1" Input Current ($\overline{P}_3$ Input)	DM54182 / DM74182	V_{CC} = 5.5V / V_{CC} = 5 25V	V_{IN} = 2 4V			120	μA
Logical "1" Input Current ($\overline{P}_2$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			160	μA
Logical "1" Input Current ($\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			200	μA
Logical "1" Input Current ($\overline{G}_0$ or $\overline{G}_2$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			360	μA
Logical "1" Input Current ($\overline{G}_1$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			400	μA
Logical "1" Input Current (Any Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Logical "0" Input Current (C_n Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 0 4V			−3 2	mA
Logical "0" Input Current ($\overline{P}_3$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V				−4 8	mA
Logical "0" Input Current ($\overline{P}_2$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V				−6 4	mA
Logical "0" Input Current ($\overline{P}_0$, $\overline{P}_1$ or $\overline{G}_3$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V				−8	mA
Logical "0" Input Current ($\overline{G}_0$ or $\overline{G}_2$ Inputs)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V				−14 4	mA
Logical "0" Input Current ($\overline{G}_1$ Input)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V				−16	mA
Output Short Circuit Current (Note 3)	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V		−40		−100	mA
Supply Current - All Outputs HIGH	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V			27		mA
Supply Current All Outputs LOW	DM54182 / DM74182	V_{CC} = 5 5V / V_{CC} = 5 25V			45 45	65 72	mA
Propagation Delay to a Logical "0" from Carry Input to Carry Output, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		14	22	ns
Propagation Delay to a Logical "0" from Carry Propagate Inputs (P_3 to Carry Generate ($\overline{G}$) & Carry Propagate ($\overline{P}$) Outputs, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		11	22	ns
Propagation Delay to a Logical "1" from Carry Input to Carry Outputs, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		11	17	ns
Propagation Delay to a Logical "1" from Carry Propagate Inputs (P_S) to Carry Generate ($\overline{G}$) & ($\overline{P}$) Propagate, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		10	17	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54182 and across the 0°C to +70°C range for the DM74182. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

Series 54/74

DM54184/DM74184(SN54184/SN74184) BCD-to-binary converter
DM54185A/DM74185A(SN54185A/SN74185A) binary-to-BCD converter

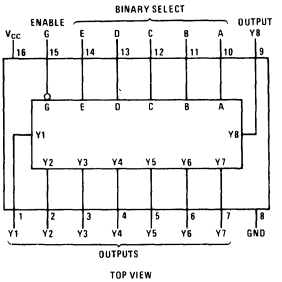
general description

Both of these converters are mask options of the DM5488/DM7488 256-bit Read-Only Memories. In normal operation the least significant bit bypasses the converter since in all cases the binary and BCD LSB's are the same. Thus each device performs a 6-bit conversion.

When the enable input is taken to the logic "1" level all outputs go high. In addition, the unused states of the DM54184/DM74184 and the unused outputs of the DM54185A/DM74185A are programmed to be logical "1"'s.

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth tables

DM54184/DM74184
BCD-to-Binary Converter

BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	BINARY SELECT					ENABLE					
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
24-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Note A: Input conditions other than those shown produce high at outputs Y1 through Y5

Note B: Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion

DM54185A/DM74185A
Binary-to-BCD Converter

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2-3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6-7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10-11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12-13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14-15	L	L	H	H	H	L	H	H	L	L	L	L	H	L
16-17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18-19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20-21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22-23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24-25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26-27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28-29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30-31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32-33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34-35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36-37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38-39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40-41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42-43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44-45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46-47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48-49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50-51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52-53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54-55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56-57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58-59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60-61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62-63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54184, DM54185A	4 5	5.5	V
DM74184, DM74185A	4.75	5.25	V
Temperature (T_A)			
DM54184, DM54185A	−55	+125	°C
DM74184, DM74185A	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Current	V_{CC} = Max, V_O = 5.5V			100	μA
Logical "0" Output Voltage	V_{CC} = Min, I_O = 12 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_I = 2 4V			40	μA
	V_{CC} = Max, V_I = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_I = 0 4V			−1.6	mA
Supply Current	V_{CC} = Max		50	80	mA
Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA			−1.5	V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, C_L = 15 pF		32	50	ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, C_L = 15 pF		34	50	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF		28	50	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF		27	50	ns

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54184, DM54185A and across the 0°C to 70°C range for the DM74184, DM74185A All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Series 54/74

DM54187/DM74187 (SN54187/SN74187)
1024-bit read only memory

general description

The DM54187/DM74187 is a custom-programmed read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; and when one is taken to the logical "1" state, it will cause all four outputs to go to the logical "1" state.

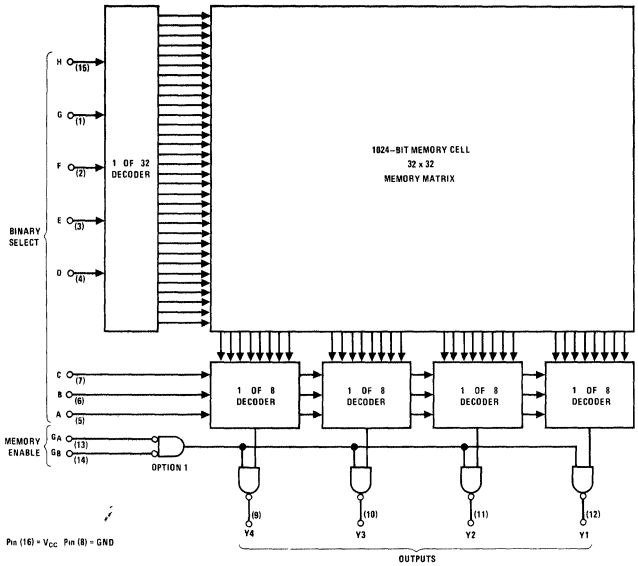
features

- 36 ns typical delay from address to output
- 20 ns typical delay from enable to output
- Open collector outputs for expansion

applications

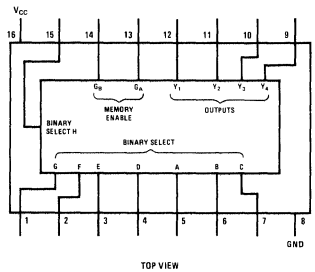
- Microprogramming
- Code conversions
- Look-up tables
- Use for any memory where content is fixed

logic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM54187	−55°C to +125°C
DM74187	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MAX	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54187 / DM74187	V_{CC} = 4.5V / V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM54187 / DM74187	V_{CC} = 4.5V / V_{CC} = 4.75V				0.8	V
Logical "1" Output Current	DM54187 / DM74187	V_{CC} = 5.5V / V_{CC} = 5.25V	V_O = 5.5V			40	μA
Logical "0" Output Voltage	DM54187 / DM74187	V_{CC} = 4.5V / V_{CC} = 4.75V	I_O = 16 mA			0.4	V
Logical "1" Input Current	DM54187 / DM74187	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
Logical "0" Input Current	DM54187 / DM74187	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
	DM54187 / DM74187	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 0.4V			−1.0	mA
Supply Current (each device)	DM54187 / DM74187	V_{CC} = 5.5V / V_{CC} = 5.25V	All Inputs at GND.		75	110	mA
Input Clamp Voltage	DM54187 / DM74187	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		20	30	ns
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		37	60	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		20	30	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		36	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54187 and across the 0°C to 70°C range for the DM74187. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ordering instructions

Programming instructions for the DM54187 or DM74187 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

supplementary ordering data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

data card format

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H", "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "DM"
62-66	Punch the National Semiconductor part number 54187 or 74187.
67-70	Blank

Series 54/74

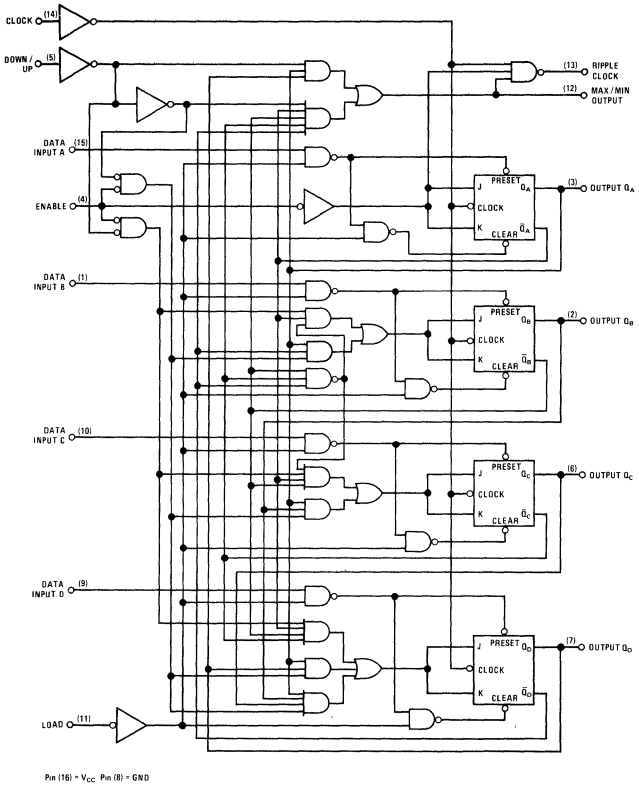
DM54190/DM74190(SN54190/SN74190) up/down decade counter

general description

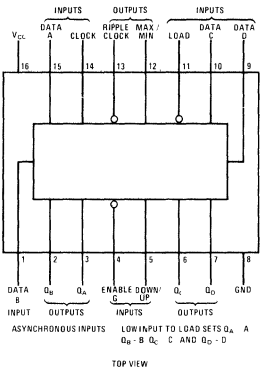
The DM54190/DM74190 is a four-bit up/down decade counter capable of being preset to any number from 0 through 9. A single Clock line is provided and depending upon the logic level on the down/up control, proper direction of counting is achieved. The flip flops are triggered on the positive-going transition of the clock providing that the Enable input is low. A logical 1 at the Enable input inhibits counting. Level changes at the Enable input should be made only when the Clock input is high. Information can be asynchronously entered by putting the desired logic levels on the Data inputs and then taking the Load input low. This may be done independent of the state of the clock.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

logic and connection diagrams



Dual-In-Line and Flat Package



operating modes

DOWN/UP	ENABLE	LOAD	MODE
X	X	L	Parallel Load
X	H	H	No Change
L	L	H	Count Up
H	L	H	Count Down

H = high level, L = low level, X = irrelevant

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54190	4 5	5.5	V
DM74190	4.75	5.25	V
Temperature (T_A)			
DM54190	−55	+125	°C
DM74190	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = −800 μA, V_{IL} = 0 8V	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = 16 mA, V_{IL} = 0 8V			0 4	V
Logical "1" Input Current at Maximum Input Voltage	V_{CC} = Max	V_{IN} = 5 5V			1	mA
Logical "1" Input Current at Any Input Except Enable	V_{CC} = Max	V_{IN} = 2 4V			40	μA
Logical "1" Input Current at Enable	V_{CC} = Max	V_{IN} = 2 4V			120	μA
Logical "0" Input Current at Any Input Except Enable	V_{CC} = Max	V_{IN} = 0 4V			−1 6	mA
Logical "0" Input Current at Enable	V_{CC} = Max	V_{IN} = 0 4V			−4 8	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	V_{OUT} = 0V	−20 −18		−65	mA
Supply Current (each device)	V_{CC} = Max			66	105	mA
Input Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Load to Outputs, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		24	50	ns
Propagation Delay to a Logical "0" from Data to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		26	50	ns
Propagation Delay to a Logical "0" from Clock to Ripple Clock, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		16	24	ns
Propagation Delay to a Logical "0" from Clock to Outputs, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		22	36	ns
Propagation Delay to a Logical "0" from Clock to Max/Min, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		21	52	ns
Propagation Delay to a Logical "0" from Down/Up to Ripple Clock, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		21	45	ns
Propagation Delay to a Logical "0" from Down/Up to Max/Min, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		16	33	ns
Propagation Delay to a Logical "1" from Load to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		22	33	ns
Propagation Delay to a Logical "1" from Data to Outputs, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		12	22	ns
Propagation Delay to a Logical "1" from Clock to Ripple Clock, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		14	20	ns
Propagation Delay to a Logical "1" from Clock to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		19	24	ns
Propagation Delay to a Logical "1" from Clock to Max/Min, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		23	42	ns
Propagation Delay to a Lgoical "1" from Down/Up to Ripple Clock, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		22	45	ns
Propagation Delay to a Logical "1" from Down/Up to Max/Min, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		14	33	ns
Maximum Clock Frequency f_{MAX}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		20	25	MHz
Input Clock Frequency f_{CLOCK}				0	20	MHz
Width of Input Pulse $t_{W(CLOCK)}$				25		ns
Width of Load Input Pulse $t_{W(LOAD)}$				35		ns
Data Setup Time, t_{SETUP}				20		ns
Data Hold Time, t_{HOLD}				0		ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54190 and across the 0°C to 70°C range for the DM74190 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3 Only one output at a time should be shorted

Series 54/74

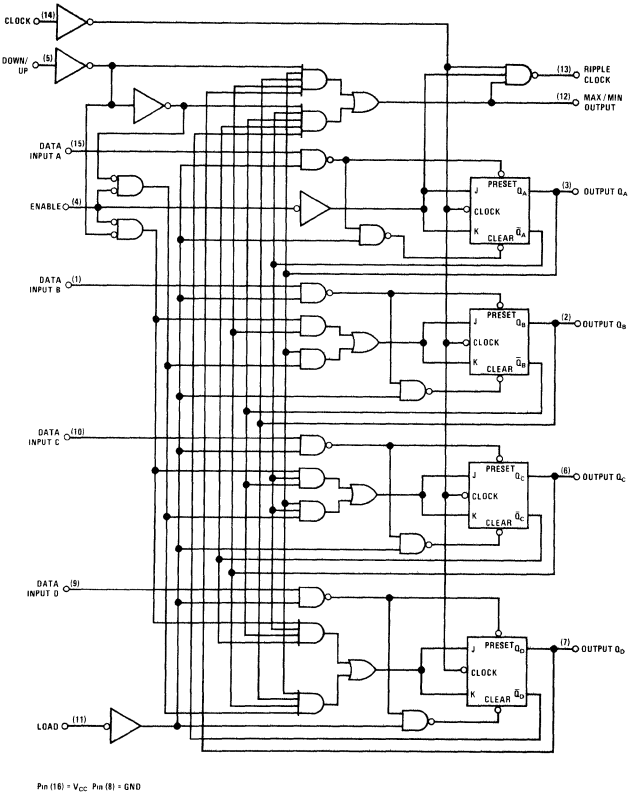
DM54191/DM74191(SN54191/SN74191) up/down binary counter

general description

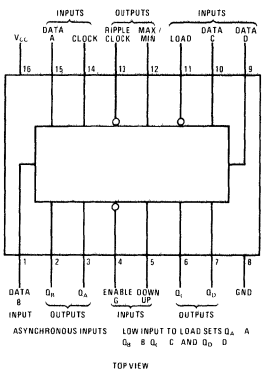
The DM54191/DM74191 is an up/down binary counter capable of being preset to any number from 0 through 15. A single Clock line is provided and depending upon the logic level on the down/up control, proper direction of counting is achieved. The flip flops are triggered on the positive-going transition of the clock providing that the Enable input is low. A logical 1 at the Enable input inhibits counting. Level changes at the Enable input should be made only when the Clock input is high. Information can be asynchronously entered by putting the desired logic levels on the Data inputs and then taking the Load input low. This may be done independent of the state of the clock.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

logic and connection diagrams



Dual-In-Line and Flat Package



operating modes

DOWN/UP	ENABLE	LOAD	MODE
X	X	L	Parallel Load
X	H	H	No Change
L	L	H	Count Up
H	L	H	Count Down

H = high level, L = low level, X = irrelevant

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54191	4.5	5.5	V
DM74191	4.75	5.25	V
Temperature (T_A)			
DM54191	−55	+125	°C
DM74191	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = −800 μA, V_{IL} = 0.8V	2.4			V
Logical "0" Output Voltage	V_{CC} = 2V, V_{IH} = 2V	I_{OUT} = 16 mA, V_{IL} = 0.8V			0.4	V
Logical "1" Input Current at Maximum Input Voltage	V_{CC} = Max	V_{IN} = 5.5V			1	mA
Logical "1" Input Current at Any Input Except Enable	V_{CC} = Max	V_{IN} = 2.4V			40	μA
Logical "1" Input Current at Enable	V_{CC} = Max	V_{IN} = 2.4V			120	μA
Logical "0" Input Current at Any Input Except Enable	V_{CC} = Max	V_{IN} = 0.4V			−1.6	mA
Logical "0" Input Current at Enable	V_{CC} = Max	V_{IN} = 0.4V			−4.8	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	V_{OUT} = 0V	−20 −18		−65	mA
Supply Current (each device)	V_{CC} = Max				105	mA
Input Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Load to Outputs, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		24	50	ns
Propagation Delay to a Logical "0" from Data to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		26	50	ns
Propagation Delay to a Logical "0" from Clock to Ripple Clock, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		16	24	ns
Propagation Delay to a Logical "0" from Clock to Outputs, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		22	36	ns
Propagation Delay to a Logical "0" from Clock to Max/Min, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		21	52	ns
Propagation Delay to a Logical "0" from Down/Up to Ripple Clock, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		21	45	ns
Propagation Delay to a Logical "0" from Down/Up to Max/Min, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		16	33	ns
Propagation Delay to a Logical "1" from Load to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		22	33	ns
Propagation Delay to a Logical "1" from Data to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		12	22	ns
Propagation Delay to a Logical "1" from Clock to Ripple Clock, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		14	20	ns
Propagation Delay to a Logical "1" from Clock to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		19	24	ns
Propagation Delay to a Logical "1" from Clock to Max/Min, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		23	42	ns
Propagation Delay to a Logical "1" from Down/Up to Ripple Clock, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		22	45	ns
Propagation Delay to a Logical "1" from Down/Up to Max/Min, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω		14	33	ns
Maximum Clock Frequency f_{MAX}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω	20	25		MHz
Input Clock Frequency f_{CLOCK}			0		20	MHz
Width of Input Pulse $t_{W(CLOCK)}$			25			ns
Width of Load Input Pulse $t_{W(LOAD)}$			35			ns
Data Setup Time, t_{SETUP}			20			ns
Data Hold Time, t_{HOLD}			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54191 and across the 0°C to 70°C range for the DM74191. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM54198/DM74198(SN54198/SN74198) 8-bit shift register

general description

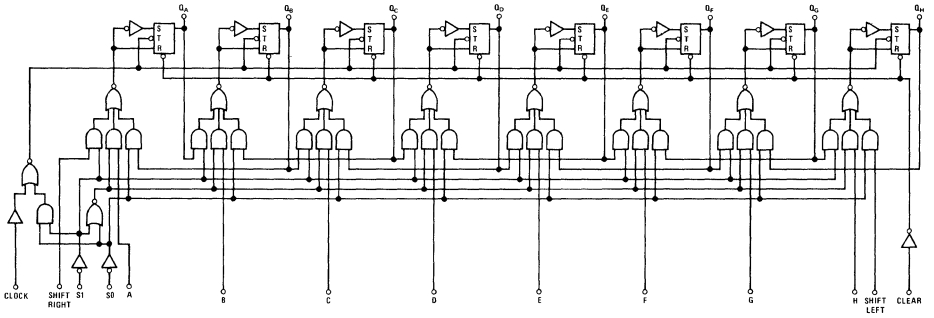
The DM54198/DM74198 is an eight-bit shift register capable of being operated in four modes: (1) Parallel-Load, (2) Shift-Right, (3) Shift-Left, (4) Clock Inhibit (do nothing).

With inputs S_0 and S_1 at logic "1" levels the data on the A through H inputs will be entered on the next clock pulse. Whether shifting left or right, clocking occurs on the rising edge of the clock pulse. During loading shifting is inhibited. Cascading is accomplished by connecting the Shift-Right and Shift-Left inputs to the outputs of Q_H of the preceeding register or Q_A of the following register respectively. Clocking is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the clock input is high.

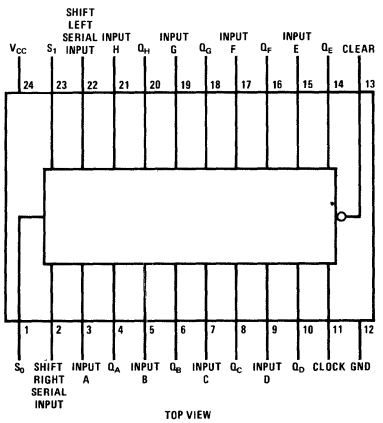
features

- Shift Frequency 35 MHz
- Power Dissipation 360 mW

logic and connection diagrams



Dual In-Line and Flat Package



truth table

INPUTS		MODE
S_1	S_0	
L	L	Inhibit Clock
L	H	Shift Right
H	L	Shift Left
H	H	Parallel Load

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54198	4 5	5.5	V
DM74198	4 75	5 25	V
Temperature (T_A)			
DM54198	−55	+125	°C
DM74198	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0 8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = −800 μA, V_{IL} = 0 8V	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = 16 mA, V_{IL} = 0 8V			0 4	V
Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2 4V			40	μA
Input Current at Maximum Input Voltage	V_{CC} = Max	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0 4V	−1 6			mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	V_O = 0V	−20 −18		−57	mA
Supply Current (each device)	V_{CC} = Max			72	104 116	mA
Input Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA	−1 5			V
Propagation Delay to a Logical "0" from Clear to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			35	ns
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			30	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			26	ns
Maximum Clock Frequency	V_{CC} = 5 0V, T_A = 25°C		25	35		MHz
Minimum Clock and Clear Pulse Width	V_{CC} = 5.0V	T_A = 25°C, C_L = 50 pF	20			ns
Data Setup Time	V_{CC} = 5.0V	T_A = 25°C, C_L = 50 pF	20			ns
Mode Control Setup Time t_{SETUP}	V_{CC} = 5.0V	T_A = 25°C, C_L = 50 pF	30			ns
Hold Time at Any Input, t_{HOLD}	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54198 and across the 0°C to +70°C range for the DM74198 All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

Series 54/74

DM54199/DM74199(SN54199/SN74199) 8-bit shift register

general description

The DM54199/DM74199 is an 8-bit shift register capable of being operated in three modes. (1) Parallel-Load, (2) Shift-Right, (3) Inhibit Clock.

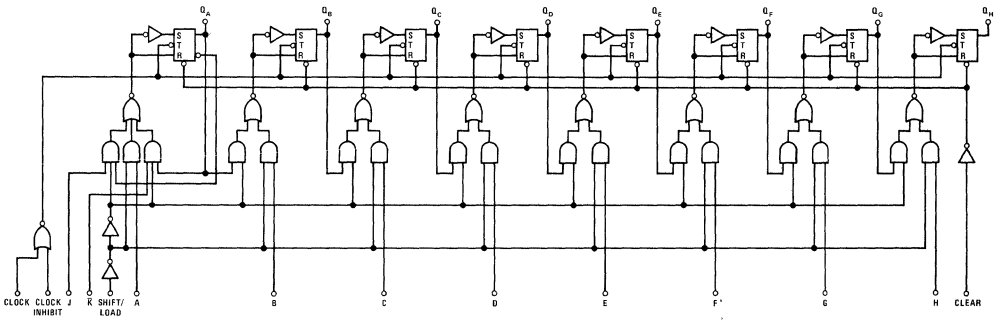
Parallel load is accomplished by applying the eight bits of data and taking the Shift/Load control input low when the clock input is not inhibited. Data appears as the output after the positive transition of the next clock pulse. During loading shifting is inhibited. Shifting is accomplished synchronously when Shift/Load is high and the clock input is not inhibited. Serial data is entered at the J-$\overline{K}$ inputs. In order to cascade devices, connect the Q_H output of one stage to the J-$\overline{K}$ inputs (tied together) of the following stage. Both Clock and Clock Inhibit are identical in function and may be used interchangeably to serve as clock or a clock inhibit inputs Holding either high inhibits clocking; but when one is held low, the other will clock the register. Therefore the clock inhibit input should be changed from low to high only while the clock input is high.

features

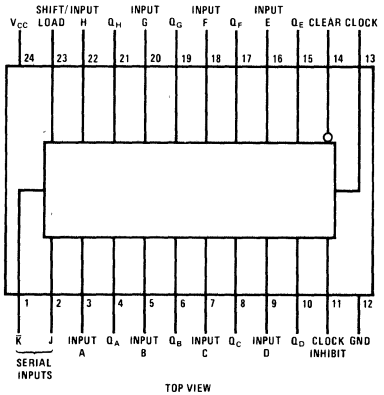
- Shift Frequency 35 MHz
- Power Dissipation 360 mW

1

logic and connection diagrams



Dual-In-Line and Flat Package



truth table

J-$\overline{K}$ INPUTS		
INPUTS at t_n		OUTPUT t_{n+1}
J	$\overline{K}$	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

H = high level, L = low level

NOTE A t_n = bit time before clock pulse

NOTE B. t_{n+1} = bit time after clock pulse

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54199	4 5	5 5	V
DM74199	4 75	5 25	V
Temperature (T_A)			
DM54199	−55	+125	°C
DM74199	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = −800 μA, V_{IL} = 0.8V	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OUT} = 16 mA, V_{IL} = 0 8V			0 4	V
Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2 4V			40	μA
Input Current at Maximum Input Voltage	V_{CC} = Max	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0.4V	−1 6			mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	V_{IN} = 0V	−20 −18		−57	mA
Supply Current (each device)	V_{CC} = Max			72	104 116	mA
Input Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA	−1 5			V
Propagation Delay to a Logical "0" from Clear to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			35	ns
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			30	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 400Ω			26	ns
Maximum Clock Frequency	V_{CC} = 5.0V, T_A = 25°C		25	35		MHz
Minimum Clock and Clear Pulse Width	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	20			ns
Data Setup Time	V_{CC} = 5 0V	T_A = 25°C, C_L = 50 pF	20			ns
Mode Control Setup Time t_{SETUP}	V_{CC} = 5.0V	T_A = 25°C, C_L = 50 pF	30			ns
Hold Time at Any Input, t_{HOLD}	V_{CC} = 5.0V	T_A = 25°C, C_L = 50 pF	0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54199 and across the 0°C to +70°C range for the DM74199. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

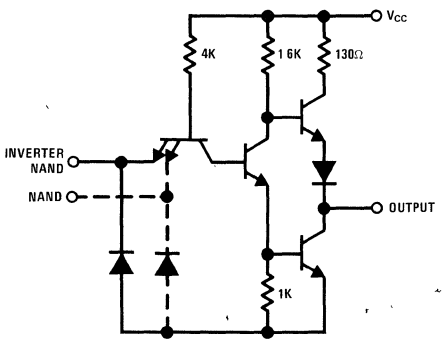
Series 54/74

DM7090/DM8090 quad inverter/dual 2-input NAND buffer

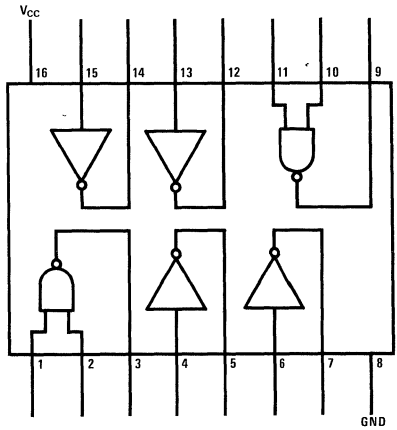
general description

The DM7090/DM8090 optimizes the flexibility of the 16-pin package by providing two 2-input NAND gates and four inverters in the same package. The electrical specifications are totally compatible with all Series 54/74 devices.

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7 0V
Input Voltage	5 5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7090	4.5	5 5	V
DM8090	4 75	5.25	V
Temperature (T_A)			
DM7090	−55	+125	°C
DM8090	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = −400 μA	2 4			V
Logical "1" Output Current					
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2 0V, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_{OUT} = 0 DM7090	−20		−55	mA
	V_{CC} = Max, V_{OUT} = 0 DM8090	−18			
Supply Current — Logical "1" (each device)	V_{CC} = Max, V_{IN} = 0			11	mA
Logical "0"	V_{CC} = Max, V_{IN} = 5 0V			31	mA
Input Clamp Voltage	V_{CC} = 5 0V, I_{IN} = −12 mA, T_A = 25°C		−1 0	−1 5	V
Propagation Delay to a Logical "0" from Inputs to Outputs, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		9	15	ns
Propagation Delay to a Logical "1" from Inputs to Outputs, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		13	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7090 and across the 0°C to 70°C range for the DM8090. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54/74

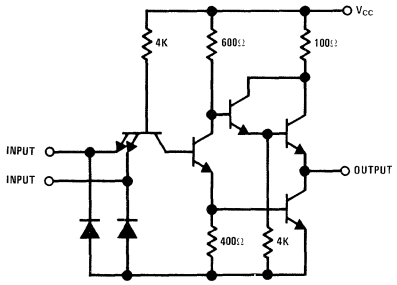
DM7091/DM8091 quad 2-input NAND buffer

general description

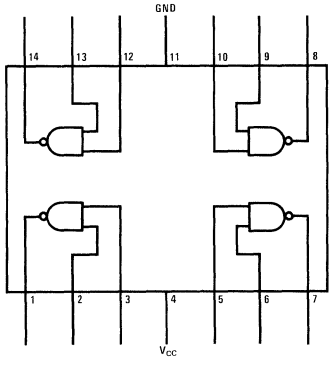
The DM7091/DM8091 provides four 2-input gates each with a fan-out of 30, in the same package.

The electrical specifications are totally compatible with all Series 54/74 devices.

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Supply Voltage	7 0V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7091	4 5	5 5	V
DM8091	4 75	5 25	V
Temperature (T_A)			
DM7091	−55	+125	°C
DM8091	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = −1 2 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2 0V, I_{OUT} = 48 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			40 1	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	−18		−70	mA
Supply Current — Logical "1"	V_{CC} = Max, V_{IN} = 0			15	mA
Logical "0"	V_{CC} = Max, V_{IN} = 5 0V			46	mA
Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1 0	−1 5	V
Propagation Delay to a Logical "0" from Any Input to Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		8	15	ns
Propagation Delay to a Logical "1" from Any Input to Output, t_{pd1}	V_{CC} = 5.0V T_A = 25°C		13	22	ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7091 and across the 0°C to 70°C range for the DM8091 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3 Only one output at a time should be shorted

Series 54/74

DM7092/DM8092 dual 5-input NAND gate

general description

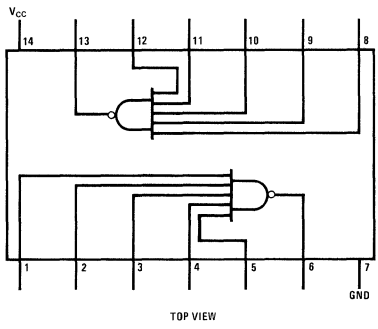
The DM7092/DM8092 is a dual 5-input NAND gate utilizing TTL (Transistor-Transistor Logic). The device fills a gap in the standard 54/74 series in that it replaces two single 8-input gates (with tied inputs) or an assembly of smaller gates. Also either of the two 5-input gates can be used as a smaller gate.

features

- Series 54/74 compatibility
- No longer necessitates use of SN5430/SN7430 (eight-input-gate) for the five-input function
- Specifications identical to standard SN54XX/SN74XX gate

logic and connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7092	−55°C to +125°C
DM8092	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7092	V_{CC} = 4.5V	2.0			V
	DM8092	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7092	V_{CC} = 4.5V			0.8	V
	DM8092	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7092	V_{CC} = 4.5V, I_{OUT} = −400 μA, V_{IN} = 0.8V	2.4			V
	DM8092	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM7092	V_{CC} = 4.5V, I_{OUT} = 16 mA, V_{IN} = 2.0V			0.4	V
	DM8092	V_{CC} = 4.75V				
Logical "1" Input Current	DM7092	V_{CC} = 5.5V, V_{IN} = 2.4V			40	μA
	DM8092	V_{CC} = 5.25V				
	DM7092	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8092	V_{CC} = 5.25V				
Logical "0" Input Current	DM7092	V_{CC} = 5.5V, V_{IN} = 0.4V			−1.6	mA
	DM8092	V_{CC} = 5.25V				
Output Short Circuit Current (Note 3)	DM7092	V_{CC} = 5.5V, V_{OUT} = 0V	−20		−55	mA
	DM8092	V_{CC} = 5.25V	−18			
Supply Current — Logical "1" (Each Device)	DM7092	V_{CC} = 5.5V, V_{IN} = 0V		1	1.8	mA
	DM8092	V_{CC} = 5.25V				
Logical "0"	DM7092	V_{CC} = 5.5V, V_{IN} = 5.0V		3	5.1	mA
	DM8092	V_{CC} = 5.25V				
Input Clamp Voltage		V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		8	15	ns
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		13	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7092 and across the 0°C to 70°C range for the DM8092. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM7093/DM8093 TRI-STATE® quad buffer
DM7094/DM8094 TRI-STATE quad buffer

general description

The DM7093/DM8093 and DM7094/DM8094 are quad 2-input buffers which accept normal TTL or DTL input levels and have outputs which provide either normal low-impedance TTL output characteristics or a high impedance state. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state. The other input simply passes the non-inverted data through the buffer. The DM7093/DM8093 and DM7094/DM8094 differ only in the activating logic state of the control input. The DM7093/DM8093 provides the high impedance state when a logical "1" is applied to the control input; the DM7094/DM8094 operates similarly with a logical "0".

features

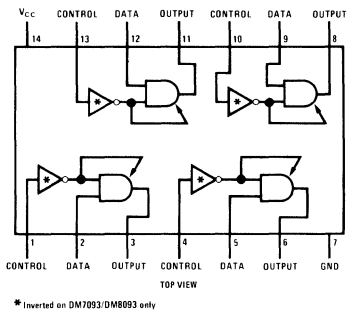
- Series 54/74 TTL and 930 DTL Compatible
- Same Pin Breakout as SN5400/SN7400 TTL and 946 DTL
- Up to 128 Buffers can be Connected to a Common Bus-Line
- 12 ns Propagation Delay
- High Capacitive Drive Capability
- Independent Control of each Buffer

This unique TRI-STATE concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If however on all but one of the connected devices both the upper and lower output transistors are turned off, then the one remaining device in the normal low impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7093/DM8093 and DM7094/DM8094.

(Continued on following pages)

logic and connection diagram

Dual-In-Line and Flat Package



*Inverted on DM7093/DM8093 only

truth tables

DM7093/DM8093

DATA	CONTROL	OUTPUT
1	0	1
0	0	0
X	1	Hi-Z

X = Irrelevant

DM7094/DM8094

DATA	CONTROL	OUTPUT
1	1	1
0	1	0
X	0	Hi-Z

X = Irrelevant

absolute maximum ratings

Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V	Operating Temperature Range	
Output Voltage	5.5V	DM7093, DM7094	−55°C to +125°C
Time that two bus-connected devices may be in opposite low impedance states simultaneously (5% duty cycle)	Indefinite	DM8093, DM8094	0°C to +70°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETERS		CONDITIONS			MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Input Clamp Voltage	DM7093/94	V_{CC} = 4.5V	T_A = 25°C, I_{IN} = −12 mA				−1.5	V
	DM8093/94	V_{CC} = 4.75V						
Logical "1" Input Voltage	DM7093/94	V_{CC} = 4.5V			2.0			V
	DM8093/94	V_{CC} = 4.75V						
Logical "0" Input Voltage	DM7093/94	V_{CC} = 4.5V					0.8	V
	DM8093/94	V_{CC} = 4.75V						
Logical "1" Input Current	DM7093/94	V_{CC} = 5.5V	V_{IN} = 2.4V				40	μA
	DM8093/94	V_{CC} = 5.25V						
Logical "1" Input Current	DM7093/94	V_{CC} = 5.5V	V_{IN} = 5.5V				1	mA
	DM8093/94	V_{CC} = 5.25V						
Logical "0" Input Current (Control Input Only)	DM7093/94	V_{CC} = 5.5V	V_{IN} = 0.4V				−1.6	mA
	DM8093/94	V_{CC} = 5.25V						
Logical "0" Input Current (Data Input Only)	DM7093/94	V_{CC} = 5.5V	V_{IN} = 0.4V	$V_{CONTROL}$ = 2.0V (DM7093/8093) 0.8V (DM7094/8094)			−40	μA
	DM8093/94	V_{CC} = 5.25V		$V_{CONTROL}$ = 0.8V (DM7093/8093) 2.0V (DM7094/8094)			−1.6	mA
Logical "1" Output Voltage	DM7093/94	V_{CC} = 4.5V	I_o = −2.0 mA		2.4			V
	DM8093/94	V_{CC} = 4.75V	I_o = −5.2 mA					
Logical "0" Output Voltage	DM7093/94	V_{CC} = 4.5	I_o = 16 mA				0.4	V
	DM8093/94	V_{CC} = 4.75						
Output Short Current (Note 2)	DM7093/94	V_{CC} = 5.5V	V_o = 0V		−30	−45	−70	mA
	DM8093/94	V_{CC} = 5.25V			−28	−45	−70	
Supply Current	DM7093	V_{CC} = 5.5V					54	mA
	DM8093	V_{CC} = 5.25V						
Supply Current	DM7094	V_{CC} = 5.5V					62	mA
	DM8094	V_{CC} = 5.25V						
Output Disable Current	DM7093/94	V_{CC} = 5.5V		V_o = 2.4V			40	μA
	DM8093/94	V_{CC} = 5.25V		V_o = 0.4V			−40	μA
V_{CC} Clamp		V_{CC} = 0V, I_o = 12 mA					1.5	V
Ground Clamp		V_{CC} = 0V, I_o = −12 mA					−1.5	V
t_{pd1}	DM7093/8093	V_{CC} = 5.0V				12	23	ns
	DM7094/8094	T_A = 25°C				12	23	ns
t_{pd0}	DM7093/8093	V_{CC} = 5.0V				12	18	ns
	DM7094/8094	T_A = 25°C				12	18	ns
t_{1H}	DM7093/8093	V_{CC} = 5.0V				5	10	ns
	DM7094/8094	T_A = 25°C				12	18	ns
t_{0H}	DM7093/8093	V_{CC} = 5.0V				14	24	ns
	DM7094/8094	T_A = 25°C				18	29	ns
t_{H1}	DM7093/8093	V_{CC} = 5.0V				14	21	ns
	DM7094/8094	T_A = 25°C				14	21	ns
t_{H0}	DM7093/8093	V_{CC} = 5.0V				13	25	ns
	DM7094/8094	T_A = 25°C				13	25	ns

NOTE 1. Unless otherwise specified the min-max limits across the −55°C to +125°C temperature range for the DM7093 & DM7094 and across the 0°C to 70°C temperature range for the DM8093 & DM8094. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

NOTE 2. Only one output at a time should be shorted.

NOTE 3. MIN and MAX values refer to the absolute values.

general description (cont.)

A typical system connection is shown in Figure 1 While true that in a TTL system open-collector gates could be used to perform the logic function of these TRI-STATE elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7093/DM8093 and DM7094/DM8094 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level thus assuring both speed and waveform integrity.

It is possible to connect as many as 128 devices to a common bus-line and still have adequate drive capability to allow fan-out from the bus. The example shown in Figure 2 indicates how this guarantee can be made under worst-case conditions.

Another advantage of these buffers is that in the high impedance state their inputs do not present the normal loading to the driving device. This is significant when it is desirable to transmit in both directions over a common line. Figure 3 illustrates such a system. Assume one device in group A is driving the bus-line; and the gates at B are receiving the signals. All outputs at C and D are gated into the high-impedance state. Normally the fan-out from the driving gate at A would be calculated at 4–2 from B and 2 from D, plus additional slight loading from those outputs in the high impedance state. But since the logical "0" input current on D's inputs deliver only 40 μA when these devices are gated into the high impedance state, the loading is significantly reduced. It's true that the logical "1" fan-out remains the same (40 μA times the number of inputs and high-impedance-state outputs). However since the logical "1" fan-out capability of these tri-state devices is 130 while the logical "0" fan-out capability is only 10, it is obvious that the logical "0" fan-out is the limiting item and that a significant increase in the number of inputs which can be tied to the bus-line can be achieved by reducing the number of ~1.6 mA logical "0" loads.

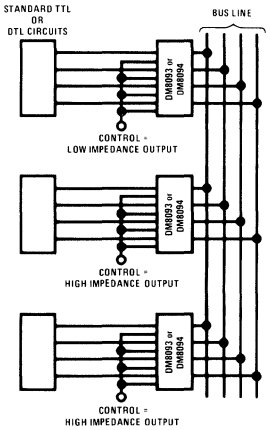


FIGURE 1

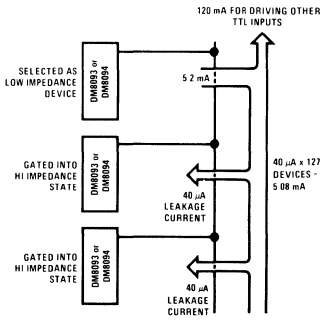


FIGURE 2

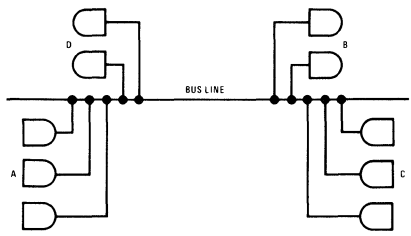


FIGURE 3

Series 54/74

DM7095/DM8095,DM7097/DM8097 TRI-STATE® hex buffers
DM7096/DM8096,DM7098/DM8098 TRI-STATE hex inverters

general description

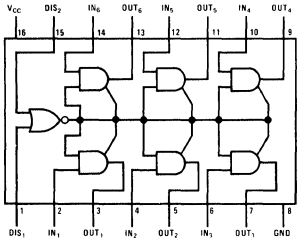
Each of the devices described herein are used to convert standard TTL or DTL outputs to TRI-STATE outputs. The DM7095/DM8095 and the DM7097/DM8097 do so with no logic inversion; the DM7096/DM8096 and DM7098/DM8098 provide the logical opposite of the input signal. The DM7095/DM8095 and DM7096/DM8096 control all six devices from common inputs; the DM7097/DM8097 and DM7098/DM8098 control four devices from one input and two from another input.

features

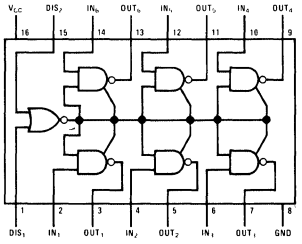
- Maximum package utilization
- Typical power dissipation
  DM7095/DM8095, DM7097/DM8097 325 mW
  DM7096/DM8096, DM7098/DM8098 295 mW
- Typical propagation delay 15 ns

connection diagrams (Dual-In-Line and Flat Packages)

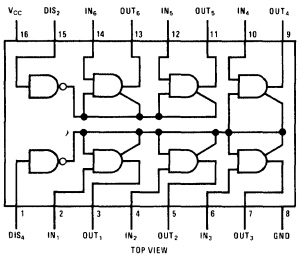
DM7095/DM8095



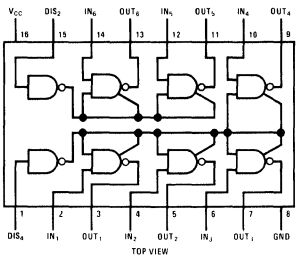
DM7096/DM8096



DM7097/DM8097



DM7098/DM8098



truth tables

DM7095/DM8095

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

DM7096/DM8096

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

DM7097/DM8097

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

DM7098/DM8098

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5-6 only
**Output 1-4 only
X = Irrelevant

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Time that 2 bus-connected devices may be in opposite low-impedance states simultaneously . . .	Indefinite

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7095/6/7/8	4.5	5.5	V
DM8095/6/7/8	4.75	5.25	V
Temperature (T_A)			
DM7095/6/7/8	−55	+125	°C
DM8095/6/7/8	0	70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		V_{CC} = Min	T_A = 25°C	2 0			V
Logical "0" Input Voltage		V_{CC} = Min				0 8	V
Logical "1" Output Voltage	DM7095/6/7/8 DM8095/6/7/8	V_{CC} = Min	I_O = −2.0 mA I_O = −5 2 mA	2 4			V
Logical "1" Output Current Logical "0" Output Voltage		V_{CC} = Min	I_O = 32 mA			0 4	V
Third State Input Current		V_{CC} = Max	V_{IN} = 0 5V DIS = 2 0V			−40	μA
Third State Output Current		V_{CC} = Max	V_O = 2 4V V_O = 0 4V			40 −40	μA μA
Logical "1" Input Current		V_{CC} = Max	V_{IN} = 2 4V V_{IN} = 5 5V			40 1	μA mA
Logical "0" Input Current		V_{CC} = Max	V_{IN} = 0 4V DIS = 0 4V			−1 6	mA
Output Short Circuit Current (Note 3)		V_{CC} = Max	V_O = 0V	−40	−80	−115	mA
Supply Current (each device)	DM7095/7 DM8095/7	V_{CC} = Max			65	85	mA
	DM7096/8 DM8096/8				59	77	
Input Clamp Voltage		V_{CC} = Min	I_{IN} = −12 mA			−1 5	V
Output V_{CC} Clamp Voltage		V_{CC} = 0V	I_O = 12 mA			1 5	V
Output Ground Clamp Voltage		V_{CC} = 0V	I_O = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Data Input to Output, t_{pd0}	DM7095/7 DM8095/7	V_{CC} = 5 0V T_A = 25°C			14	22	ns
	DM7096/8 DM8096/8				10	16	ns
Propagation Delay to a Logical "1" from Data Input to Output, t_{pd1}	DM7095/7 DM8095/7	V_{CC} = 5 0V T_A = 25°C			10	16	ns
	DM7096/8 DM8096/8				11	17	ns
Delay from Disable Input to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0V T_A = 25°C			6	11	ns
Delay from Disable Input to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V T_A = 25°C			16	27	ns
Delay from Disable Input to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5 0V T_A = 25°C			21	35	ns
Delay from Disable Input to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5 0V T_A = 25°C			24	37	ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7095/6/7/8 and across the 0°C to 70°C range for the DM8095/6/7/8 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3. Only one output at a time should be shorted

Series 54/74

DM7121/DM8121 TRI-STATE® eight channel digital multiplexer

general description

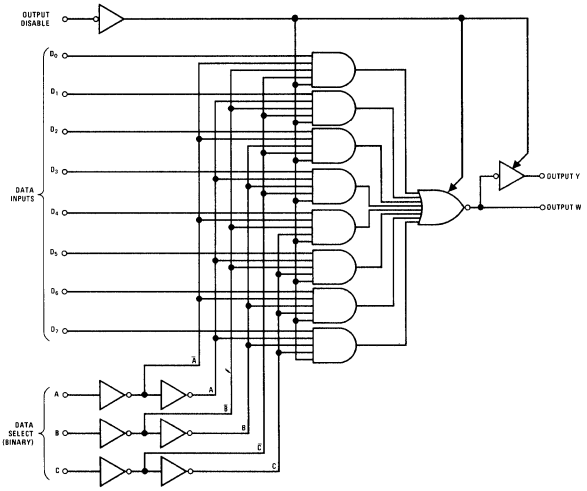
The DM7121/DM8121 multiplexes digital signals from eight lines to one line. Two outputs provide either true or complement information. Three select lines determine which of the eight input lines are routed to the output. A strobe input is provided which when taken to the logical "1" state overrides all other inputs and places the outputs in a defined state.

This unique state turns off both upper and lower output transistors thus presenting a high impedance state and allowing numerous outputs to be connected to a common bus-line. Only one device at a time may be in the normal output state when connected in this manner. The logical "0" state on the strobe line was selected as the level which places the device in the normal output state, because the logical "0" state is usually the unique state which occurs on such devices as the SN5442/SN7442 and SN54154/SN74154 decoders

features

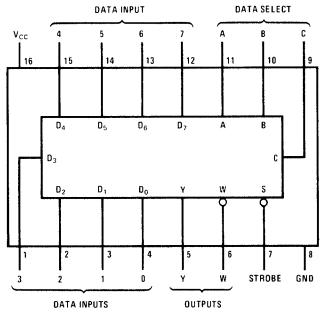
- Performs parallel-to-serial conversion
- Pin compatible with SN54151/SN74151
- Strobe over-ride
- 15 ns typical propagation delay
- 150 mW typical power dissipation
- Outputs can be connected to a common bus-line

logic diagram



connection diagram

Dual-In-Line and Flat Package



truth table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	Hi Z	Hi Z
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM7121	−55°C to +125°C
	DM8121	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7121	V_{CC} = 4.5V		2			V
	DM8121	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7121	V_{CC} = 4.5V				0.8	V
	DM8121	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7121	V_{CC} = 4.5V	I_{OUT} = −2 mA	2.4			V
	DM8181	V_{CC} = 4.75V	I_{OUT} = −5.2 mA				
Logical "0" Output Voltage	DM7121	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8121	V_{CC} = 4.75V					
Logical "1" Input Current	DM7121	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8121	V_{CC} = 5.25V					
	DM7121	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8121	V_{CC} = 5.25V					
Logical "0" Input Current	DM7121	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM8121	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7121	V_{CC} = 5.5V		−20		−55	mA
	DM8121	V_{CC} = 5.25V		−18		−55	
Supply Current	DM7121	V_{CC} = 5.5V			31	51	mA
	DM8121	V_{CC} = 5.25V					
Input Clamp Voltage	DM7121	V_{CC} = 4.5V	T_A = 25°C, I_{IN} = −12 mA			−1.5	V
	DM8121	V_{CC} = 4.75V					
Output V_{CC} Clamp Voltage	DM7121	V_{CC} = 5.5V	I_O = ±12 mA, T_A = 25°C			V_{CC} + 1.5	V
	DM8121	V_{CC} = 5.25V					
Output Ground Clamp Voltage	DM7121	V_{CC} = 5.5V	I_O = −12 mA, T_A = 25°C			−1.5	V
	DM8121	V_{CC} = 5.25V					
Third State Output Current	DM7121	V_{CC} = 5.5V	V_O = 2.4V or 0.4V	−40		40	μA
	DM8121	V_{CC} = 5.25V					
Propagation Delay Time to Logical "1" from A,B,C or D		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω			18	36	ns
Propagation Delay Time to Logical "0" from A,B,C or D		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω			21	33	ns
Propagation Delay Time to Logical "1" from Strobe		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω			17	30	ns
Propagation Delay Time to Logical "0" from Strobe		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω			18	27	ns
Delay from Strobe to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V, T_A = 25°C	to W Output		4	8	ns
			to Y Output		4	8	
Delay from Strobe to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V, T_A = 25°C	to W Output		15	30	ns
			to Y Output		14	28	
Delay from Strobe to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V, T_A = 25°C	to W Output		15	30	ns
			to Y Output		15	30	
Delay from Strobe to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V, T_A = 25°C	to W Output		19	38	ns
			to Y Output		18	36	

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2 Unless otherwise specified min./max. limits apply across the −55°C to +125°C temperature range for the DM7121 and across the 0°C to 70°C range for the DM8121. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3 Only one output at a time should be shorted.

Series 54/74

DM7123/DM8123 TRI-STATE® quad 2-input multiplexer

general description

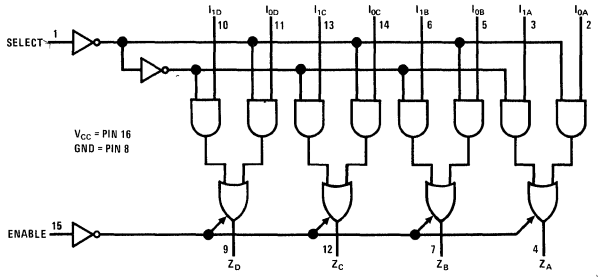
The DM7123/DM8123 consists of four 2-input multiplexers with common input select logic and common output disable circuitry. It allows two groups of four bits each to be multiplexed to four parallel outputs. When the Enable input is at the logical "0" level the outputs are conventional TTL. However, when a logical "1" is applied, the outputs assume a high-impedance state. Both upper and lower output transistors are turned off and the resulting condition allows many devices to be connected to a common bus line without loading down or being loaded down by other devices on the line.

The DM7123/DM8123 is pin compatible and functionally compatible with the FSC 9322 and the SN54157/SN74157 except for the TRI-STATE capability.

features

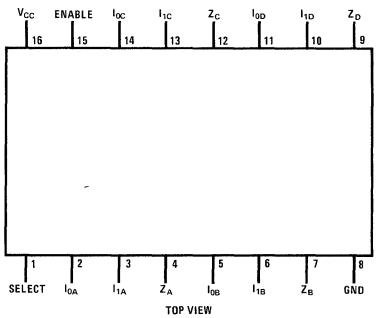
- Typically 10 ns from data to output
- Power dissipation 200 mW typ
- TRI-STATE outputs
- Pin compatible with FSC 9322 and SN54157/SN74157
- Diode clamped inputs

logic diagram



connection diagram

Dual-In-Line and Flat Package



truth table

ENABLE	SELECT	INPUT I_0	INPUT I_1	OUTPUT
1	X	X	X	Hi-Z State
0	1	X	0	0
0	1	X	1	1
0	0	0	X	0
0	0	1	X	1

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7123	−55°C to 125°C
DM8123	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7123 / DM8123	V_{CC} = 4.5V / V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM7123 / DM8123	V_{CC} = 4.5V / V_{CC} = 4.75V				.8	V
Logical "1" Output Voltage	DM7123 / DM8123	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = −2.0 mA, V_{IN} = 2V / I_{OUT} = −5.2 mA, V_{IN} = 2V	2.4			V
Logical "0" Output Voltage	DM7123 / DM8123	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = 16 mA, V_{IN} = 8V			.4	V
Third State Output Current	DM7123 / DM8123	V_{CC} = 5.5V / V_{CC} = 5.25V	$0.40 \leq V_{OLH} \leq 2.4V$, V_{IN} (Enable) = 2V	−40		40	μA
Logical "1" Input Current	DM7123 / DM8123	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
	DM7123 / DM8123	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7123 / DM8123	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 0.4V		−1.0	−1.6	mA
Output Short Circuit Current (Note 3)	DM7123 / DM8123	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 4.5V	−30	−50	−70	mA
Supply Current	DM7123 / DM8123	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} (Enable) = 4.5V, Other Inputs 0V		40	51	mA
Input Clamp Voltage	DM7123 / DM8123	V_{CC} = 5.0V / T_A = 25°C	I_{IN} = −12 mA		−1.0	−1.5	V
Propagation Delay to a Logical "0" from Data to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		5	11	18	ns
Propagation Delay to a Logical "0" from Select to Z_A, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		8	17	24	ns
Propagation Delay to a Logical "1" from Data to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		4	8	15	ns
Propagation Delay to a Logical "1" from Select to Z_A, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		5	15	23	ns
Delay from Disable to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V, T_A = 25°C		4	7	11	ns
Delay from Disable to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V, T_A = 25°C		9	19	27	ns
Delay from Disable to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V, T_A = 25°C		9	18	25	ns
Delay from Disable to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V, T_A = 25°C		10	23	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7123 and across the 0°C to 70°C range for the DM8123. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM7130/DM8130 10-bit comparator
DM7160/DM8160 6-bit comparator

general decription

The DM7130/DM8130 and DM7160/DM8160 comparators determine equality or non-equality between two binary words. The DM7130/DM8130 compares two ten-bit words while the DM7160/DM8160 compares two six-bit words. A strobe over-ride is provided on both devices which when taken to a logical "1" will force the output to a logical "1".

features

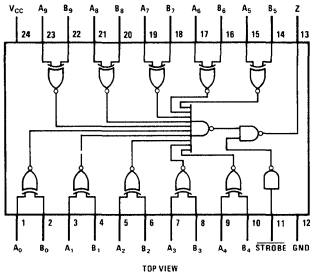
- Series 54/74 compatible
- 20 ns typical compare delay
- Typical power dissipation

DM7130/DM8130	240 mW
DM7160/DM8160	205 mW

- Open collector outputs for expandability

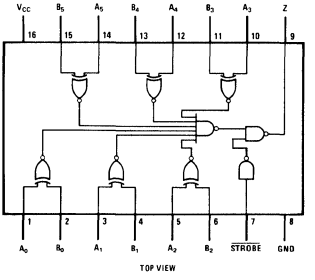
logic and connection diagrams

Dual-In-Line and Flat Package



DM7130/DM8130

Dual-In-Line and Flat Package



DM7160/DM8160

truth table

CONDITION	$\overline{\text{STROBE}}$ S	Z
A = B, A ≠ B	1	1
A = B	0	1
A ≠ B	0	0

For DM7130/DM8130:

$(A) = A_9 \cdots\cdots A_0$
$(B) = B_9 \cdots\cdots B_0$

$$Z = S + [X_0 \cdot X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5 \cdot X_6 \cdot X_7 \cdot X_8 \cdot X_9]$$

For DM7160/DM8160

$(A) = A_5 \cdots\cdots A_0$
$(B) = B_5 \cdots\cdots B_0$

$$Z = S + [X_0 \cdot X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5]$$

where

$$X_0 = A_0 B_0 + \overline{A}_0 \overline{B}_0, \; X_1 = A_1 B_1 + \overline{A}_1 \overline{B}_1$$

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM8130, DM8160	0°C to 70°C
	DM7130, DM7160	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7130,DM7160 DM8130,DM8160	V_{CC} = 4.5V V_{CC} = 4.75V		2			V
Logical "0" Input Voltage	DM7130,DM7160 DM8130,DM8160	V_{CC} = 4.5V V_{CC} = 4.75V				0.8	V
Logical "1" Output Current	DM7130,DM7160 DM8130,DM8160	V_{CC} = 5.5V V_{CC} = 5.25V	V_{OUT} = 5.5V			100	μA
Logical "0" Output Voltage	DM7130,DM7160 DM8130,DM8160	V_{CC} = 4.5V V_{CC} = 4.75V	I_{OL} = 16 mA		0.2	0.4	V
Logical "1" Input Current	DM7130/DM7160 DM8130,DM8160	V_{CC} = 5.5V V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
	DM7130,DM7160 DM8130,DM8160	V_{CC} = 5.5V V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7130,DM7160 DM8130,DM8160	V_{CC} = 5.5V V_{CC} = 5.25V	V_{IN} = 0.4V			−1.6	mA
Supply Current	DM7130,DM7160 DM8130,DM8160	V_{CC} = 5.5V V_{CC} = 5.25V			48	70	mA
	DM7130,DM7160 DM8130,DM8160	V_{CC} = 5.5V V_{CC} = 5.25V			41	60	mA
Input Clamp Voltage	DM7130,DM7160 DM8130,DM8160	V_{CC} = 4.5V V_{CC} = 4.75V	I_{IN} = −12 mA, T_A = 25°C			−1.5	V
Propagation Delay to a Logical "0" from $\overline{\text{Strobe}}$ to Output, t_{pd0}		V_{CC} = 5.0V T_A = 25°C	See ac test circuit		20	30	ns
Propagation Delay to a Logical "1" from $\overline{\text{Strobe}}$ to Output, t_{pd1}		V_{CC} = 5.0V T_A = 25°C	See ac test circuit		9	18	ns
Propagation Delay to a Logical "0" from Data to Output, t_{pd0}		V_{CC} = 5.0V T_A = 25°C	See ac test circuit		27	40	ns
Propagation Delay to a Logical "1" from Data to Output, t_{pd1}		V_{CC} = 5.0V T_A = 25°C	See ac test circuit		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7130 and DM7160 and across the 0°C to 70°C range for the DM8130 and DM8160. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Series 54/74

DM7131/DM8131, DM7136/DM8136 6-bit unified bus comparator

general description

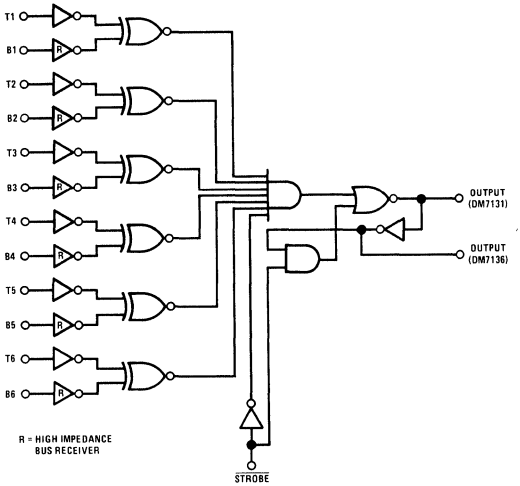
The DM7131/DM8131, DM7136/DM8136 compare two binary words of two-to-six-bits in length and indicates matching bit-for-bit of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high impedance receivers driven by a terminated data bus. These bus inputs include 1V typical hysteresis which provides 1.8V noise immunity. The DM7131/DM8131 has active pull up output and goes to the low state upon comparison. The DM7136/DM8136 has open-collector output which goes to high state upon comparison and is expandable to n bits by collector-ORing. Both devices have an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level without affecting the state of output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

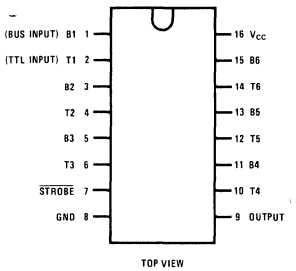
features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.8V typ
- High fan out
- Input clamping diodes
- Output compatible with TTL circuits
- Output latch provision

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Supply Voltage	7V
TTL and Strobe Input Voltage	5.5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C

operating conditions

	MIN	TYP	MAX	UNITS
Supply Voltage				
DM7131,DM7136	4.5	5	5.5	V
DM8131,DM8136	4 75	5	5.25	V
Temperature (T_A)				
DM7131,DM7136	−55	+25	+125	°C
DM8131,DM8136	0	+25	+70	°C

electrical characteristics (Operating Temperature Range — Unless Otherwise Specified)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input "1" Voltage (Except Bus Inputs)	V_{CC} = Min		2 0			V
Input "0" Voltage (Except Bus Inputs)	V_{CC} = Min				0 8	V
Bus Input "1" Threshold Voltage	DM7131,DM7136		1 65	2 25	2 65	V
	DM8131,DM8136		1 80	2 25	2 50	V
Bus Input "0" Threshold Voltage	DM7131,DM7136		0 97	1 3	1 63	V
	DM8131,DM8136		1 05	1 3	1 55	V
Input Clamp Diode Voltage	V_{CC} = Max, I_{IN} = −12 mA T_A = +25°C				−1 5	V
TTL Input "1" Current	V_{CC} = Max, V_{IN} = 2 4V				40	μA
	V_{IN} = 5 5V				1	mA
TTL Input "0" Current	V_{CC} = Max, V_{IN} = 0 4V				−1 6	mA
Strobe Input "1" Current	V_{CC} = Max, V_{IN} = 2 4V				80	μA
	V_{IN} = 5 5V				2	mA
Strobe Input "0" Current	V_{CC} = Max, V_{IN} = 0 4V				−2 4	mA
Maximum Bus Input Current	V_{CC} = Max, V_{IN} = 4V			15	50	μA
	V_{CC} = 0V, V_{IN} = 4V			1	50	μA
Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0 4	V
Logic "1" Output Voltage	V_{CC} = Min, I_{OUT} = −400 μA	DM7131 DM8131	2 4			V
Logic "1" Output Current	V_{CC} = Max, V_{OUT} = 5V	DM7136 DM8136			250	μA
Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0V	DM7131	−20		−55	mA
		DM8131	−18		−55	mA
Power Supply Current	V_{CC} = Max			50	74	mA
Propagation Delays						
TTL Input to Output, t_{pd1}	V_{CC} = 5V, T_A = 25°C			20		ns
TTL Input to Output, t_{pd0}	V_{CC} = 5V, T_A = 25°C			20		ns
Bus Input to Output, t_{pd1}	V_{CC} = 5V, T_A = 25°C			30		ns
Bus Input to Output, t_{pd0}	V_{CC} = 5V, T_A = 25°C			30		ns
Strobe Input to Output, t_{pd1}	V_{CC} = 5V, T_A = 25°C			20		ns
Strobe Input to Output, t_{pd0}	V_{CC} = 5V, T_A = 25°C			20		ns

Series 54/74

DM7200/DM8200 4-bit comparator

general description

The DM7200/DM8200 is a monolithic TTL (Transistor-Transistor Logic) circuit which is used to compare the numerical values of two four-bit binary numbers. Outputs indicate (1) whether number A is greater than number B, (2) whether number B is greater than number A, or (3) whether the two numbers are equal. A strobe input overrides all other inputs and places the outputs in a definite state. The design chosen provides maximum speed with minimum circuit complexity. Numerical comparisons of words longer than four bits may be made by using additional DM7200/DM8200's only.

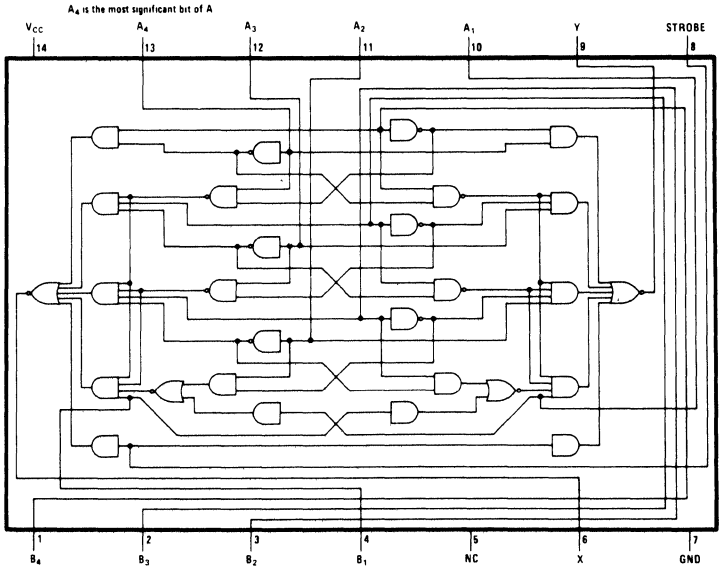
features

- Series 54/74 Compatible
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Typical Propagation Delay 20 ns
- Typical Power Dissipation 175 mW

applications

- Digital stepping-motor control applications
- Convergence applications
- Summing junction for digital servo systems

logic and connection diagram (Dual-In-Line and Flat Package)



logic table

Input				Output	
Number $A_4A_3A_2A_1$		Number $B_4B_3B_2B_1$	Strobe	X	Y
A	>	B	0	1	0
A	<	B	0	0	1
A	=	B	0	1	1
A	≷	B	1	0	0

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM7200	−55°C to +125°C
	DM8200	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7200	V_{CC} = 4.5V	2.0			V
	DM8200	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7200	V_{CC} = 4.5V			.8	V
	DM8200	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7200	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM8200	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM7200	V_{CC} = 4.5V, I_{OUT} = 16 mA			.4	V
	DM8200	V_{CC} = 4.75V				
Logical "1" Input Current	DM7200	V_{CC} = 5.5V, V_{IN} = 2.4V			80	μA
	DM8200	V_{CC} = 5.25V				
Logical "0" Input Current	DM7200	V_{CC} = 5.5V, V_{IN} = 0.4V			−3.2	mA
	DM8200	V_{CC} = 5.25V				
Logical "1" Input Current	DM7200	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8200	V_{CC} = 5.25V				
Output Short Circuit Current (Note 2)	DM7200	V_{CC} = 5.5V	−20		−55	mA
	DM8200	V_{CC} = 5.25V	−18		−55	
Supply Current	DM7200	V_{CC} = 5.5V		35	53	mA
	DM8200	V_{CC} = 5.25V				
Propagation Delay to a Logical "1" from Any Data Input to Output t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		24	40	ns
Propagation Delay to a Logical "0" from Any Data Input to Output t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		17	30	ns
Propagation Delay to a Logical "1" from Strobe Input to Output t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		15	27	ns
Propagation Delay to a Logical "0" from Strobe Input to Output t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		8	18	ns
Time Prior to Removal of Strobe that Data Inputs Must Be Stabilized; $t_{SET\ UP}$		V_{CC} = 5.0V, T_A = 25°C		0	10	ns
Time After Activation of Strobe that Data Inputs Must be Held, t_{HOLD}		V_{CC} = 5.0V, T_A = 25°C		−10	0	ns

Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7200 and 0°C to +70°C for the DM8200. Typical values apply to supply voltages of 5.0V.

Note 2: Only one output should be shorted at a time.

Series 54/74

DM7210/DM8210 8-channel digital switch
DM7211/DM8211 8-channel digital switch

general description

The DM7210/DM8210 and DM7211/DM8211 are digital bipolar integrated circuits employing TTL, used to multiplex eight INPUT channels to a single OUTPUT. Depending upon the 3-bit binary number applied to the SELECT lines, the digital bit on the unique INPUT selected appears on the output.

The DM7211/DM8211 provides a strobe input which when taken to a logical "1" level places the output in the logical "1" state.

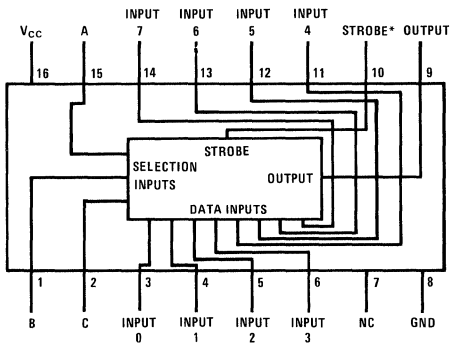
The circuit can also be used to convert parallel input information to serial output information. If eight bits of parallel information are applied to the inputs, and if the binary numbers 000 through 111 are sequenced on the select lines, the output will provide a serial presentation of the input bits.

features

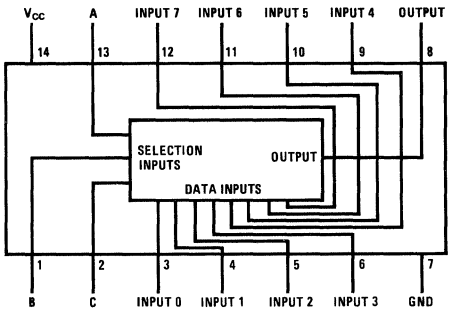
- TTL Circuitry
- Input Clamping Diodes
- 1 Volt Typical Noise Immunity
- 400 mV Guaranteed Noise Immunity
- Completely compatible with Series 54/74 circuits

connection diagrams

Dual-In-Line and Flat Packages



*A Logical 1 on the strobe input causes the output to go the Logical 1 state
A Logical 0 on the strobe input allows information to be routed through the device.



absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Fanout		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7210, DM7211	−55°C to +125°C
	DM8210, DM8211	0°C to +70°C
Lead Temperature (soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7210, DM7211	V_{CC} = 4.5V	2.0			V
	DM8210, DM8211	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7210, DM7211	V_{CC} = 4.5V			0.8	V
	DM8210, DM8211	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7210, DM7211	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM8210, DM8211	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM7210, DM7211	V_{CC} = 4.5V, I_{OUT} = 16 mA			0.4	V
	DM8210, DM8211	V_{CC} = 4.75V				
Logical "1" Input Current (All Inputs)	DM7210, DM7211	V_{CC} = 5.5V, V_{IN} = 2.4V			40	μA
	DM8210, DM8211	V_{CC} = 5.25V				
Logical "1" Input Current (All Inputs)	DM7210, DM7211	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8210, DM8211	V_{CC} = 5.25V				
Logical "0" Input Current (All Inputs)	DM7210, DM7211	V_{CC} = 5.5V, V_{IN} = 0.4V		−1.0	−1.6	mA
	DM8210, DM8211	V_{CC} = 5.25V				
Input Clamp Diode (All Inputs)	DM7210, DM7211	V_{CC} = 5.5V, I_{IN} = −12 mA, T_A = 25°C		−1.0	−1.5	V
	DM8210, DM8211	V_{CC} = 5.25V				
Output Short Circuit Current	DM7210, DM7211	V_{CC} = 5.5V, V_{OUT} = 0	−20		−55	mA
	DM8210, DM8211	V_{CC} = 5.25V	−18			
Power Supply Current (All Inputs GND)	DM7210, DM7211	V_{CC} = 5.5V		20	33	mA
	DM8210, DM8211	V_{CC} = 5.25V				
Propagation Delay to a Logical "0" From Data Input to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	10	21	30	ns
Propagation Delay to a Logical "0" From Strobe Input to Output		V_{CC} = 5.0V, T_A = 25°C	10	19	27	ns
Propagation Delay to a Logical "1" From Data Input to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	10	23	32	ns
Propagation Delay to a Logical "1" From Strobe Input to Output		V_{CC} = 5.0V, T_A = 25°C	10	21	30	ns
Data Selection Settling Time From 0→1 Transition on A, B, C (t_{s1})		V_{CC} = 5.0V, T_A = 25°C	15	31	43	ns
Data Selection Settling Time From 1→0 Transition on A, B, C (t_{s0})		V_{CC} = 5.0V, T_A = 25°C	15	31	42	ns

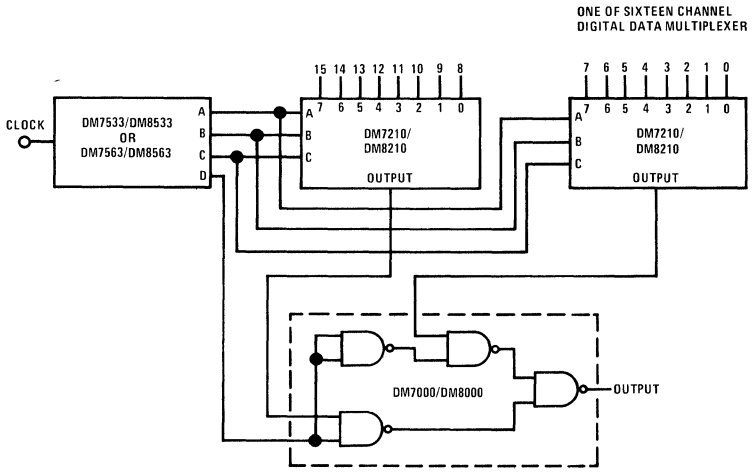
Note 1 Unless otherwise specified the min-max limits apply across the −55°C to +125°C temperature range for the DM7210 and DM7211 and across the 0°C to 70°C temperature range for the DM8210 and DM8211. Typicals are given for V_{CC} = 5.0V and 25°C.

logic table

SELECTION INPUTS C	B	A	STROBE (DM7211/DM8211 ONLY)	DATA INPUTS 0	1	2	3	4	5	6	7	OUTPUT
0	0	0	0	0	X	X	X	X	X	X	X	0
0	0	0	0	1	X	X	X	X	X	X	X	1
0	0	1	0	X	0	X	X	X	X	X	X	0
0	0	1	0	X	1	X	X	X	X	X	X	1
0	1	0	0	X	X	0	X	X	X	X	X	0
0	1	0	0	X	X	1	X	X	X	X	X	1
0	1	1	0	X	X	X	0	X	X	X	X	0
0	1	1	0	X	X	X	1	X	X	X	X	1
1	0	0	0	X	X	X	X	0	X	X	X	0
1	0	0	0	X	X	X	X	1	X	X	X	1
1	0	1	0	X	X	X	X	X	0	X	X	0
1	0	1	0	X	X	X	X	X	1	X	X	1
1	1	0	0	X	X	X	X	X	X	0	X	0
1	1	0	0	X	X	X	X	X	X	1	X	1
1	1	1	0	X	X	X	X	X	X	X	0	0
1	1	1	0	X	X	X	X	X	X	X	1	1
X	X	X	1	X	X	X	X	X	X	X	X	1

X = "Don't Care" Condition

typical application



Series 54/74

DM7214/DM8214 TRI-STATE® dual 4:1 multiplexer

general description

The DM7214/DM8214 is a TRI-STATE dual four-line to one-line multiplexer. The device acts as a double-pole four-throw switch. One data line is selected from each of two four-line inputs. Two SELECT lines determine which of the four inputs is chosen, however the same input of both four-line selections will be selected. TRI-STATE logic allows for the added feature that the outputs of the device can be tied to outputs of similar devices and connected to a common bus-line. Nominal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If, however, on all but one of the connected devices both the upper and lower output transistors are turned off, then the one remaining device in the normal low-impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7214/DM8214 The STROBE input is used to place the output in this unique high-impedance state

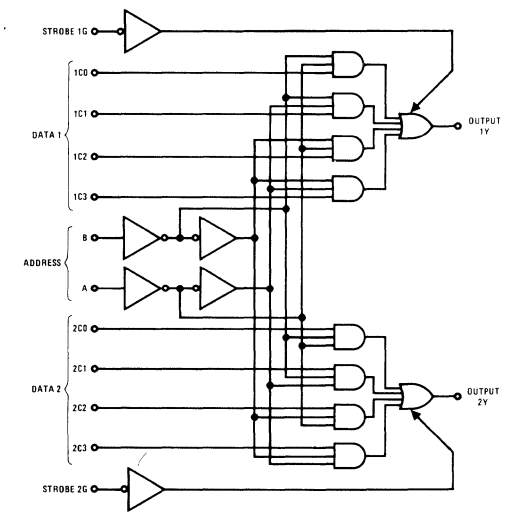
features

- Pin-for-pin compatible with SN54153/SN74153
- Organized for party-line systems
- Up to 128 devices can be connected to a common bus-line
- Propagation delay 20 ns typical
- Power dissipation 170 mW typical
- Input diode clamps
- Series 54/74 compatible

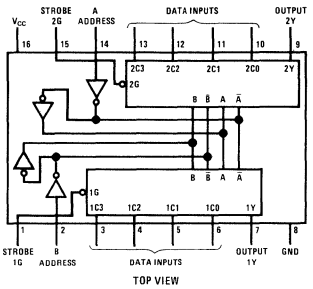
The DM7214 is characterized for operation over the full military temperature range of −55°C to +125°C, the DM8214 is characterized for operation from 0°C to 70°C.

1

logic and connection diagrams

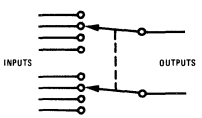


Dual-In-Line and Flat Package



TOP VIEW

Analogous to DP4T Switch



truth table

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	Hi Z
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

X = DON'T CARE

absolute maximum ratings (Note 1)

V_{CC}	7V
Input Voltage	5 5V
Output Voltage	5.5V
Time that two bus-connected devices may be in opposite low impedance states simultaneously (5% Duty Cycle)	Indefinitely
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DM7214	−55°C to +125°C
DM8214	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5 0V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
Logical "1" Input Voltage	DM7214 V_{CC} = 4.5V; DM8214 V_{CC} = 4 75V	2.0			V
Logical "0" Input Voltage	DM7214 V_{CC} = 4.5V; DM8214 V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM7214 V_{CC} = 4 5V, I_{OUT} = −2.0 mA; DM8214 V_{CC} = 4.75V, I_{OUT} = −5 2 mA	2 4	3.2		V
Logical "0" Output Voltage	DM7214 V_{CC} = 4.5V; DM8214 V_{CC} = 4.75V, I_{OUT} = 16 mA		0.2	0.4	V
Logical "1" Input Current	DM7214 V_{CC} = 5.5V; DM8214 V_{CC} = 5 25V, V_{IN} = 2.4V			40	μA
	V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	DM7214 V_{CC} = 5.5V; DM8214 V_{CC} = 5 25V, V_{IN} = 0 4V			−1.6	mA
Short-Circuit Output Current (Note 3)	DM7214 V_{CC} = 5.5V; DM8214 V_{CC} = 5.25V, V_{OUT} = 0V	−20 −18		−55 −57	mA
Output Disable Current (Hi-Z Output State)	DM7214 V_{CC} = 5 5V, V_{OUT} = 0 4V to 2 4V; DM8214 V_{CC} = 5.25V, V_{OUT} = 0.4V to 2.4V			40 −40	μA
Supply Current	DM7214 V_{CC} = 5.5V; DM8214 V_{CC} = 5.25V, All inputs at GND		34 34	56 65	mA
Propagation Delay from Data to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF		15	23	ns
t_{pd0}			12	18	
Propagation Delay from Address to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF		20	34	ns
t_{pd0}			20	34	
Delay from Logical "1" to Hi-Z Output State, t_{1H}	V_{CC} = 5.0V, T_A = 25°C		5	10	ns
Delay from Logical "0" to Hi-Z Output State, t_{0H}	V_{CC} = 5.0V, T_A = 25°C		15	23	ns
Delay from Hi-Z to Logical "1" Output State, t_{H1}	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF		12	18	ns
Delay from Hi-Z to Logical "0" Output State, t_{H0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF		14	21	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7214 and across the 0°C to 70°C range for the DM8214 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54/74

DM7219/DM8219 TRI-STATE® 16-line to one-line multiplexer

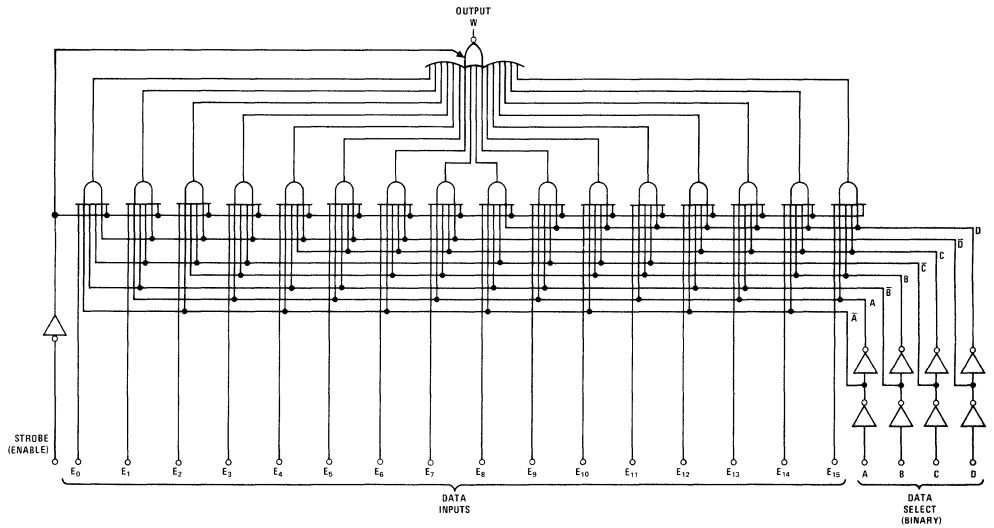
general description

The DM7219/DM8219 multiplexes sixteen digital lines to one output. A four-bit code determines the particular one-of-sixteen inputs which is routed to the output. The data is inverted from input to output. A strobe over-ride places the output in the high-impedance state.

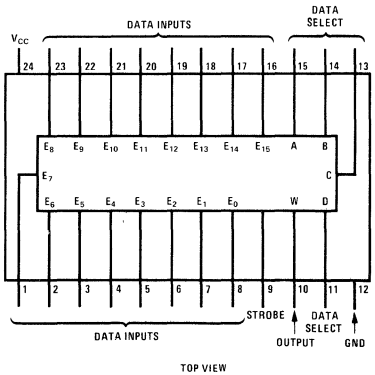
features

- Typical propagation delay 10 ns
- Typical power dissipation 225 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7219	4.5	5 5	V
DM8219	4.75	5.25	V
Temperature (T_A)			
DM7219	−55	+125	°C
DM8219	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage DM7219 / DM8219	V_{CC} = Min, I_{OUT} = −2.0 mA; $V_{IN(1)}$ = 2 0V, I_{OUT} = −5 2 mA; $V_{IN(0)}$ = 0.8V	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = +16 mA			0 4	V
Third State Output Current	V_{CC} = Max, V_{OUT} = 2.4V V_{OUT} = 0.4V			±40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V V_{IN} = 5 5V			40 1.0	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1 6	mA
Output Short Circuit Current DM7219 / DM8219	V_{CC} = Max, V_{OUT} = 0V	−30 −28		−100 −100	mA mA
Supply Current	V_{CC} = Max, V_{IN} = 4.5V			68	mA
Input Diode Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA, T_A = 25°C			−1 5	V
Propagation Delay to a Logical "0" from Data Select Inputs to Output, t_{pd0}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C, R_L = 400Ω		22	33	ns
Propagation Delay to a Logical "1" from Data Select Inputs to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		21	35	ns
Propagation Delay to a Logical "0" from Data Inputs to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		8.5	14	ns
Propagation Delay to a Logical "1" from Data Inputs to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		13	20	ns
Delay from Strobe to High Impedance State (from Logical "1" Level), t_{1H}	V_{CC} = 5 0V, T_A = 25°C		5 0	10	ns
Delay from Strobe to High Impedance State (from Logical "0" Level), t_{0H}	V_{CC} = 5.0V, T_A = 25°C		21	30	ns
Delay from Strobe to Logical "1" Level (from High Impedance State), t_{H1}	V_{CC} = 5 0V, T_A = 25°C		15	23	ns
Delay from Strobe to Logical "0" Level (from High Impedance State), t_{H0}	V_{CC} = 5 0V, T_A = 25°C		17	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7219 and across the 0°C to 70°C range for the DM8219. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

truth table

INPUTS																				OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hi-Z
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
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1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

Series 54/74

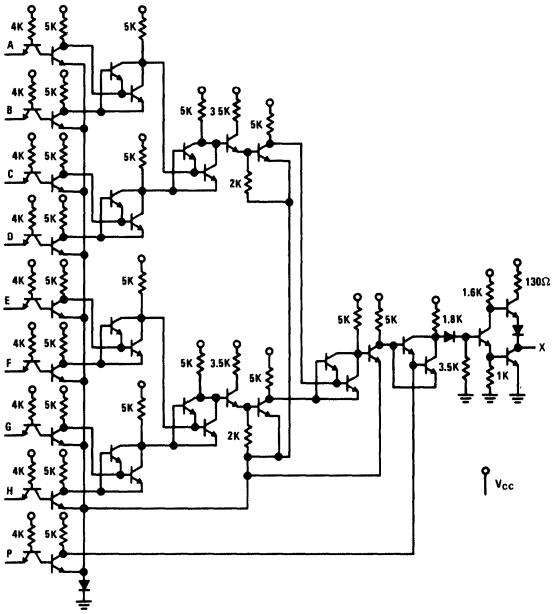
DM7220/DM8220 parity generator and checker

general description

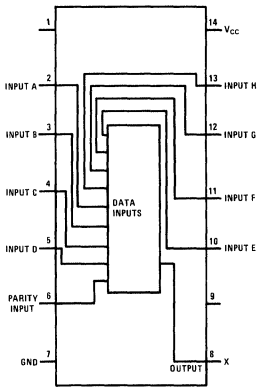
The DM7220/DM8220 is a monolithic integrated circuit which can be used to both generate a parity bit and check for parity. Nine inputs and a single output are provided. When it is desired to generate a parity bit, eight of the nine inputs are connected to the eight data transmission lines. Depending upon whether odd parity or even parity is desired a logical 1 or a logical 0 is applied to the ninth input. For a parity check, the output of the parity generator (sending end) is connected to the ninth input of the parity checker (receiver end). The resulting output of the parity checker will remain in one particular logic state unless a bit is "lost" during transmission.

The device is fully compatible with other Series 54/74 circuits.

schematic and connection diagrams

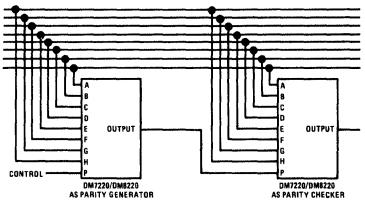


Dual-In-Line and Flat Package



$X = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus H \oplus \overline{P}$

typical application



If the control line is a logical "0" the parity generator will generate odd parity. The parity checker will acknowledge the presence of an odd number of "1"s (odd parity) with a logical "0" on its output

If the control line is a logical "1" the parity generator will generate even parity The parity checker will acknowledge the presence of an even number of "1"s (even parity) with a logical "1" on its output

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7220	−55°C to +125°C
	DM8220	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7220	V_{CC} = 4.5V		2.0			V
	DM8220	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7220	V_{CC} = 4.5V				0.8	V
	DM8220	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7220	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8220	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7220	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8220	V_{CC} = 4.75V					
Logical "1" Input Current	DM7220	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8220	V_{CC} = 5.25V					
Input Diode Clamp Voltage	DM7220	V_{CC} = 5.5V	I_{IN} = −12 mA		−1.1	−1.5	V
	DM8220	V_{CC} = 5.25V	T_A = 25°C				
Logical "1" Input Current	DM7220	V_{CC} = 5.5V	V_{IN} = 5.5V			1.0	mA
	DM8220	V_{CC} = 5.25V					
Logical "0" Input Current	DM7220	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM8220	V_{CC} = 5.25V					
Output Short Circuit Current	DM7220	V_{CC} = 5.5V	V_{OUT} = 0V	20		55	mA
	DM8220	V_{CC} = 5.25V		18			
Power Supply Current	DM7220	V_{CC} = 5.5V			26	35	mA
	DM8220	V_{CC} = 5.25V					
Propagation Delay to Logical "1", t_{pd1} Inputs A, B, C, D, E, F, G, H		V_{CC} = 5.0V C_O = 50 pF	T_A = 25°C F.O. = 10	15	36	58	ns
Propagation Delay to Logical "0", t_{pd0} Inputs A, B, C, D, E, F, G, H		V_{CC} = 5.0V C_O = 50 pF	T_A = 25°C F.O. = 10	11	32	52	ns
Propagation Delay to Logical "1", t_{pd1} Input P		V_{CC} = 5.0V C_O = 50 pF	T_A = 25°C F.O. = 10	8	21	35	ns
Propagation Delay to Logical "0", t_{pd0} Input P		V_{CC} = 5.0V C_O = 50 pF	T_A = 25°C F.O. = 10	7	14	25	ns

Note 1: Unless otherwise specified the min-max limits apply across the −55°C to +125°C temperature range for the DM7220 and across the 0°C to 70°C temperature range for the DM8220. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Series 54/74

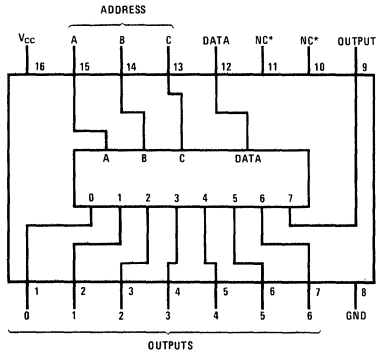
DM7223/DM8223 1-line to 8-line demultiplexer

general description

The DM7223/DM8223 1-line to 8-line demultiplexer utilizes Series 54/74 compatible circuitry to demultiplex a data train to one of eight outputs. These eight outputs are capable of driving 10 standard TTL loads each. Three address lines determine which output receives the data train. When the data input is a logical "0" only the addressed output will be a logical "0". When the data input is a logical "1", all outputs, and therefore the addressed output, will be logical "1's".

connection diagram

Dual-In-Line Package



*Do not make connection to Pins 10 or 11

TOP VIEW

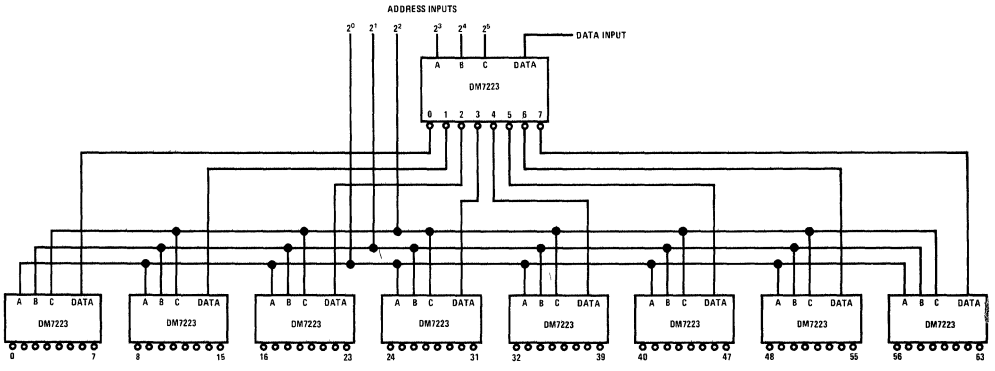
logic table

DATA	ADDRESS INPUTS			OUTPUTS							
	C	B	A	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

X = Don't Care

typical application

Digital Data Demultiplexer (1 Line to 64 Lines)



absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Fan Out	10
Operating Temperature Range	
DM7223	−55°C to +125°C
DM8223	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7223	V_{CC} = 4.5V		2.0			V
	DM8223	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7223	V_{CC} = 4.5V				0.8	V
	DM8223	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7223	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8223	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7223	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8223	V_{CC} = 4.75V					
Logical "1" Input Current	DM7223	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8223	V_{CC} = 5.25V					
	DM7223	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8223	V_{CC} = 5.25V					
Logical "0" Input Current	DM7223	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM8223	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7223	V_{CC} = 5.5V	V_{OUT} = 0V	−20	−32	−55	mA
	DM8223	V_{CC} = 5.25V		−18			
Supply Current	DM7223	V_{CC} = 5.5V			28	41	mA
	DM8223	V_{CC} = 5.25V					
Input Clamp Voltage	DM7223	V_{CC} = 5.5V	I_{IN} = −12 mA		−1.0	−1.5	V
	DM8223	V_{CC} = 5.25V					
Propagation Delay to a Logical "0"		V_{CC} = 5.0V, T_A = 25°C	C_{OUT} = 50 pF, F.O. = 10	12	24	35	ns
Propagation Delay to a Logical "1"		V_{CC} = 5.0V, T_A = 25°C	C_{OUT} = 50 pF, F.O. = 10	12	26	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7223 and across the 0°C to 70°C range for the DM8223. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM7230/DM8230 TRI-STATE® demultiplexer

general description

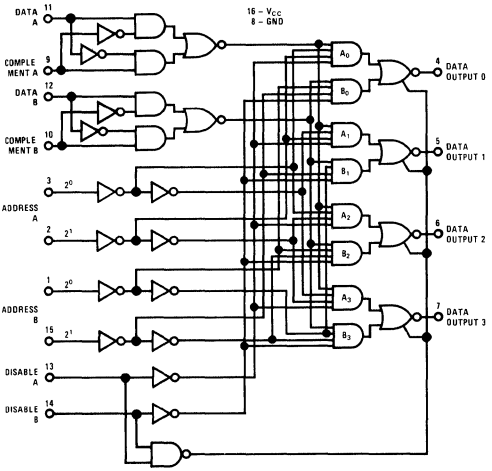
The DM7230/DM8230 demultiplexer is another device in National's TRI-STATE logic family.

Digital signals applied to two input lines can be routed to two-of-four output lines depending upon the logic on the Address inputs. Outputs can be directly connected to other similar outputs for use in bus-organized systems.

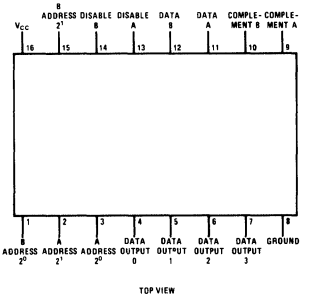
features

- Series 54/74 compatible
- 20 ns propagation delay
- Data complement capability
- Very low output impedance—high drive capability
- Separate input disable controls
- High-impedance output state which allows many outputs to be connected to a common bus-line.

logic and connection diagrams



Dual-In-Line and Flat Package



logic table

DATA A	COMP A	DATA B	COMP B	ADDRESS A 2^1	ADDRESS A 2^0	ADDRESS B 2^1	ADDRESS B 2^0	DIS A	DIS B	OUT 0	OUT 1	OUT 2	OUT 3
0	0	X	X	0	0	X	X	0	1	0	1	1	1
0	1	X	X	0	0	X	X	0	1	1	1	1	1
1	0	X	X	0	0	X	X	0	1	1	1	1	1
1	1	X	X	0	0	X	X	0	1	0	1	1	1
0	0	X	X	0	1	X	X	0	1	1	0	1	1
0	1	X	X	0	1	X	X	0	1	1	1	1	1
1	0	X	X	0	1	X	X	0	1	1	1	1	1
1	1	X	X	0	1	X	X	0	1	1	0	1	1
0	0	X	X	1	0	X	X	0	1	1	1	1	1
0	1	X	X	1	0	X	X	0	1	1	1	1	1
1	0	X	X	1	0	X	X	0	1	1	1	1	1
1	1	X	X	1	0	X	X	0	1	1	1	1	1
0	0	X	X	1	1	X	X	0	1	1	1	1	1
0	1	X	X	1	1	X	X	0	1	1	1	1	1
1	0	X	X	1	1	X	X	0	1	1	1	1	1
1	1	X	X	1	1	X	X	0	1	1	1	1	1
X	X	0	0	X	X	0	0	1	0	0	1	1	1
X	X	0	1	X	X	0	0	1	0	1	1	1	1
X	X	1	0	X	X	0	0	1	0	1	1	1	1
X	X	1	1	X	X	0	0	1	0	0	1	1	1
X	X	0	0	X	X	0	1	1	0	1	0	1	1
X	X	0	1	X	X	0	1	1	0	1	1	1	1
X	X	1	0	X	X	0	1	1	0	1	1	1	1
X	X	1	1	X	X	0	1	1	0	1	0	1	1
X	X	0	0	X	X	1	0	1	0	1	1	0	1
X	X	0	1	X	X	1	0	1	0	1	1	1	1
X	X	1	0	X	X	1	0	1	0	1	1	1	1
X	X	1	1	X	X	1	0	1	0	1	1	0	1
X	X	0	0	X	X	1	1	1	0	1	1	1	0
X	X	0	1	X	X	1	1	1	0	1	1	1	1
X	X	1	0	X	X	1	1	1	0	1	1	1	1
X	X	1	1	X	X	1	1	1	0	1	1	1	0
X	X	X	X	X	X	X	X	1	1	Hi Z	Hi Z	Hi Z	Hi Z

absolute maximum ratings

Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Input Voltage	5 5V	Operating Temperature Range	
Output Voltage	5 5V	DM7230	−55°C to +125°C
Time that two bus-connected devices may be in opposite low impedance states simultaneously (5% duty cycle)	Indefinite	DM8230	0°C to +70°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7230	V_{CC} = 4 5V	2 0			V
	DM8230	V_{CC} = 4 75V				
Logical "0" Input Voltage	DM7230	V_{CC} = 4 5V			0 8	V
	DM8230	V_{CC} = 4 75V				
Logical "1" Output Voltage	DM7230	V_{CC} = 4 5V, I_{OUT} = −2 mA	2 4	3 5		V
	DM8230	V_{CC} = 4 75V, I_{OUT} = −5 2 mA				
Logical "0" Output Voltage	DM7230	V_{CC} = 4 5V		0 2	0 4	V
	DM8230	V_{CC} = 4 75V I_{OUT} = 16 mA				
Logical "0" Input Current	DM7230	V_{CC} = 5 5V V_{IN} = 0 4V				
	DM8230	V_{CC} = 5 25V				
		Disable inputs		−2 0	−3 2	mA
		All other inputs		−1 0	−1 6	mA
Logical "1" Input Current	DM7230	V_{CC} = 5 5V V_{IN} = 2 4V				
	DM8230	V_{CC} = 5 25V				
		Disable inputs			80	μA
		All other inputs			40	μA
Logical "1" Input Current	DM7230	V_{CC} = 5 5V V_{IN} = 5 5V			1 0	mA
	DM8230	V_{CC} = 5 25V				
Output Disable Current	DM7230	V_{CC} = 5 5V V_O = 2 4V			40	μA
	DM8230	V_{CC} = 5 25V V_O = 0 4V			−40	μA
Output Short Current (Note 2)	DM7230	V_{CC} = 5 5V V_O = 0 0V	−30		−70	mA
	DM8230	V_{CC} = 5 25V	−28			
Supply Current	DM7230	V_{CC} = 5 5V V_{IN} = 5 0V		48	75	mA
	DM8230	V_{CC} = 5 25V				
Input Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C I_{IN} = −12 mA			−1 5	V
Output Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C I_{OUT} = −12 mA			−1 5	V
		I_{OUT} = +12 mA			V_{CC} +1 5	V
Propagation Delay to Logical "1" from Data or Complement Input, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF				
		Noninverting		13	24	ns
		Inverting		20	36	ns
Propagation Delay to Logical "0" from Data or Complement Input, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF				
		Noninverting or Inverting		18	26	ns
Propagation Delay to Logical "1" from Address Input, t_{pd1} (Note 3)		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF		20	36	ns
Propagation Delay to Logical "0" from Address Input, t_{pd0} (Note 3)		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF		20	30	ns
Propagation Delay to Logical "1" from Disable Input, t_{pd1} (Note 4)		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF		13	25	ns
Propagation Delay to Logical "0" from Disable Input, t_{pd0} (Note 4)		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF		16	25	ns
Delay from Disable Input to High Impedance State (Note 5), t_{iH}		V_{CC} = 5 0V, T_A = 25°C		7	14	ns
t_{OH}				15	27	ns
Delay from Disable Input to Low Impedance State (Note 5), t_{HI}		V_{CC} = 5 0V, T_A = 25°C C_L = 50 pF		15	23	ns
t_{HO}				18	27	ns

Note 1: Min/max values apply across the −55°C to +125°C temperature range for the DM7230 and across the 0°C to 70°C range for the DM8230 unless otherwise specified Typicals are given for T_A = 25°C and V_{CC} = 5 0V

Note 2: Only one output at a time should be short circuited.

Note 3: The only conditions under which a t_{pd0} from the Address inputs can be observed is when an output goes from being nonselected to being selected and the information being routed to that output is a logical "0" If the information had been a logical "1," no change would have occurred and no measurement could have been made Similarly, the only time a t_{pd1} from the Address inputs can be observed, is when an output goes from being selected to being nonselected and the information that had been routed to that output was a logical "0" If the information had been a logical "1," no change would have occurred and no measurement could have been made

Note 4: Information in Note 3 concerning t_{pd0} and t_{pd1} from the address inputs are applicable here also

Note 5: All delays involving transitions to or from the High Impedance state are measured with respect to the Disable inputs For example, with A information at a logical "0" and Disable B at a logical "1" the selected output will go from a logical "0" to the High Impedance state some time, t_{OH}, after Disable A has gone from a logical "0" to a logical "1"

mode of operation

COMPLEMENT AND DATA INPUTS

When Complement A is a logical "1", Data A will appear inverted at the output. When Complement A is a logical "0", Data A will appear non-inverted at the output.

This function is accomplished on the chip through the use of a two-input exclusive-OR gate with Complement A and Data A as the two inputs. Therefore, the A information that is routed to the outputs is actually (Complement A ⊕ Data A). That this is the case may be verified by examining the logic diagram.

The two inputs of this exclusive-OR gate have identical characteristics, allowing the functions of these two inputs to be reversed. Also the propagation delay from either input to the output will be the same. This is also true for the Complement B and Data B inputs.

ADDRESS INPUTS

The Address A inputs select to which of the four outputs A information will be routed. The same is true for the Address B inputs and B information. If A and B information are both routed to the same output simultaneously, that output will be a logical "0" if either the A or B information is a logical "0". All outputs which are not selected for either A or B information will be in the logical "1" state.

DISABLE INPUTS

The Disable inputs are similar to higher order Address inputs in that when Disable A is a logical "1", A information is not routed to any output. All four outputs are nonselected for A information. The same is true for Disable B and B information The Disable inputs have the additional feature that when both Disable A and Disable B are a logical "1" all outputs go to the High Impedance state. When multiple outputs are connected to a bus line, only one device at a time can be in the normal low impedance state. All others should be gated into the high impedance state (Figure 1). The selected device therefore has the normal TTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current of the selected device is 13 times that of a conventional Series 54/74 device (5.2 mA vs 400 μA), the output is easily able to supply that leakage current to as many as 127 other DM7230/DM8230's and still have available drive for the bus-line. (Figure 2)

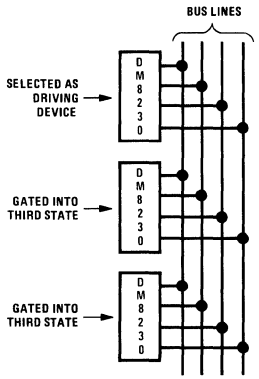


Figure 1

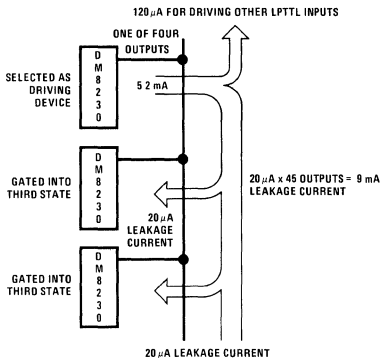


Figure 2

Series 54/74

DM7280/DM8280(S8280/N8280) presettable decade counter
DM7281/DM8281(S8281/N8281) presettable binary counter
DM7288/DM8288(S8288/N8288) presettable ÷12 counter

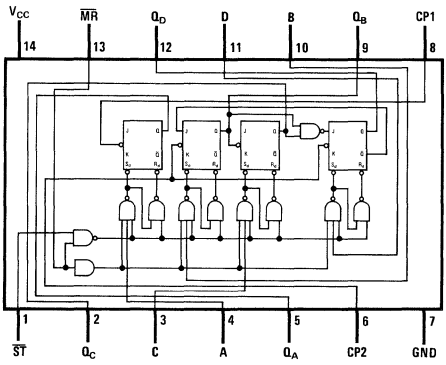
general description

The counters in this series are four-bit monolithic subsystems containing a divide-by-two counter with one clock input and a second counter with a second clock input. The two clock inputs and the other logic functions provided will implement a wide variety of counter and storage register functions.

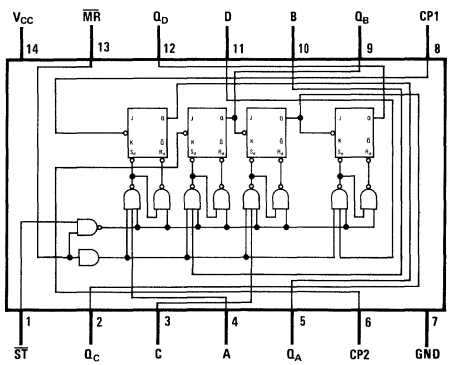
features

- Series 54/74 compatible
- Two clock inputs for additional flexibility
- Strobed parallel-entry capability
- Reset inputs common to all stages
- Typical toggle rates to 45 MHz
- Typical power dissipation of 130 mW
- Direct-coupled stages
- Available in cavity or molded DIP

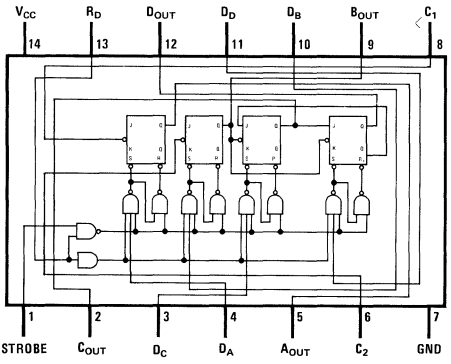
connection diagrams (Dual-In-Line and Flat Packages)



DM7280/DM8280



DM7281/DM8281



DM7288/DM8288

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7280, DM7281, DM7288	−55°C to +125°C
DM8280, DM8281, DM8288	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1, 2)

CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	LIMITS UNITS	TEMP	V_{CC}	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS
"1" Output Voltage[3] [4]	2 6			V	0°C	4 75V	0 8V	2 0V	2 0V		Output A	−200 μA
	2 8			V	+25°C	5 0V	0 8V	2 0V	2 0V		Output A	−200 μA
	2 6			V	+75°C	4 75V	0 8V	2 0V	2 0V		Output A	−200 μA
"0" Output Voltage[3] [5]			0 4	V	0°C	4 75V	0 8V	0 8V	0 8V		Output A	6 4 mA
			0 4	V	+25°C	5 0V	0 8V	0 8V	0 8V		Output A	6 4 mA
			0 4	V	+75°C	4 75V	0 8V	0 8V	0 8V		Output A	6 4 mA
"0" Input Current												
Data Strobe	−0 1		−1 6	mA	+25°C	5 25V	0 4V					
Data Inputs	−0 1		−1 2	mA	+25°C	5 25V		0 4V				
Reset (DM8280, DM8281)	−0 1		−3 0	mA	+25°C	5 25V			0 4V			
Reset (DM8288)	−0 1		−2 8	mA	+25°C	5 25V			0 4V			
$Clock_1$ (DM8280, DM8281)	−0 1		−3 2	mA	+25°C	5 25V				0 4V		
$Clock_1$ (DM8288)	−0 1		−1 6	mA	+25°C	5 25V				0 4V		
$Clock_2$ (DM8280)	−0 1		−3 2	mA	+25°C	5 25V					0 4V	
$Clock_2$ (DM8281, DM8288)	−0 1		−1 6	mA	+25°C	5 25V					0 4V	
"1" Input Current												
Data Strobe			25	μA	+75°C	5 0V	4 5V					
Data Input			25	μA	+75°C	5 0V		4 5V				
Reset (DM8280, DM8281)			75	μA	+75°C	5 0V			4 5V			
Reset (DM8288)			50	μA	+75°C	5 0V			4 5V			
$Clock_1$			75	μA	+75°C	5 0V				4 5V		
$Clock_2$			75	μA	+75°C	5 0V					4 5V	
Clock Mode T_{ON} Delay												
Bit A			25	ns	+25°C	5 0V						6 4 mA
Bit B, C, D			25	ns	+25°C	5 0V						
Clock Mode T_{OFF} Delay												
Bit A			25	ns	+25°C	5 0V						6 4 mA
Bit B, C, D			25	ns	+25°C	5 0V						
Data/Strobe T_{ON} Delay												
Bit A, B, C, D			35	ns	+25°C	5 0V						6 4 mA
Data/Strobe T_{OFF} Delay												
Bit A, B, C, D			45	ns	+25°C	5 0V						6 4 mA
Toggle Rate	20	45		MHz	+25°C	5 0V						6 4 mA
		35		MHz	+25°C	5 0V						6 4 mA
Clock Mode Switching Test[6]			∞	ns	+25°C	5 0V				Pulse	Pulse	
Output Fall Time			50	nA	+25°C	4 75V						100 pF
Power Consumption		130	194	mW	+25°C	5 25V			0V	0V	0V	
Input Voltage Rating												
Data Strobe	5 5			V	+25°C	5 0V	10 mA					
Data Inputs	5 5			V	+25°C	5 0V		10 mA				
Reset	5 5			V	+25°C	5 0V			10 mA			
Output Short Circuit Current	−10		−60	mA	+25°C	5 0V	0V				0V	
Input Capacitance			3 0	pF	+25°C	5 0V						
Strobe Memory Holding Time with "1" to "0" Clock or Output Transition		17	35	ns	+25°C	5 0V		0 8V	2 0V	2 0V	Output A	
With no "1" to "0" Clock or Output Transition		17	35	ns	+25°C	5 0V		2 0V	2 0V	2 0V	Output A	
Strobe Pulse Width	25			ns	+25°C	5 0V		0 8V	2 0V	2 0V	Output A	
Reset Pulse Width	30			ns	+25°C	5 0V	2 0V	0 8V		2 0V	Output A	

Note 1: All voltage and capacitance measurements are referenced to the ground terminal. Terminals that are not specifically referenced are left electrically open.

Note 2: Positive current flow is defined as the current into the referenced terminal.

Note 3: Measurements of each output and the associated data input apply independently.

Note 4: Output source current is supplied through a resistor to ground.

Note 5: Output sink current is supplied through a resistor to V_{CC}.

Note 6: The unit will tolerate any fall time on the clock due to the DC design.

general description (cont.)

The DM7280/DM8280 counter operates as a divide-by-two and divide-by-five counter with no external connections. When the A output is connected to the Clock 2 input, it counts in the familiar BCD mode. The bi-quinary mode is obtained by connecting the D output to the Clock 1 input while applying the clock to the Clock 2 input. This produces a square-wave output at f/10 on the A output that is particularly useful in frequency synthesizers.

The DM7281/DM8281 is a 2,2,4,8 counter when operated with two clock inputs and no external connections. It is a 2,4,8,16 counter when the A output is connected to the Clock 2 input. Thus, it may be used as a divide-by-two, -eight, or -sixteen counter.

The DM7288/DM8288 consists of divide-by-two and divide-by-six counters. For divide-by-twelve operation, output A is connected to the Clock 2 input.

Counting is performed on the negative-going edge of the clock pulse in all three types. The divide-by-two stages may be toggled at up to 45 MHz, typical, approximately twice the maximum frequency of the Clock 2 input.

All three have parallel inputs which may be used to set the corresponding outputs to desired states. The parallel input logic levels are transferred to the outputs when the strobe line is placed at the logical "0" level. A "0" on the reset line will place all four outputs in the "0" state.

The register-storage function can be obtained by using the strobed parallel-entry capability. Data to be stored is entered by the method indicated above and retained on the outputs holding both clock inputs at logical "1" (V_{CC}) The register may be reloaded with a new parallel entry and strobe operation or cleared by the reset line.

Series 54/74

DM74200(SN74200) TRI-STATE® 256-bit random access memory

DM8582 256-bit random access memory (open collector)

general description

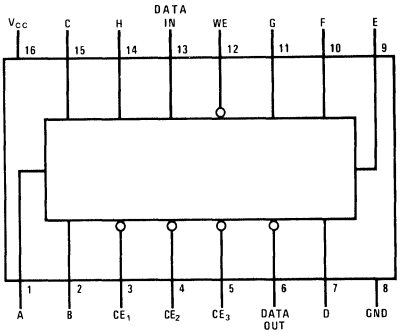
The DM74200 and the DM8582 are 256 x 1 read/write random access. TTL memories which can be used in applications ranging from scratch-pad to main memories. Eight address inputs select the proper bit-location and a Write-Enable input determines whether the read mode or write mode is chosen. Three chip-enable inputs determine whether the output is in the conventional logical "1" or logical "0" state or whether it is gated into the off-state (DM8582) or the high-impedance state DM74200. The off-state and high-impedance states are useful when connection is made to a common bus-line.

features

- 40 ns typical address access time, DM74200
- 50 ns typical address access time, DM8582
- 20 ns typical chip select access time
- <2 mW/bit typical power dissipation

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

CE	WE	OPERATION	OUTPUT (DM8582)	OUTPUT (DM74200)
L	L	Write	Logical "1" (Open Collector)	High Z
L	H	Read	$\overline{D}$ (Complement of Stored Data)	$\overline{D}$ (Complement of Stored Data)
H	L	Do Nothing	Logical "1"	High Z
H	H	Do Nothing	Logical "1"	High Z

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range DM74200, DM8582	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM74200 / DM8582	V_{CC} = 4.75V	2 0			V
Logical "0" Input Voltage	DM74200 / DM8582	V_{CC} = 4 75V			0 8	V
Logical "1" Output Voltage	DM74200	V_{CC} = 4 75V , I_{SOURCE} = 10 mA	2.4			V
Logical "1" Output Current	DM8582	V_{CC} = 5.25V , V_{OUT} = 5 5V			50	μA
Logical "0" Output Voltage	DM74200 / DM8582	V_{CC} = 4 75V , I_{SINK} = 24 mA			0 4	V
Third State Output Current	DM74200	V_{CC} = 5.25V , V_{OUT} = 0 4V or 2 4V	−40		+40	μA
Logical "1" Input Current	DM74200 / DM8582	V_{CC} = 5.25V , V_{IN} = 2.4V , V_{IN} = 5 5V			25 1 0	μA mA
Logical "0" Input Current	DM74200 / DM8582	V_{CC} = 5 25V , V_{IN} = 0 4V			−1 0	mA
Output Short Circuit Current (Note 3)	DM74200	V_{CC} = 5.25V , V_{OUT} = 0V	−40		−80	mA
Supply Current	DM74200 / DM8582	V_{CC} = 5 0V		99 96	130 125	mA mA
Input Clamp Voltage	DM74200 / DM8582	V_{CC} = 4 75V , I_{IN} = −12 mA			−1 5	V
Output V_{CC} Clamp Voltage	DM74200	I_{OUT} = 12 mA			V_{CC} + 1.5	V
Output Ground Clamp Voltage	DM74200	I_{OUT} = 12 mA			−1 5	V
Address Access Time, t_{AA}	DM8582 / DM74200	V_{CC} = 5.0V		50 40		ns ns
Chip Select Access Time, t_{ACS}				20		ns
Chip Select Recovery Time, t_{RCS}		T_A = 25°C		20		ns
Write Enable Pulsewidth, t_{WP}		R_L = 300Ω		25		ns
Sense Recovery Time, t_{SR}		C_L = 30 pF		40		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C range for the DM74200 and DM8582 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Series 54/74

DM7520/DM8520 modulo-n divider

general description

The DM7520/DM8520 combines TTL technology and MSI (Medium Scale Integration) design to provide a circuit equal in complexity to more than 50 gates.

Although extremely versatile in a number of digital applications, its primary usage will be realized in two areas.

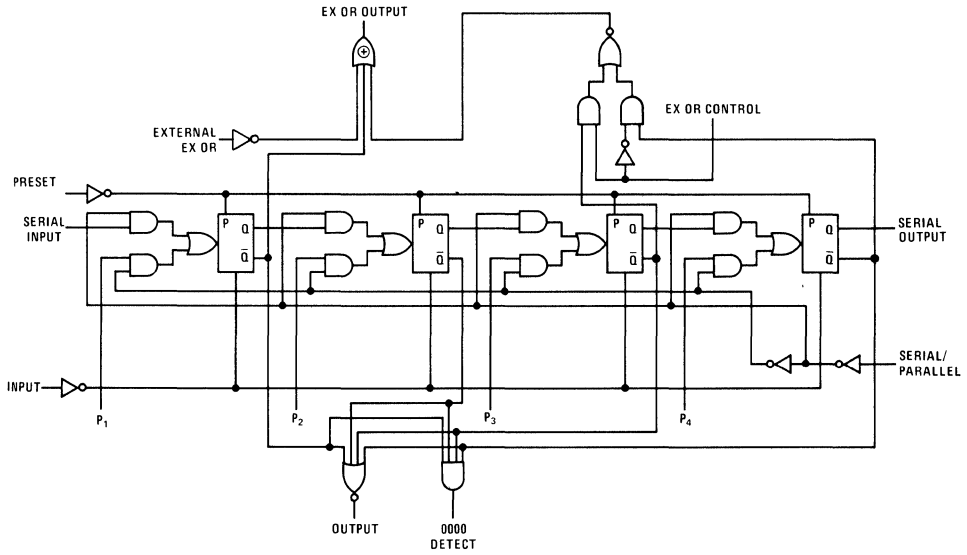
1. MODULO-N DIVIDER

   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.

2. SHIFT REGISTER

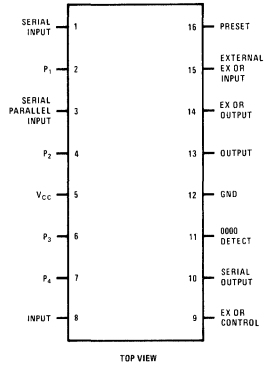
   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial out shifting is required.

logic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

table for division by n

SETTING				÷BY
P_1	P_2	P_3	P_4	
1	1	1	0	2
1	1	0	0	3
1	0	0	0	4
0	0	0	1	5
0	0	1	0	6
0	1	0	0	7
1	0	0	1	8
0	0	1	1	9
0	1	1	0	10
1	1	0	1	11
1	0	1	0	12
0	1	0	1	13
1	0	1	1	14
0	1	1	1	15

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM7520	−55°C to +125°C
	DM8520	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7520	V_{CC} = 4.5V		2.0			V
	DM8520	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7520	V_{CC} = 4.5V				0.8	V
	DM8520	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7520	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8520	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7520	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8520	V_{CC} = 4.75V					
Logical "0" Input Current (All inputs except pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM8520	V_{CC} = 5.25V					
Logical "0" Input Current (Pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 0.4V			−3.2	μA
	DM8520	V_{CC} = 5.25V					
Logical "1" Input Current	DM7520	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8520	V_{CC} = 5.25V					
Logical "1" Input Current (Pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM8520	V_{CC} = 5.25V					
Logical "1" Input Current (All inputs except pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8520	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7520	V_{CC} = 5.5V	V_{OUT} = 0V (Note 2)	−20		55	mA
	DM8520	V_{CC} = 5.25V		−18			
Power Supply Current		V_{CC} = 5.0V	T_A = 25°C		50		mA
Counting Frequency		V_{CC} = 5.0V	T_A = 25°C		20		MHz

Note 1: Unless otherwise specified, limits shown apply across the −55°C to +125°C temperature range for the DM7520 and the 0°C to +70°C temperature range for the DM8520. Typical values apply to supply voltages of 5.0V.

Note 2: Only one output should be shorted at a time.

Note 3: Serial and exclusive OR outputs.

theory of operation

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is 2^n-1, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence, this state is detected; and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16-m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidently set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Other connections are shown. (Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255. For division by higher numbers, a more complete discussion of the interconnection techniques will be given in the final data sheet.)

To divide by numbers between 16 and 255, the table in Figure 2 will apply.

Thus to summarize, the following connections should be made for operation of a single DM7520/DM8520.

Ex-Or Output to Serial Input
0000 Detect to External Ex-Or Input
Output to Serial/Parallel Input
Preset to Ground
Ex-Or Control to Ground

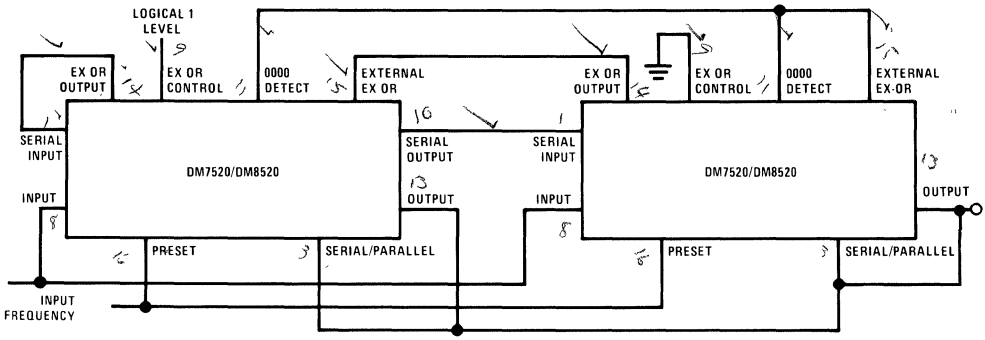


FIGURE 1. Connection for 2 Divider or Maximum Frequency Division of 255

SETTING								÷ BY
DIVIDER 1				DIVIDER 2				
P_1	P_2	P_3	P_4	P_1	P_2	P_3	P_4	
0	1	1	1	1	1	1	1	255
1	0	1	1	1	1	1	1	254
0	1	0	1	1	1	1	1	253
0	0	1	0	1	1	1	1	252
1	0	0	1	0	1	1	1	251
0	1	0	0	1	0	1	1	250
0	0	1	0	0	1	0	1	249
0	0	0	1	0	0	1	0	248
0	0	0	0	1	0	0	1	247
0	0	0	0	0	1	0	0	246
0	0	0	0	0	0	1	0	245
0	0	0	0	0	0	0	1	244
1	0	0	0	0	0	0	0	243
1	1	0	0	0	0	0	0	242
1	1	1	0	0	0	0	0	241
0	1	1	1	0	0	0	0	240
1	0	1	1	1	0	0	0	239
1	1	0	1	1	1	0	0	238
0	1	1	0	1	1	1	0	237
0	0	1	1	0	1	1	1	236
0	0	0	1	1	0	1	1	235
0	0	0	0	1	1	0	1	234
0	0	0	0	0	1	1	0	233
0	0	0	0	0	0	1	1	232
1	0	0	0	0	0	0	1	231
0	1	0	0	0	0	0	0	230
0	0	1	0	0	0	0	0	229
1	0	0	1	0	0	0	0	228
1	1	0	0	1	0	0	0	227
0	1	1	0	0	1	0	0	226
1	0	1	1	0	0	1	0	225
0	1	0	1	1	0	0	1	224
0	0	1	0	1	1	0	0	223
0	0	0	1	0	1	1	0	222
0	0	0	0	1	0	1	1	221
0	0	0	0	0	1	0	1	220
1	0	0	0	0	0	1	0	219
1	1	0	0	0	0	0	1	218
0	1	1	0	0	0	0	0	217
1	0	1	1	0	0	0	0	216
0	1	0	1	0	0	0	0	215
1	0	1	0	1	1	0	0	214
1	1	0	1	0	1	1	0	213
1	1	1	0	1	0	1	1	212
0	1	1	1	0	1	0	1	211
0	0	1	1	1	0	1	0	210
0	0	0	1	1	1	0	1	209
0	0	0	0	1	1	1	0	208
1	0	0	0	0	1	1	1	207
0	1	0	0	0	0	1	1	206
1	0	1	0	0	0	0	1	205
1	1	0	1	0	0	0	0	204
1	1	1	0	1	0	0	0	203
1	1	1	1	0	1	0	0	202
0	1	1	1	1	0	1	0	201
0	0	1	1	1	1	0	1	200
1	0	0	1	1	1	1	0	199
0	1	0	0	1	1	1	1	198
0	0	1	0	0	1	1	1	197
0	0	0	1	0	0	1	1	196
1	0	0	0	1	0	0	1	195
1	1	0	0	0	1	0	0	194
1	1	1	0	0	0	1	0	193
0	1	1	1	0	0	0	1	192
0	0	1	1	1	0	0	0	191
0	0	0	1	1	1	0	0	190
1	0	0	0	1	1	1	0	189
0	1	0	0	0	1	1	1	188
1	0	1	0	0	0	1	1	187
1	1	0	1	0	0	0	1	186
0	1	1	0	1	0	0	0	185
0	0	1	1	0	1	0	0	184
1	0	0	1	1	0	1	0	183
0	1	0	0	1	1	0	1	182
0	0	1	0	0	1	1	0	181
1	0	0	1	0	0	1	1	180
0	1	1	0	0	1	0	0	179
0	0	1	0	0	0	1	0	178
1	0	0	1	0	0	0	1	177
1	1	0	0	1	0	0	0	176
1	1	1	0	0	1	0	0	175
0	1	1	1	0	0	1	0	174
1	0	1	1	1	0	0	1	173
0	1	0	1	1	1	0	0	172
1	0	1	0	1	1	1	0	171
1	1	0	1	0	1	1	1	170
0	1	1	0	1	0	1	1	169
1	0	1	1	0	1	0	1	168
1	1	0	1	1	0	1	0	167
0	1	1	0	1	1	0	1	166
1	0	1	1	0	1	1	0	165
0	1	0	1	1	0	1	1	164
0	0	1	0	1	1	0	1	163
0	0	0	1	1	1	1	0	162
1	1	0	0	1	0	1	1	161
0	0	1	1	0	0	1	1	160
0	0	0	0	1	1	1	1	159
0	0	0	0	0	1	1	1	158
1	0	0	0	0	0	1	1	157
0	1	0	0	0	0	0	1	156
1	0	1	0	0	0	0	0	155
0	1	0	1	0	0	0	0	154
0	0	1	0	1	0	0	0	153
0	0	0	1	0	1	0	0	152
0	0	0	0	1	0	1	0	151
1	0	0	0	0	1	0	1	150
0	1	0	0	0	0	1	0	149
0	0	1	0	0	0	0	1	148
0	0	0	1	0	0	0	0	147
0	0	0	0	1	0	0	0	146
1	0	0	0	0	1	0	0	145
1	1	0	0	0	0	1	0	144
1	1	1	0	0	0	0	1	143
1	1	1	1	0	0	0	0	142
0	1	1	1	1	0	0	0	141
0	0	1	1	1	1	0	0	140
0	0	0	1	1	1	1	0	139
1	0	0	0	1	1	1	1	138
1	1	0	0	0	1	1	1	137
0	1	1	0	0	0	1	1	136
0	0	1	1	0	0	0	1	135
0	0	0	1	1	0	0	0	134
1	0	0	0	1	1	0	0	133
0	1	0	0	0	1	1	0	132
0	0	1	0	0	0	1	1	131
0	0	0	1	0	0	0	1	130
1	0	0	0	1	0	0	0	129
0	1	0	0	0	1	0	0	128
0	0	1	0	0	0	1	0	127
1	0	0	1	0	0	0	1	126
0	1	0	0	1	0	0	0	125
1	0	1	0	0	1	0	0	124
0	1	0	1	0	0	1	0	123
0	0	1	0	1	0	0	1	122
1	0	0	1	0	1	0	0	121
1	1	0	0	1	0	1	0	120
0	1	1	0	0	1	0	1	119
0	0	1	1	0	0	1	0	118
1	0	0	1	1	0	0	1	117
1	1	0	0	1	1	0	0	116
1	1	1	1	0	0	1	1	115
0	1	1	0	0	1	1	0	114
1	0	1	1	0	0	1	1	113
1	1	0	1	1	0	0	1	112
1	1	1	0	1	1	0	0	111
0	1	1	1	1	0	1	1	110
1	0	1	1	1	1	0	1	109
0	1	0	1	1	1	1	0	108
1	0	1	0	1	1	1	1	107
0	1	0	1	0	1	1	1	106
1	0	1	0	1	0	1	1	105
0	1	0	1	0	1	0	1	104
1	0	1	0	1	0	1	0	103
1	1	0	1	0	1	0	1	102
0	1	1	0	1	0	1	0	101
0	0	1	1	0	1	0	1	100
0	0	0	1	1	0	1	0	99
1	0	0	0	1	1	0	1	98
1	1	0	0	0	1	1	0	97
1	1	1	0	0	0	1	1	96
1	1	1	1	0	0	0	1	95
1	1	1	1	1	0	0	0	94
1	1	1	1	1	1	0	0	93
1	1	1	1	1	1	1	0	92

FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations)

Series 54/74

DM7551/DM8551 TRI-STATE® quad D flip flop

general description

The DM7551/DM8551 is a TRI-STATE logic device which provides four D-type flip flops in one package which operate synchronously from a common clock.

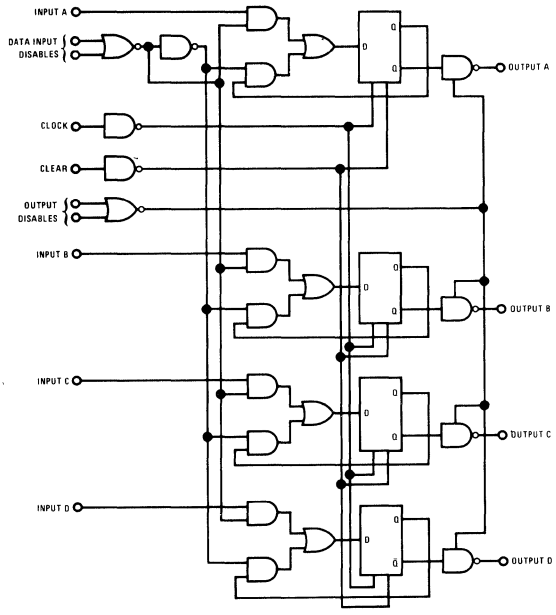
features

- Series 54/74 compatible
- 23 ns typical propagation delay
- 250 mW typical power dissipation
- Outputs directly connectable for bus-line operation
- A "do-nothing" state accomplished without gating the clock
- Simple disable encoding

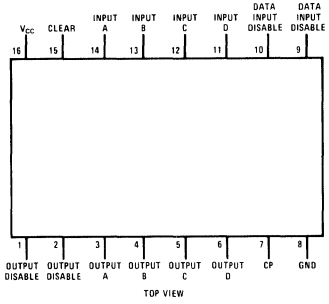
A unique three-state output allows the device to be used in bus-organized systems. The outputs can be directly wired to outputs of other DM7551/DM8551's without encountering the problems normally met with "collector-ORing" TTL circuits. This is accomplished by gating the normally low impedance logical "1" or logical "0" output into a high impedance state.

(Continued)

logic and connection diagrams



Dual-In-Line and Flat Package



truth table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logical "1" on 1 or both inputs	X	Qn
Logical "0" on both inputs	1	1
Logical "0" on both inputs	0	0

X = Don't Care

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5 5V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7551	−55°C to +125°C
	DM8551	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C
Time that two bus-connected devices may be in opposite low impedance states simultaneously		Indefinitely

electrical characteristics (Note 2)

PARAMETERS		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7551	V_{CC} = 4 5V		2 0			V
	DM8551	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM7551	V_{CC} = 4 5V				0 80	V
	DM8551	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM7551	V_{CC} = 4 5V	I_{OUT} = −2 0 mA	2 4	3 3		V
	DM8551	V_{CC} = 4 75V	I_{OUT} = −5 2 mA				
Logical "0" Output Voltage	DM7551	V_{CC} = 4 5V	I_{OUT} = 16 mA		0 2	0 40	V
	DM8551	V_{CC} = 4 75V					
Logical "0" Input Current	DM7551	V_{CC} = 5 5V	V_{IN} = 0 40V		−1 0	−1 6	mA
	DM8551	V_{CC} = 5 25V					
Logical "1" Input Current	DM7551	V_{CC} = 5 25V	V_{IN} = 2 4V			40	µA
	DM8551	V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Output Current In High Impedance State	DM7551	V_{CC} = 5 5V	V_O = 2 4V			40	µA
	DM8551	V_{CC} = 5 25V	V_O = 0 4V			−40	µA
Supply Current	DM7551	V_{CC} = 5 5V			50	72	mA
	DM8551	V_{CC} = 5 25V					
Output Short Current (Note 3)	DM7551	V_{CC} = 5 5V	V_{OUT} = 0 0V	−30		−70	mA
	DM8551	V_{CC} = 5 25V					
Maximum Clock Frequency		V_{CC} = 5 0V, C_L = 50 pF	T_A = 25°C	25	30		MHz
Propagation Delay from Clock to Logical "0", t_{pd0}		V_{CC} = 5 0V, C_L = 50 pF	T_A = 25°C	11	20	28	ns
Propagation Delay from Clock to Logical "1", t_{pd1}		V_{CC} = 5 0V, C_L = 50 pF	T_A = 25°C	11	16	25	ns
Input Data Setup Time, $t_{S\,DATA}$		V_{CC} = 5 0V	T_A = 25°C		3	10	ns
Input Data Hold Time, $t_{H\,DATA}$		V_{CC} = 5 0V	T_A = 25°C		4	10	ns
Input Disable Setup Time, $t_{S\,DIS}$		V_{CC} = 5 0V	T_A = 25°C		7	14	ns
Input Disable Hold Time, $t_{H\,DIS}$		V_{CC} = 5 0V	T_A = 25°C		−7		ns
Delay from "Output Disable" to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0V	T_A = 25°C	3	5	30	ns
Delay from "Output Disable" to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V	T_A = 25°C	3	11	30	ns
Delay from "Output Disable" to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5 0V	T_A = 25°C	7	16	30	ns
Delay from "Output Disable" to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5 0V	T_A = 25°C	7	21	30	ns
Propagation Delay from Clear to Output, t_{pdR}		V_{CC} = 5 0V	T_A = 25°C		18	27	ns

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range", they are not meant to imply operating conditions

Note 2: Unless otherwise specified the min-max limits across the −55°C to +125°C temperature range for the DM7551 and across the 0°C to 70°C temperature range for the DM8551 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only 1 output at a time should be shorted

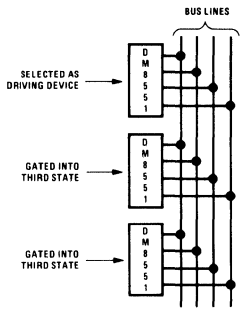


FIGURE 1

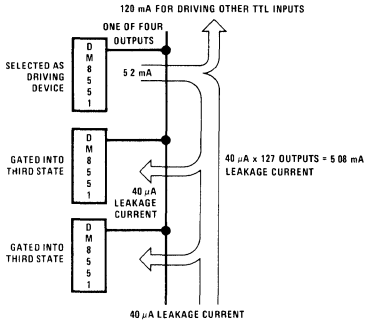


FIGURE 2

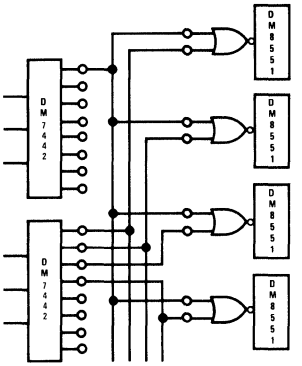


FIGURE 3

general description (cont.)

The high impedance state occurs on all outputs of all devices except the four outputs of the one device selected (Figure 1). The result is that the selected device has a normal TTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from a logical "0" to a logical "1". The other outputs are all in the "third-state" and take only a small amount of leakage current from the driving outputs. Since the logical "1" output current of the selected device is 13 times that of a normal Series 54/74 output (5.2 mA vs 400 μA), the output is easily able to supply that leakage current to as many as 127 connected devices and still retain enough drive for a full Series 54/74 fan-out of 3 at the end of the bus line (Figure 2).

A two-input NOR gate facilitates selection of the driving device through the use of only two octal decoders for as many as 64 DM7551/DM8551's (Figure 3).

A problem inherent in conventional D-type flip flops is that it is impossible to code the data input in such a way as to cause the flip flop to remain in its present state when clocked. Because flexibility is not as great as with a J-K flip flop (and its J=0, K=0 state), to keep a D-type flip flop in its present state it is usually necessary to gate the clock, which increases the danger of false-clocking. The DM7551/DM8551 contains a gated input disable which does not disrupt clocking, but rather recirculates information from the Q output to the D input. In this manner the flip flop does not change state and the possibility of false-clocking is eliminated.

The following logic levels control the device.

- Clocking occurs on the positive-going transition.
- Clearing is enabled by taking the input to a Logical "1" level.
- Outputs are placed in the "third-state" if either of the two Output Disable inputs is taken to a Logical "1" level.
- The flip flops will remain in their previous state when clocked so long as either of the two Data Input Disable inputs is taken to a Logical "1" level.

The DM7551/DM8551 is completely compatible with other Series 54/74 devices.

Series 54/74

DM7552/DM8552 TRI-STATE® decade counter/latch
DM7554/DM8554 TRI-STATE binary counter/latch

general description

The DM7552/DM8552 and DM7554/DM8554 are TTL TRI-STATE Synchronous Decode and Binary counter/latch circuits respectively. The circuits consist of a counter made up of four edge-triggered JK flip-flops.

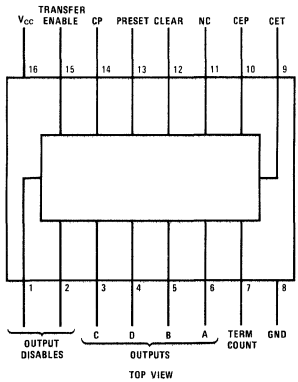
features

- Series 54/74 compatible
- 330 mW typical power dissipation
- TRI-STATE outputs directly connectable for bus-line operation
- TRI-STATE outputs information may be latched
- 30 ns typical propagation delay
- Count mode and Terminal Count output are operable when the outputs are in the high impedance state or latch mode
- Blanking capability with the DM7552/DM8552
- Positive true logic

The circuits logically combine the function of counters for frequency division, latches to hold the counter's information, and output buffer gates which allow active TTL outputs as well as the high impedance (3rd) state for output multiplexing of data.

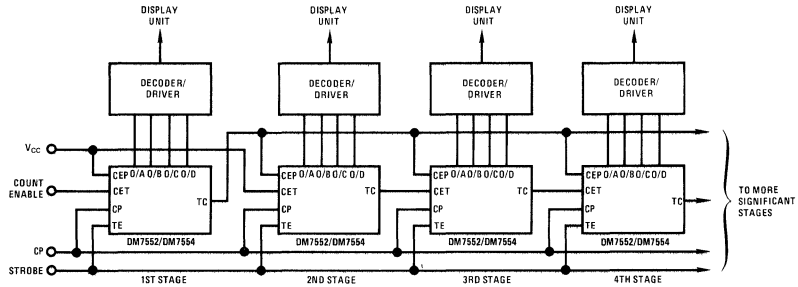
connection diagram

Dual-In-Line and Flat Package



typical application

Multi-Stage Synchronous Counter with Visual Display



Counter stages can be cascaded as shown above to provide multiple stage BCD or binary synchronous counting by using the DM7552/DM8552 or the DM7554/DM8554 respectively. With a Terminal Count (TC) fan out of six the above scheme allows seven stages to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the strobe line while the counters can continue counting. The display can be updated by applying a positive pulse to the strobe line.

absolute maximum ratings (Note 1)

Supply Voltage	7 0V
Input Voltage	5 5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7552/54	4 5	5 5	V
DM8552/54	4 75	5 25	V
Temperature (T_A)			
DM7552/54	−55	+125	°C
DM8552/54	0	70	°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2 0			V
Logical "0" Input Voltage				0 8	V
Logical "1" Output Voltage TC Output	I_{OUT} = −0 4 mA	2 4	3 3		V
Logical "1" Output Voltage (Other Outputs)	I_{OUT} = −2 mA (DM7552/54) I_{OUT} = −5 2 mA (DM8552/54)	2 4	3.3		V
Logical "0" Output Voltage	I_{OUT} = 16 mA		0 2	0 4	V
Third State Output Current	V_{OUT} = 0.4V to 2.4V			±40	μA
Logical "1" Input Current "CET"	V_{IN} = 2.4V V_{IN} = 5 5V			80 2	μA mA
"Other Inputs"	V_{IN} = 2.4V V_{IN} = 5 5V			40 1	μA mA
Logical "0" Input Current "CET"	V_{IN} = 0 4V		−2 0	−3 2	mA
"Other Inputs"	V_{IN} = 0 4V		−1.0	−1.6	mA
Output Short Circuit Current (Note 3)					
TC Output	V_{OUT} = 0V	−20		−55	mA
Other Outputs	V_{OUT} = 0V	−30		−70	mA
Supply Current (each device) I_{CC} (max)			66	106	mA
Input Clamp Voltage	I_{IN} = −12 mA			−1.5	V
Output V_{CC} Clamp Voltage	V_{CC} = 0V I_{OUT} = 12 mA			1 5	V
Output Ground Clamp Voltage	V_{CC} = 0V I_{OUT} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Clock to Any Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		23	45	ns
Propagation Delay to a Logical "1" from Clock to Any Output, t_{pd1}	V_{CC} = 5 0V T_A = 25°C		34	70	ns
Propagation Delay from TE to Output, t_{pd}(TE)	V_{CC} = 5.0V T_A = 25°C		26	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7552/DM7554 and across the 0°C to 70°C range for the DM8552/DM8554. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

electrical characteristics (cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Delay from Output Disable to High Impedance State (from Logical "1" Level), t_{1H}	V_{CC} = 5.0 T_A = 25°C		27	8	ns
Delay from Output Disable to High Impedance State (from Logical "0" Level), t_{0H}	V_{CC} = 5.0 T_A = 25°C		17	40	ns
Delay from Output Disable to Logical "1" Level (from High Impedance State), t_{H1}	V_{CC} = 5 0 T_A = 25°C		21	45	ns
Delay from Output Disable to Logical "0" Level (from High Impedance State), t_{H0}	V_{CC} = 5.0 T_A = 25°C		25	50	ns
Maximum Clock Frequency	V_{CC} = 5.0 T_A = 25°C	15	23		MHz

mode of operation

When the Transfer Enable (TE) is at a logical "1" level the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable (TE) is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear (CL) resets the counter to 0000.

Asynchronous Preset (PRE) resets the counter to 1111.

The 1111 state may be used in the DM7552/DM8552 for blanking out leading zeroes in visual displays. The next clock pulse will advance the DM7552/DM8552 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the DM7554/DM8554 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

DM7552/DM8552 $TC = CET \cdot A \cdot \overline{B} \cdot \overline{C} \cdot D$

DM7554/DM8554 $TC = CET \cdot A \cdot B \cdot C \cdot D$

The following logic levels control the device:

- The counter changes state on the positive-going transition of the clock.
- Clearing or Presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "Third-State" either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique (see application).

logic tables

FUNCTION TABLE

INPUTS							OUTPUTS				
OD1	OD2	CEP	CET	CLEAR	PRESET	TE	A	B	C	D	TC
1	X	X	X	X	X	X	"High Impedance State"				*
X	1	X	X	X	X	X	"High Impedance State"				*
0	0	X	X	1	X	1	0	0	0	0	0
0	0	X	X	0	1	1	1	1	1	1	*
0	0	X	X	X	X	0	LATCH				*
0	0	1	1	0	0	1	COUNT				*

*Function of the count sequence

DM7552/DM8552 DECADE COUNT SEQUENCE

COUNT	OUTPUTS				
	A	B	C	D	TC
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
3	1	1	0	0	0
4	0	0	1	0	0
5	1	0	1	0	0
6	0	1	1	0	0
7	1	1	1	0	0
8	0	0	0	1	0
9	1	0	0	1	1
**If Preset Applied Next Count	1	1	1	1	0
	1	0	0	0	0

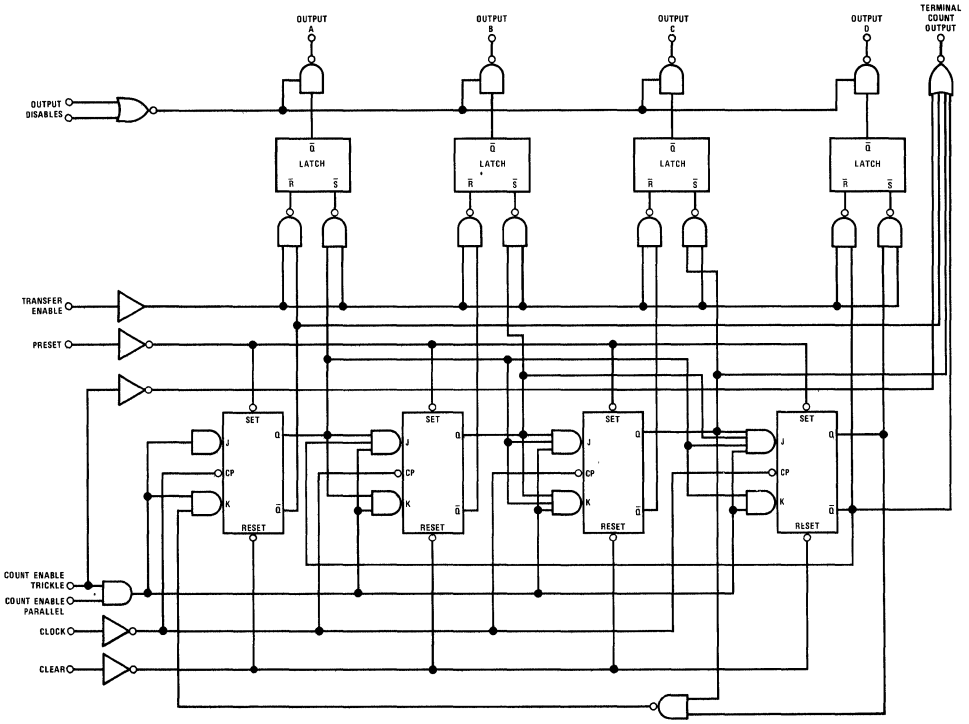
**The 1111 state may be used in conjunction with certain decoder/drivers i e DM5446, DM5447 and DM5448 for blanking leading zeroes

DM7554/DM8554 BINARY COUNT SEQUENCE

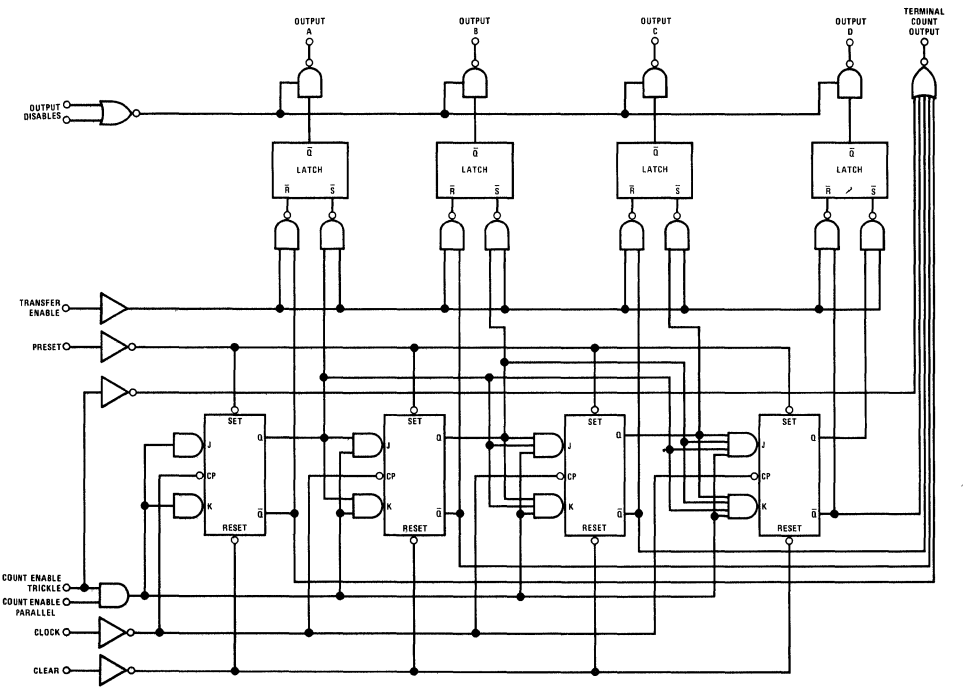
COUNT	OUTPUTS				
	A	B	C	D	TC
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
3	1	1	0	0	0
4	0	0	1	0	0
5	1	0	1	0	0
6	0	1	1	0	0
7	1	1	1	0	0
8	0	0	0	1	0
9	1	0	0	1	0
10	0	1	0	1	0
11	1	1	0	1	0
12	0	0	1	1	0
13	1	0	1	1	0
14	0	1	1	1	0
15	1	1	1	1	1

logic diagrams

DM7552/DM8552



DM7554/DM8554



Series 54/74

DM7553/DM8553 TRI-STATE® eight bit latch

general description

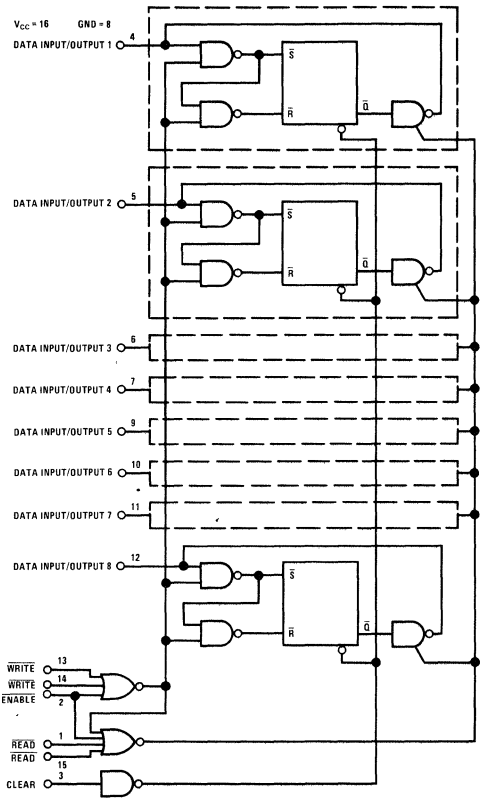
The DM7553/DM8553 provides eight latches whose inputs and outputs are accessed on the same leads. The fact that the outputs utilize TRI-STATE circuitry allows this to be done. While in the high-impedance state, the outputs and inputs are disabled and no information can be entered. When the outputs are active the gating associated with each latch prevents information from being entered. The outputs are disabled while information is entered.

In this manner eight bits of storage can be accomplished with parallel inputs and outputs in a 16-pin package.

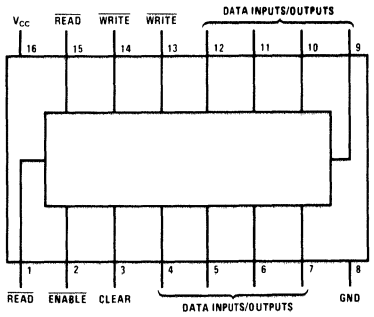
features

- Series 54/74 compatible
- Typical power dissipation 330 mW
- Typical propagation delay 25 ns

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

truth table

CLEAR	ENABLE	READ	WRITE	I/O STATE
1	0	0	X	Output = 0
X	X	1	1	Hi-z
X	1	X	X	
0	0	X	0	Write
0	0	0	1	Read

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V or 0.5V above V_{CC}
Output Voltage	
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7553	4.5	5 5	V
DM8553	4 75	5.25	V
Temperature (T_A)			
DM7553	−55	+125	°C
DM8553	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage, Output Enabled	V_{CC} = Min, I_{OUT} = −2.0 mA (7553), −5 2 mA (8553)	2.4			V
Logical "0" Output Voltage, Output Enabled	V_{CC} = Min, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current, Input Enabled	V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
	V_{IN} = 2.4V			40	μA
Logical "0" Input Current, Input Enabled	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
TRI-STATE I/O Current with Inputs & Outputs Disabled	$V_{I/O}$ = 2.4V or 0 4V			±40	μA
Output Short Circuit Current (Note 3)	V_{CC} = Max, 8553	−28		−70	mA
	V_{CC} = Max, 7553	−30			
Supply Current			66	93	mA
Input/Output V_{CC} Clamp Voltage	V_{CC} = 0V, I_{OUT} = +12 mA			1 5	V
Input/Output Ground Clamp Voltage, Outputs Disabled	V_{CC} = 5V, I_{OUT} = −12 mA			−1.5	V
TRI-STATE OUTPUT CHARACTERISTICS					
Delay from Output to High Impedance State (from Logical "1" Level), t_{1H}	V_{CC} = 5.0V, T_A = 25°C		7	12	ns
Delay from Output to High Impedance State (from Logical "0" Level), t_{0H}	V_{CC} = 5 0V, T_A = 25°C		20	30	ns
Delay from Output to Logical "1" Level (from High Impedance State), t_{H1}	V_{CC} = 5.0V, T_A = 25°C		22	33	ns
Delay from Output to Logical "0" Level (from High Impedance State), t_{H0}	V_{CC} = 5.0V, T_A = 25°C		25	38	ns
Delay from Clear Input to Output = Logical "0", t_{pdR}			21	32	ns
Min Clear Pulse Width Required, t_{rpw}			10	15	ns
Data Setup Time, t_s	Data = 1		14	20	ns
	Data = 0		26	36	ns
Data Hold Time, t_h	Data = 1		−26	−15	ns
	Data = 0		−14	−8	ns
Min Write Pulse Width Required, t_{wpw}			28	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7553 and across the 0°C to 70°C range for the DM8553. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

Series 54/74

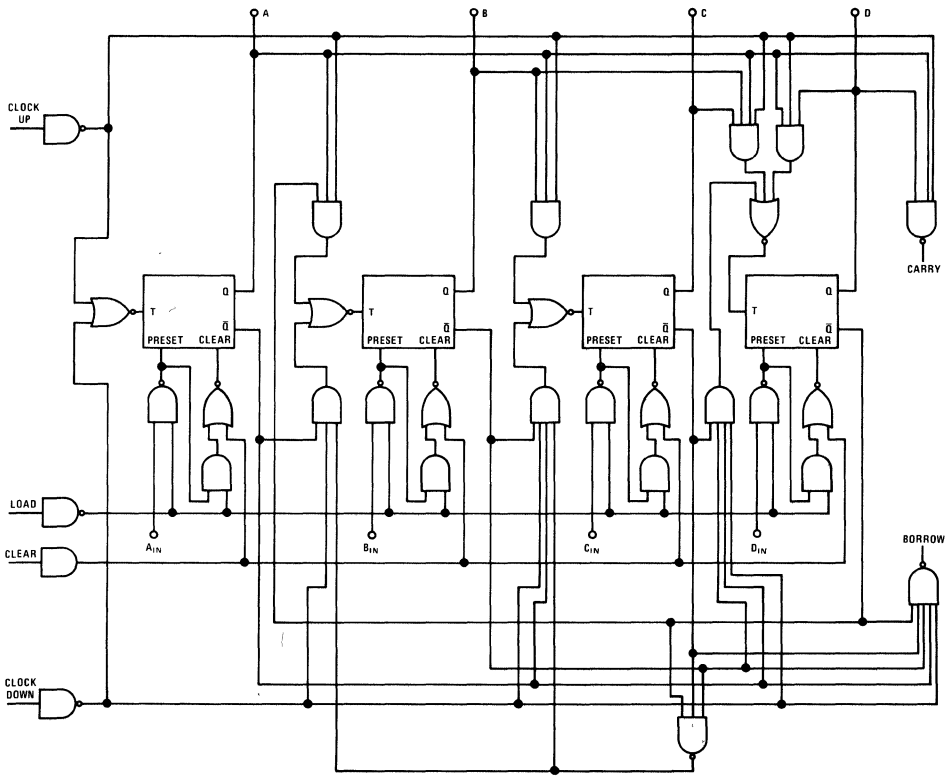
DM7560/DM8560(SN54192/SN74192) up/down decade counter

general description

The DM7560/DM8560 is a TTL, Series 54/74 compatible, up-down decade counter which is capable of being preset to any number from 0 through 9. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines—one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 9. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

logic diagram



absolute maximum ratings

V_{CC}		7 0V
Input Voltage		5 5V
Operating Temperature Range	DM7560	−55°C to +125°C
	DM8560	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Fanout		10
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

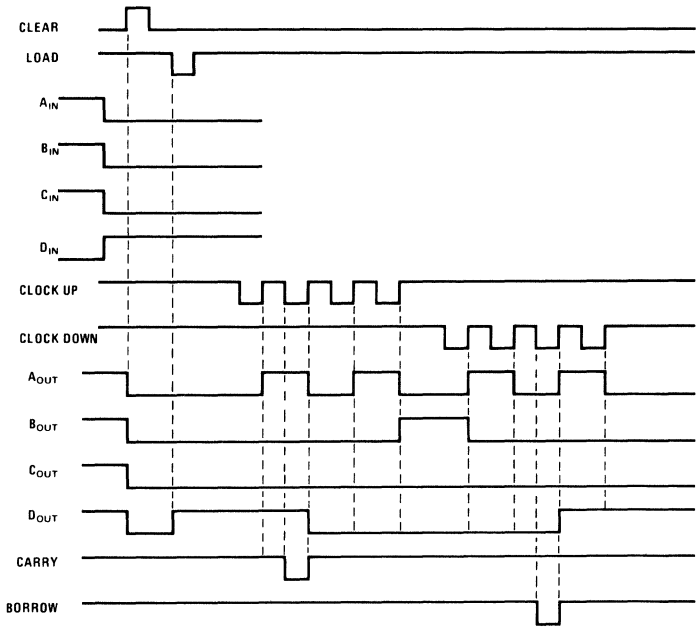
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7560	V_{CC} = 4 5V		2 0			V
	DM8560	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM7560	V_{CC} = 4 5V				0 8	V
	DM8560	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM7560	V_{CC} = 4 5V	I_{OUT} = −400 μA	2 4			V
	DM8560	V_{CC} = 4 75V					
Logical "0" Output Voltage	DM7560	V_{CC} = 4 5V	I_{OUT} = 16 mA			0 4	V
	DM8560	V_{CC} = 4.75V					
Logical "1" Input Current (All Inputs)	DM7560	V_{CC} = 5 5V	V_{IN} = 2 4V			40	μA
	DM8560	V_{CC} = 5 25V					
Logical "1" Input Current (All Inputs)	DM7560	V_{CC} = 5.5V	V_{IN} = 5 5V			1	mA
	DM8560	V_{CC} = 5.25V					
Logical "0" Input Current	DM7560	V_{CC} = 5 5V	V_{IN} = 0 4V			−1.6	mA
	DM8560	V_{CC} = 5 25V					
Output Short Circuit Current (Note 2)	DM7560	V_{CC} = 5 5V	V_{OUT} = 0	−20		−55	mA
	DM8560	V_{CC} = 5 25V		−18			
Supply Current	DM7560	V_{CC} = 5 5V			50	89	mA
	DM8560	V_{CC} = 5 25V					
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5 0V	From Clock to Output		27	38	ns
		T_A = 25°C	From Clock to Carry/Borrow		22	30	ns
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5 0V	From Clock to Output		37	47	ns
		T_A = 25°C	From Clock to Carry/Borrow		18	30	ns
Maximum Clock Frequency		V_{CC} = 5.0V, T_A = 25°C		20	30		MHz

Note 1: Specifications apply across −55°C to +125°C temperature range for the DM7560 and 0°C to 70°C for the DM8560 unless otherwise specified. Typicals are given for V_{CC} = 5V and T_A = 25°C only.

Note 2: Only 1 output may be shorted at a time

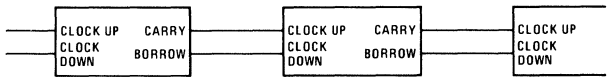
logic waveforms

[Example shown for (1) clearing, (2) asynchronously setting to eight count, (3) counting "up" to two, and (4) counting "down" to eight]



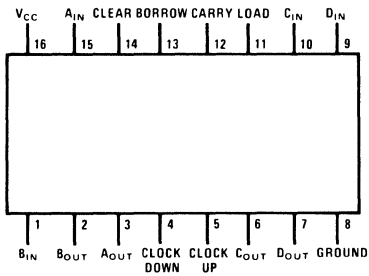
NOTES 1 LOAD AND CLEAR INPUTS SHOULD NEVER BE ENABLED TOGETHER
2 A, B, C AND D INPUTS ARE FREE TO CHANGE AFTER LOAD INPUT IS DISABLED
3 WHEN COUNTING "UP", THE "DOWN" CLOCK MUST BE IN THE LOGICAL 1 STATE, AND CONVERSELY

cascading counters



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Series 54/74

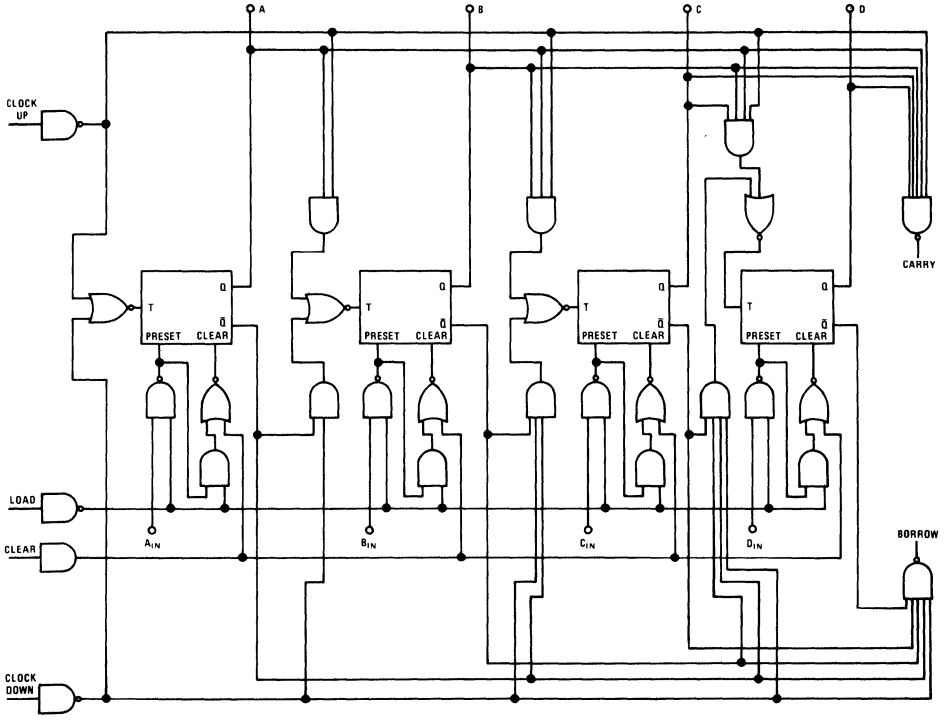
DM7563/DM8563(SN54193/SN74193) up/down binary counter

general description

The DM7563/DM8563 is a TTL, Series 54/74 compatible, up-down binary counter which is capable of being preset to any number from 0 through 15. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines—one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 15. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

logic diagram



absolute maximum ratings

V_{CC}		7 0V
Input Voltage		5 5V
Operating Temperature Range	DM7563	−55°C to +125°C
	DM8563	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Fanout		10
Lead Temperature (Soldering, 10 sec)		300°C

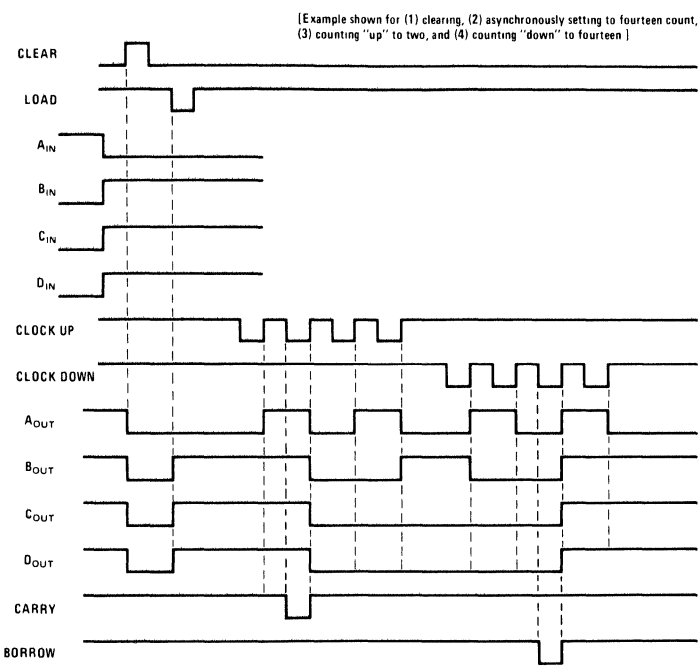
electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7563 / DM8563	V_{CC} = 4 5V / V_{CC} = 4 75V		2.0			V
Logical "0" Input Voltage	DM7563 / DM8563	V_{CC} = 4 5V / V_{CC} = 4 75V				0 8	V
Logical "1" Output Voltage	DM7563 / DM8563	V_{CC} = 4 5V / V_{CC} = 4 75V	I_{OUT} = −400 μA	2 4			V
Logical "0" Output Voltage	DM7563 / DM8563	V_{CC} = 4 5V / V_{CC} = 4 75V	I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current (All Inputs)	DM7563 / DM8563	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			40	μA
Logical "1" Input Current (All Inputs)	DM7563 / DM8563	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	DM7563 / DM8563	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 0 4V			−1.6	mA
Output Short Circuit Current (Note 2)	DM7563 / DM8563	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{OUT} = 0	−20 / −18		−55	mA
Supply Current	DM7563 / DM8563	V_{CC} = 5 5V / V_{CC} = 5 25V			50	89	mA
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	From Clock to Output		27	38	ns
			From Clock to Carry/Borrow		22	30	ns
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	From Clock to Output		37	47	ns
			From Clock to Carry/Borrow		18	30	ns
Maximum Clock Frequency		V_{CC} = 5 0V, T_A = 25°C			30		MHz

Note 1: Specifications apply across −55°C to +125°C temperature range for the DM7563 and 0°C to 70°C for the DM8563 unless otherwise specified Typicals are given for V_{CC} = 5V and T_A = 25°C only

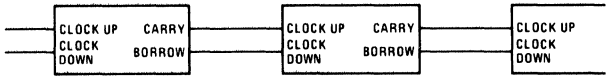
Note 2. Only 1 output may be shorted at a time

logic waveforms



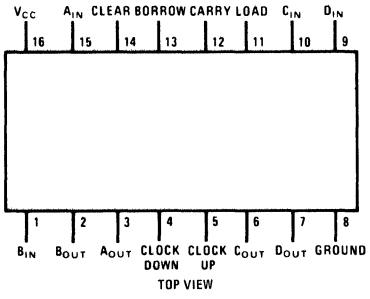
NOTES. 1. LOAD AND CLEAR INPUTS SHOULD NEVER BE ENABLED TOGETHER
2 A, B, C, and D INPUTS ARE FREE TO CHANGE AFTER LOAD INPUT IS DISABLED
3 WHEN COUNTING "UP", THE "DOWN" CLOCK MUST BE IN THE LOGICAL 1 STATE, AND CONVERSELY

cascading counters



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Series 54/74

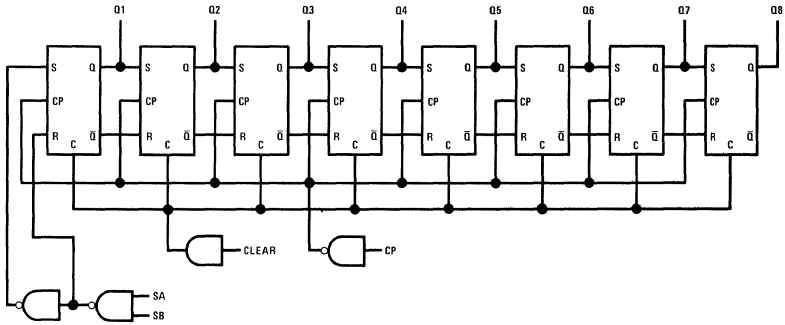
DM7570/DM8570 (SN54164/SN74164)
8-bit serial-in parallel-out shift register

general description

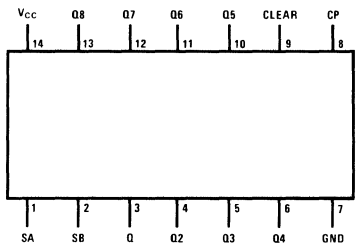
The DM7570/DM8570 utilizes Series 54/74 compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register designed to operate at frequencies of 20 MHz. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical 0, asynchronously sets all flip flops to the logical 0 state

Because the flip flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical 1 levels on SA and SB enter logical 1's into the shift register Clocking occurs on the positive-going edge of the clock pulse.

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Fanout		5
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7570	−55°C to +125°C
	DM8570	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7570	V_{CC} = 4.5V	2.0			V
	DM8570	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7570	V_{CC} = 4.5V			0.8	V
	DM8570	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7570	V_{CC} = 4.5V, I_{OUT} = −200 μA	2.4			V
	DM8570	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM7570	V_{CC} = 4.5V, I_{OUT} = 8 mA			0.4	V
	DM8570	V_{CC} = 4.75V				
Logical "1" Input Current (Except Clear Input)	DM7570	V_{CC} = 5.5V, V_{IN} = 2.4V			40	μA
	DM8570	V_{CC} = 5.25V				
Logical "1" Input Current (Clear Input)	DM7570	V_{CC} = 5.5V, V_{IN} = 2.4V			80	μA
	DM8570	V_{CC} = 5.25V				
Logical "1" Input Current	DM7570	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8570	V_{CC} = 5.25V				
Logical "0" Input Current (Except Clear Input)	DM7570	V_{CC} = 5.5V, V_{IN} = 0.4V			−1.6	mA
	DM8570	V_{CC} = 5.25V				
Logical "0" Input Current (Clear Input)	DM7570	V_{CC} = 5.5V, V_{IN} = 0.4V			−3.2	mA
	DM8570	V_{CC} = 5.25V				
Output Short Circuit Current (Note 2)	DM7570	V_{CC} = 5.5V, V_{OUT} = 0V	−10		−27.5	mA
	DM8570	V_{CC} = 5.25V	−9			
Power Supply Current	DM7570	V_{CC} = 5.5V		36	54	mA
	DM8570	V_{CC} = 5.25V				
Maximum Clock Frequency		V_{CC} = 5.0V, 25°C, 50% Duty Cycle	14	20		mHz
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF	10	28	40	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF	10	28	40	ns
Propagation Delay to a Logical "0" from Clear to Output		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		34	50	ns
Minimum Clock Pulse Width		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		25	45	ns
Minimum Clear Pulse Width		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		30	45	ns
Minimum Time that S_A S_B Data Must be Set-up Prior to Clock Pulse, $t_{set\text{-}up}$		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF, Clock Pulse Width = 50 ns		15	30	ns
Minimum Time that S_A S_B Data Must be Held After Clock Pulse, t_{hold}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF, Clock Pulse Width = 50 ns		−15	0	ns

Note 1 Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7570 and 0°C to +70°C for the DM8570. Typical values apply to supply voltages of 5.0V and 25°C.
Note 2 Only one output should be shorted at a time.

Series 54/74

DM7573/DM8573 1024-bit field-programmable read only memory

general description

The DM7573/DM8573 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs will be turned off. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

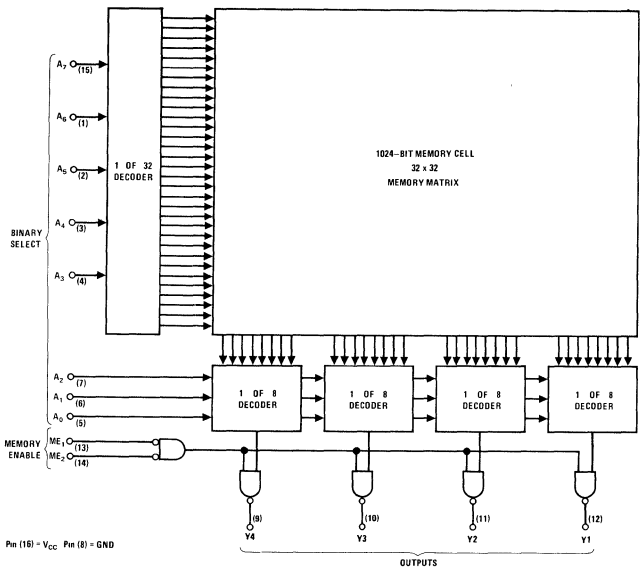
An additional feature of the DM7573/DM8573 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 9V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer returns.

features

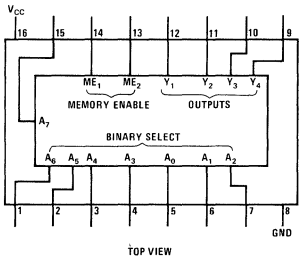
- Can be programmed in 1 sec (50% logical 1's, 50% logical 0's)
- Pin compatible with SN54187/SN74187
- Can be programmed after being connected in a system
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

1

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V (12V on Pins 13, 14)
Output Voltage	5.5V (25V for programming)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7573	4 5	5.5	Volts
DM8573	4.75	5.25	Volts
Temperature (T_A)			
DM7573	−55	+125	°C
DM8573	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Current	V_{CC} = Max, V_O = 4.0V			50	μA
Logical "0" Output Voltage	V_{CC} = Min, I_O = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			40 1	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1	mA
Supply Current	V_{CC} = Max		82	110	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5 0V T_A = 25°C		60		ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		28		ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5.0V T_A = 2.5°C		60		ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}	V_{CC} = 5.0V T_A = 25°C		28		ns

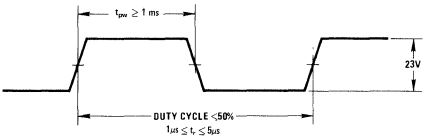
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55° to +125°C temperature range for the DM7573 and across the 0°C to 70°C range for the DM8573. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

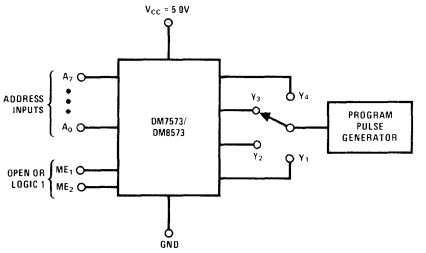
programming procedure

The DM7573/DM8573 is manufactured such that the outputs are high for all addresses. To program a logic zero (low output level), the following procedure should be followed:

1. Apply a V_{CC} voltage of 5.0V and select the word to be programmed using address inputs $A_7 - A_0$.
2. Apply a high level (logic 1) to either or both of the ENABLE inputs (Pins 13 and 14).
3. Apply a programming pulse to the output where a low level is desired. The voltage should be limited to 25V; the current should be limited to 70 mA. Apply the pulse as shown in the diagram. A reduction in current of approximately 15 mA indicates the bit is programmed.
4. To verify that the bit has been programmed, apply a logic zero to both of the enable inputs and check for a low level on the programmed output.
5. Advance to the next output and/or word, programming only one bit at a time.



Programming Pulse



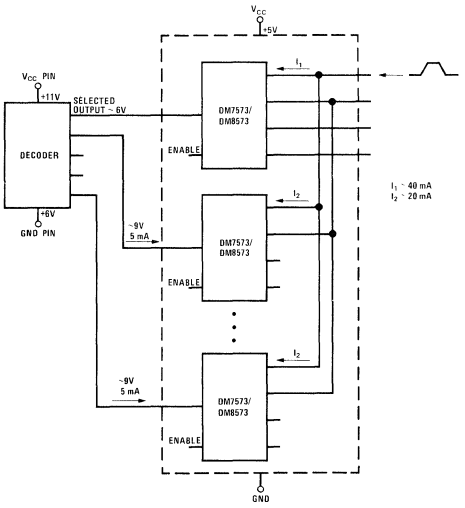
Programming Connections

board programming

The DM7573/DM8573 possesses added flexibility in that it can be programmed *after* it has already been connected in a system. Whether soldered to a printed circuit board or socketed, if the procedure described below is followed the units may be programmed even though their outputs are connected.

As shown in the diagram the decoder used to select the appropriate package must be operated at voltage levels which are 6 volts higher than normal. The outputs of the decoder therefore range between about 6V for a logical "0" and 9V for a logical "1". Because the decoder outputs are active-low, the ENABLE input of the device to be programmed is operated at 6V. The other ENABLE inputs reach 9V, normally a prohibited level, but in this case the circuit was designed to use the 9V to prevent the outputs from being programmed.

Although all common outputs receive the programming pulse, only the memory whose ENABLE input is at the 6V level is programmed.



Series 54/74

DM7574/DM8574 TRI-STATE® 1024-bit field-programmable read only memory

general description

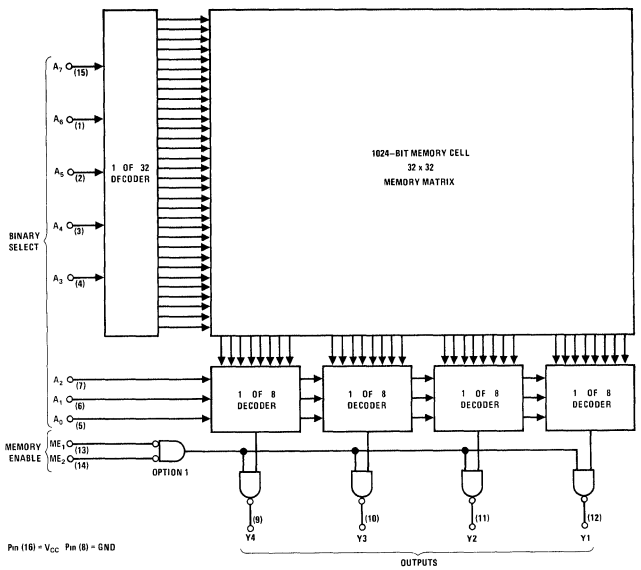
The DM7574/DM8574 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs go to the high impedance state. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

An additional feature of the DM7574/DM8574 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 9V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer returns.

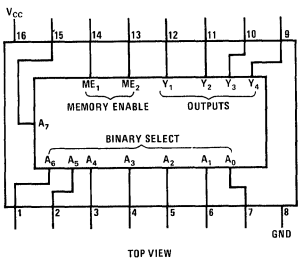
features

- Pin compatible with SN54187/SN74187
- Can be programmed after being connected in a system
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7 0V
Input Voltage	5 5V (12V on Pins 13, 14)
Output Voltage	5 5V (25V for programming)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7574	4 5	5 5	Volts
DM8574	4 75	5 25	Volts
Temperature (T_A)			
DM7574	−55	+125	°C
DM8574	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Max, I_O = −2.0 mA (DM7574) / −5 2 mA (DM8574)	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, I_O = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V V_{CC} = Max, V_{IN} = 5 5V			40 1	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1	mA
Supply Current	V_{CC} = Max		82	110	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5 0V T_A = 25°C		60		ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}	V_{CC} = 5 0V T_A = 25°C		28		ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5.0V T_A = 2 5°C		60		ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}	V_{CC} = 5 0V T_A = 25°C		28		ns

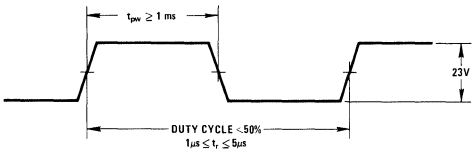
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55° to +125°C temperature range for the DM7574 and across the 0°C to 70°C range for the DM8574. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

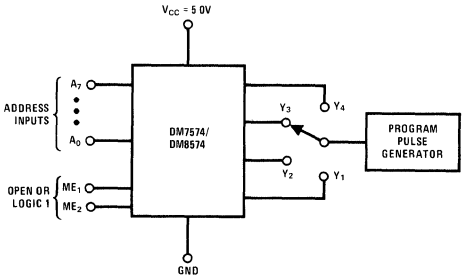
programming procedure

The DM7574/DM8574 is manufactured such that the outputs are high for all addresses. To program a logic zero (low output level), the following procedure should be followed:

1. Apply a V_{CC} voltage of 5.0V and select the word to be programmed using address inputs $A_7 - A_0$.
2. Apply a high level (logic 1) to either or both of the ENABLE inputs (Pins 13 and 14).
3. Apply a programming pulse to the output where a low level is desired. The voltage should be limited to 25V; the current should be limited to 70 mA. Apply the pulse as shown in the diagram. A reduction in current of approximately 15 mA indicates the bit is programmed.
4. To verify that the bit has been programmed, apply a logic zero to both of the enable inputs and check for a low level on the programmed output.
5. Advance to the next output and/or word, programming only one bit at a time.



Programming Pulse



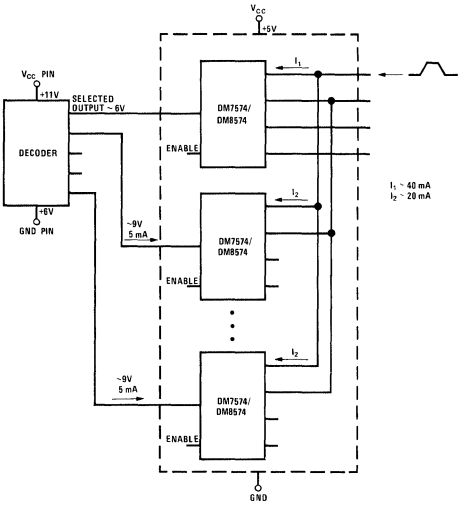
Programming Connections

board programming

The DM7574/DM8574 possesses added flexibility in that it can be programmed *after* it has already been connected in a system. Whether soldered to a printed circuit board or socketed, if the procedure described below is followed the units may be programmed even though their outputs are connected.

As shown in the diagram the decoder used to select the appropriate package must be operated at voltage levels which are 6 volts higher than normal. The outputs of the decoder therefore range between about 6V for a logical "0" and 9V for a logical "1". Because the decoder outputs are active-low, the ENABLE input of the device to be programmed is operated at 6V. The other ENABLE inputs reach 9V, normally a prohibited level, but in this case the circuit was designed to use the 9V to prevent the outputs from being programmed.

Although all common outputs receive the programming pulse, only the memory whose ENABLE input is at the 6V level is programmed.



Series 54/74

DM7575/DM8575, DM7576/DM8576 programmable logic array (PLA)

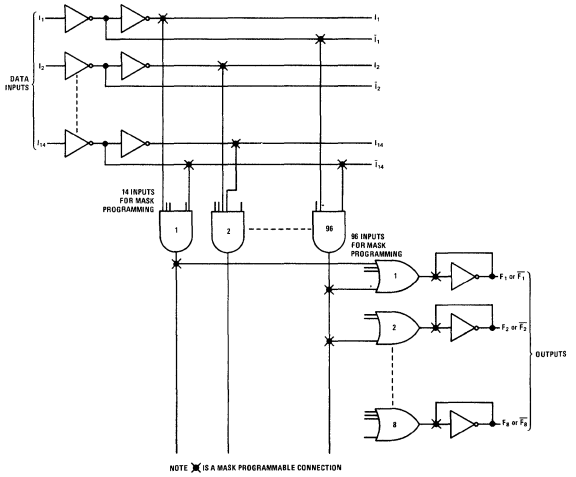
general description

The DM7575/DM8575 and DM7576/DM8576 are mask-programmable logic arrays designed for use in applications where random logic is required. The devices have fourteen data inputs and eight outputs. Each output provides a sum of product terms where each product term can contain any combination of 14 variables or their complements. The total number of product terms which can be provided is 96. Any product term which is repeated is counted only once. Since some functions are more easily represented in their inverted form, an option is provided to allow for either the true or complement of the function on each output. The products are particularly useful in providing control logic for digital systems. The DM7575/DM8575 has a conventional totem-pole output whereas the DM7576/DM8576 is provided with a passive pullup output. This latter configuration is useful in expanding functions by connection of outputs of different packages.

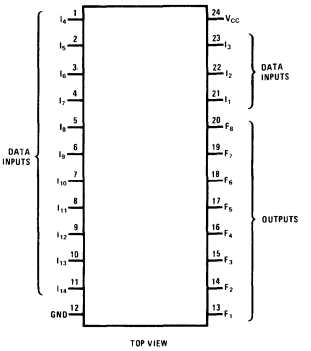
features

- A 2^{14}-by-8 (128k) bit memory would be needed to provide equivalent function
- Typical delay 90 ns
- Typical power dissipation 550 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line Package



absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7575, DM7576	4.5	5.5	V
DM8575, DM8576	4.75	5.25	V
Temperature (T_A)			
DM7575, DM7576	−55	+125	°C
DM8575, DM8576	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Voltage (DM7575/DM8575 Only)	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0 8V, I_{OUT} = −800μA	2 4			V
Logical "1" Output Current (DM7576/DM8576 Only)	V_{CC} = Max, V_{OUT} = 5 5V			100	μA
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0 8V, I_{OUT} = +12 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V V_{IN} = 5 5V			40 1	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 0	mA
Output Short Circuit Current (Note 3) DM7575/76 DM8575/76	V_{CC} = Max, V_{OUT} = 0V	−20/−1 75 −18/−1 65		−55/−3 5 −55/−3 3	mA
Supply Current	V_{CC} = Max		110	170	mA
Input Diode Clamp Voltage	V_{CC} = Min, T_A = 25°C, I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Data Inputs to Outputs, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		100		ns
Propagation Delay to a Logical "1" from Data Inputs to Outputs, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		80		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7575/76 and across the 0°C to 70°C range for the DM8575/76. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

information needed to program the PLA

Information to program the PLA can be supplied in one of two formats

1 Punched 80-column cards

2 The applicable section of this data sheet (manual entry of information)

punched cards

CARD 1. (Used to determine whether outputs are presented in their true or inverted form If this card is not used it is assumed that all eight outputs are true)

Col. 1-6 DM7575 or DM8575 or DM7576 or DM8576

Col. 7-9 (Blank)

Col. 10-17. Output Data Outputs are F_8 (most significant) to F_1 (least significant) All eight outputs must be specified

A 'T' in an output location indicates that the output is true

A 'C' in an output location indicates that the output is complemented (inverted)

Col. 18-39 (Blank)

Col. 40-75 This space is reserved for any unique letters/numbers desired by the customer (special part number, program number, etc) However the exact combination of characters must appear on all cards, but only those cards, associated with that particular device

Col. 76-78 (Blank)

Col. 79-80 00

CARDS 2-97: Term Data Cards Used to specify the input and output conditions

Col. 1-6. DM7575 or DM8575 or DM7576 or DM8576

Col. 7-9 (Blank)

Col. 10-17 Output Connections Outputs are F_8 (most significant) to F_1 (least significant) This field describes the outputs on which the product term appears

A '+' in one of the eight output locations indicates that the term described by the card is one of the "OR" terms in that output.

A '(blank)' in one of the eight output locations indicates that the term described by the card is not one of the "OR" terms in that output

(Care should be exercised in punching this particular field, since in most cases, unless a product term is repeated, this field will appear as one '+' and seven blanks)

Col. 18 (Blank)

Col. 19 = (equal sign)

Col. 20: (Blank)

Col. 21-34 Input Data Inputs are I_{13} (most significant) to I_0 (least significant)

An 'H' in one of the fourteen locations indicates that input appears in the high state in the output term

An 'L' in one of the fourteen input locations indicates that input appears in the low state in the output term

An 'X' in one of the fourteen input locations indicates that input does not appear in the output term.

Col. 35-39 (Blank)

Col. 40-75 This space is reserved for any unique letter/number desired by the customer (special part number, program number, etc) However the exact combination of characters must appear on all cards, but only those cards, associated with that particular device The purpose of this section is to prevent mixing of cards

Col. 76-78 (Blank)

Col. 79-80 Product Term Number 01 to 96 (All 96 cards need not be used) Zero in column 79 may be suppressed

manual entry

The matrix-blank shown in this data sheet can be used in lieu of punched cards to submit information for programming the PLA

INSTRUCTIONS

1 Circle the appropriate part number In the event a catalog part is not being purchased, circle the closest catalog part number If an electrical screen is required between the military and commerical devices, the military designation should be circled

2 Customer should write the name of his company

3 Enter the total number of unique product terms found in all eight outputs Repeated terms count only once

4 Output Inverter Option Under the appropriate output designation specify a 'T' when the high (true) level is desired on the output for the given input conditions. Specify a 'C' if the complement is needed

5 Matrix

a Input data This block is used to describe what comprises each of the 96 (maximum) product terms In each row, opposite the appropriate Product Term number, information on the fourteen Input Data locations is entered Information must be entered on all 14 inputs.

1) Enter an "H" under the appropriate input designation if that particular input appears in the product term as a high (true) level

2) Enter an "L" under the appropriate input designation if that particular input appears in the product term as a low (complemented) level

3) Enter an "X" under the appropriate input designation if that particular input does not appear in the product term

If less than 96 product terms are used leave all spaces for the unused terms blank

b. Output Data This block is used to describe the outputs on which the product terms appear

1) Enter a '+' under the appropriate output designation if the product term is contained in that output's expression

2) Leave a location blank if the product term is not contained in that output's expression

truth table/order blank

1. PART NO. — (DM7575, DM8575, DM7576, DM8576)

2. CUSTOMER IDENTIFICATION –

3. TOTAL NO. OF UNIQUE PRODUCT TERMS USED –
(Repeated Terms Count Only Once)

4. OUTPUT INVERTER OPTION

F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1

5. MATRIX

PRODUCT TERM	INPUT DATA														OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1		F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
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truth table/order blank (con't)

PRODUCT TERM	INPUT DATA														OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1		F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
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Series 54/74

DM7590/DM8590(SN54165/SN74165)
8-bit parallel-in serial-out shift register

general description

The DM7590/DM8590 utilizes Series 54/74 compatible TTL circuitry to provide an eight-bit parallel-in serial-out shift register designed to operate at frequencies of 20 MHz. The device also features gating to inhibit clocking, parallel load control, and both Q and $\overline{Q}$ outputs from the last flip flop for added flexibility.

characteristics

The Clock Inhibit input, when in the logical "1" state, will inhibit the Clock. It must be in the logical "0" state for clocking to occur.

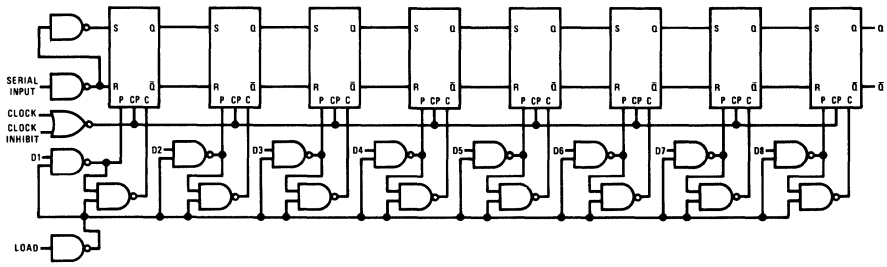
There is no difference between the Clock input and the Clock Inhibit input. Their functions may be reversed if ease of layout results.

Clocking occurs on the positive-going transition of the Clock input.

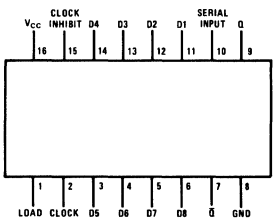
Data on the D1 through D8 inputs will be entered on the negative-going transition of the Load input. This information is entered independent of the state of the Clock, Clock Inhibit, or Serial Input lines. Information on these parallel inputs may be changed while the Load line is enabled thus changing the information in the register.

The logic level applied to the Serial Input is entered into the first flip flop when the register is clocked.

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Supply Voltage		+7V
Input Voltage		+5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7590	−55°C to +125°C
	DM8590	0°C to +70°C

electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C, I_{IN} = −12 mA			−1 5	V
Logical "1" Input Voltage	DM7590	V_{CC} = 4 5V	2 0			V
	DM8590	V_{CC} = 4 75V				
Logical "0" Input Voltage	DM7590	V_{CC} = 4 5V			0 8	V
	DM8590	V_{CC} = 4 75V				
Logical "1" Output Voltage	DM7590	V_{CC} = 4 5V	2 4			V
	DM8590	V_{CC} = 4 75V I_{OUT} = −400 μA				
Logical "0" Output Voltage	DM7590	V_{CC} = 4 5V			0 4	V
	DM8590	V_{CC} = 4 75V I_{OUT} = 16 mA				
Logical "1" Input Current (All Inputs Except Load Input)	DM7590	V_{CC} = 5 5V			40	μA
	DM8590	V_{CC} = 5 25V V_{IN} = 2 4V				
Logical "1" Input Current (Load Input)	DM7590	V_{CC} = 5 5V			80	μA
	DM8590	V_{CC} = 5 25V V_{IN} = 2 4V				
Logical "1" Input Current	DM7590	V_{CC} = 5 5V			1	mA
	DM8590	V_{CC} = 5 25V V_{IN} = 5 5V				
Logical "0" Input Current (All Inputs Except Load Input)	DM7590	V_{CC} = 5 5V			−1 6	mA
	DM8590	V_{CC} = 5 25V V_{IN} = 0 4V				
Logical "0" Input Current (Load Input)	DM7590	V_{CC} = 5 5V			−3 2	mA
	DM8590	V_{CC} = 5 25V V_{IN} = 0 4V				
Output Short Circuit Current	DM7590	V_{CC} = 5 5V	−20		−55	mA
	DM8590	V_{CC} = 5 25V V_{OUT} = 0V	−18			
Power Supply Current	DM7590	V_{CC} = 5 5V		40	63	mA
	DM8590	V_{CC} = 5 25V				
Propagation Delay to a Logical "0" from Clock to Q or $\overline{Q}$, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C		35	50	ns
Propagation Delay to a Logical "1" from Clock to Q or $\overline{Q}$, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C		26	40	ns
Propagation Delay to a Logical "0" from D_8 to Q or $\overline{Q}$, $t_{pd0(D8)}$		V_{CC} = 5 0V, T_A = 25°C		36	50	ns
Propagation Delay to a Logical "1" from D_8 to Q or $\overline{Q}$, $t_{pd1(D8)}$		V_{CC} = 5 0V, T_A = 25°C		25	40	ns
Propagation Delay to a Logical "0" from Load to Q or $\overline{Q}$, $t_{pd0(load)}$		V_{CC} = 5 0V, T_A = 25°C		42	60	ns
Propagation Delay to a Logical "1" from Load to Q or $\overline{Q}$, $t_{pd1(load)}$		V_{CC} = 5 0V, T_A = 25°C		34	50	ns
Minimum Time That Serial Input Data Must Be Set Up Prior to Clock Pulse, $t_{set\ up\ (clock)}$		V_{CC} = 5 0V, T_A = 25°C		23	40	ns
Minimum Time That Serial Input Data Must Be Held after Clock Pulse, $t_{hold\ (clock)}$		V_{CC} = 5 0V, T_A = 25°C			0	ns
Minimum Time That D_1−D_8 Input Data Must Be Set Up Prior to Load Pulse Termination, $t_{set\ up\ (load)}$		V_{CC} = 5 0V, T_A = 25°C		10	25	ns
Minimum Time That D_1−D_8 Input Data Must Be Held after to Load Pulse Termination, $t_{hold\ (load)}$		V_{CC} = 5 0V, T_A = 25°C			5	ns
Minimum Clock Pulse Width		V_{CC} = 5 0V, T_A = 25°C		25	35	ns
Minimum Load Pulse Width		V_{CC} = 5 0V, T_A = 25°C		24	35	ns
Maximum Shift Frequency		V_{CC} = 5 0V, T_A = 25°C, 40%−60% Duty Cycle	14	20		MHz

Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7590 and 0°C to +70°C for the DM8590 Typical values apply to supply voltages of 5.0V

Series 54/74

DM7595/DM8595 4096-bit bipolar ROM
DM7695/DM8695 4096-bit bipolar ROM

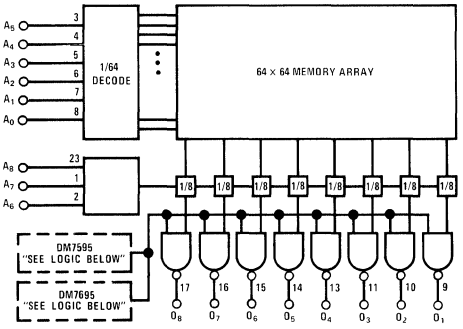
general description

The DM7595/DM8595 and DM7695/DM8695 are 4096-bit bipolar mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words. Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. Open collector outputs allow for expansion to greater number of words.

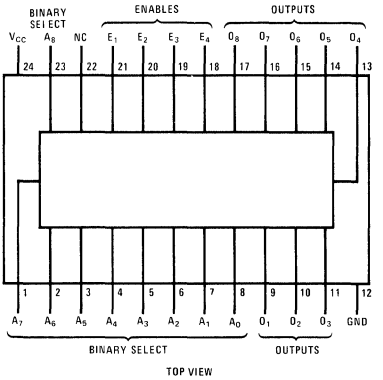
features

- Series 54/74 specification compatibility
- Pin compatible with monolithic memories 5240/6240
- Typical address time — 90 ns
- Open collector output

logic and connection diagrams

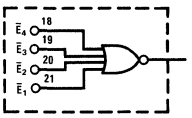


Dual-In-Line Package



logic diagrams and truth tables for enable circuitry

DM7595/DM8595

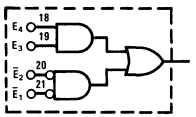


$\bar{E}_1$	$\bar{E}_2$	$\bar{E}_3$	$\bar{E}_4$	OUTPUT
0	0	0	0	Read Stored Data
1	X	X	X	Logical "1"
X	1	X	X	Logical "1"
X	X	1	X	Logical "1"
X	X	X	1	Logical "1"

X = Don't Care

ENABLE = $\bar{E}_1 \cdot \bar{E}_2 \cdot \bar{E}_3 \cdot \bar{E}_4$

DM7695/DM8695



$\bar{E}_1$	$\bar{E}_2$	E_3	E_4	OUTPUT
X	X	1	1	Read Stored Data
0	0	X	X	Read Stored Data
X	1	X	0	Disable
1	X	0	X	Disable

X = Don't Care

ENABLE = $\bar{E}_1 \cdot \bar{E}_2 + E_3 \cdot E_4$

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7595, DM7695	4 5	5 5	V
DM8595, DM8695	4 75	5 25	V
Temperature (T_A)			
DM7595, DM7695	−55	+125	°C
DM8595, DM8695	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0 8	V
Logical "1" Output Current	V_{CC} = Max	V_{OUT} 5 5V			50	μA
Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 12 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2 4V			40	μA
	V_{CC} = Max	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0 4V			−1 0	mA
Supply Current (each device)	V_{CC} = Max	Chip Enabled		103	158	mA
Input Clamp Voltage	V_{CC} = Min	I_{IN} = −12 mA	−1 5			V
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L 30 pF		30		ns
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 30 pF		100		ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 30 pF		30		ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	C_L 30 pF		80		ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7595 and DM8695 and across the 0°C to 70°C range for the DM8595 and DM8695 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

80-column card program data format

Col. 1-3: 3 Character ID code any 3 Alpha-Numeric characters. Must be the same on all cards associated with a particular pattern, but different for the ID code used on other patterns. The purpose of this code is to prevent mixing of cards

Col. 4: (Blank)

Col. 5-12: Word Data. Order is 08 (most significant) to 01 (least significant). Note 1. Characters — For TTL high level are: H or 1. Characters — For TTL low are L or 0. "Don't Care" is X.

Col. 13: (Blank)

Col. 14-21: Word Data — same format as 5-12

Col. 22: (Blank)

Col. 23-30: Word Data

Col. 31: (Blank)

Col. 32-39: Word Data

Col. 40: (Blank)

Col. 41-48: Word Data

Col. 49: (Blank)

Col. 50-57: Word Data

Col. 58: (Blank)

Col. 59-66: Word Data

Col. 67: (Blank)

Col. 68-75: Word Data

Col. 76-78: (Blank)

Col. 79-80: Card sequence number 1 to 64 Leading zeros may be punched or suppressed. (Note 2)

NOTE 1. The words are listed in sequence beginning on the first card with the word associated with address 0 and ending on the last card with the word associated with address 512, if all 4096-bits are programmed Address input A_8 is the most significant, A_0, the least significant

NOTE 2. Card sequence numbers reference a specific group of 8 words, i e ,

Card 01 Word address 0 to 7
Card 02 Word address 8 to 15
Card 03 Word address 16 to 23
.
.
.
Card 64 Word address 504 to 511

Series 54/74

DM7596/DM8596 TRI-STATE® 4096-bit bipolar ROM
DM7696/DM8696 TRI-STATE 4096-bit bipolar ROM

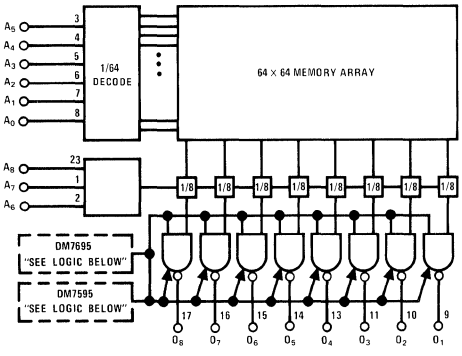
general description

The DM7596/DM8596 and DM7696/DM8696 are 4096-bit bipolar mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. TRI-STATE outputs allow for expansion to greater numbers of words without sacrifice in speed as would be evidenced by open-collector outputs

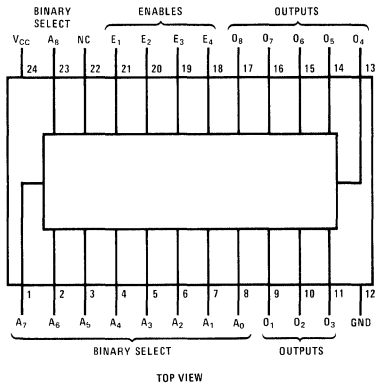
features

- Series 54/74 specification compatibility
- Pin compatible with monolithic memories 5240/6240
- Typical address time — 90 ns
- TRI-STATE outputs

logic and connection diagrams



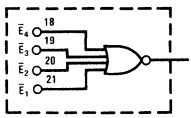
Dual-In-Line Package



TOP VIEW

logic diagrams and truth tables for enable circuitry

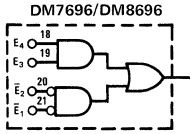
DM7596/DM8596



$\bar{E}_1$	$\bar{E}_2$	$\bar{E}_3$	$\bar{E}_4$	OUTPUT
0	0	0	0	Read Stored Data
1	X	X	X	Hi - Z
X	1	X	X	Hi - Z
X	X	1	X	Hi - Z
X	X	X	1	Hi - Z

X = Don't Care
ENABLE = $\bar{E}_1 \cdot \bar{E}_2 \cdot \bar{E}_3 \cdot \bar{E}_4$

DM7696/DM8696



$\bar{E}_1$	$\bar{E}_2$	E_3	E_4	OUTPUT
X	X	1	1	Read Stored Data
0	0	X	X	Read Stored Data
X	1	X	0	Hi - Z
1	X	0	X	Hi - Z

X = Don't Care
ENABLE = $\bar{E}_1 \quad \bar{E}_2 + E_3 \cdot E_4$

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7596, DM7696	4 5	5 5	V
DM8596, DM8696	4 75	5 25	V
Temperature (T_A)			
DM7596, DM7696	−55	+125	°C
DM8596, DM8696	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min		2			V
Logical "0" Input Voltage	V_{CC} = Min				0 8	V
Logical "1" Output Voltage DM7596/DM7696 / DM8596/DM8696	V_{CC} = Min	I_{OUT} = −2 0 mA / I_{OUT} = −5 2 mA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 12 mA			0 4	V
Third State Output Current	V_{CC} = Max	V_O = 0 4V or 2 4V			±40	μA
Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2 4V			40	μA
	V_{CC} = Max	V_{IN} = 5 5V			1	μA
Logical "0" Input Current	V_{CC} = Max	V_{IN} = 0 4V			−1 0	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	V_{OUT} = 0V	−30		−70	mA
Supply Current (each device)	V_{CC} = Max	Chip Disabled		106	158	mA
Input Clamp Voltage	V_{CC} = Min	V_{IN} = −12 mA	−1 5			V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	R_L = 400Ω, C_L = 50 pF		100		ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C	R_L = 400Ω, C_L = 50 pF		70		ns
Delay from Enable to High Impedance State (from Logical "1" Level), t_{1H}	V_{CC} = 5 0V, T_A = 25°C			10		ns
Delay from Enable to High Impedance State (from Logical "0" Level), t_{0H}	V_{CC} = 5 0V, T_A = 25°C			15		ns
Delay from Enable to Logical "1" Level (from High Impedance State), t_{H1}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF		25		ns
Delay from Enable to Logical "0" Level (from High Impedance State), t_{H0}	V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF		30		ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the -55°C to +125°C temperature range for the DM7596 and DM7696 and across the 0°c to 70°C range for the DM8596 and DM8696 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

80-column card program data format

Col. 1-3: 3 Character ID code any 3 Alpha-Numeric characters. Must be the same on all cards associated with a particular pattern, but different for the ID code used on other patterns. The purpose of this code is to prevent mixing of cards.

Col. 4: (Blank)

Col. 5-12: Word Data. Order is 08 (most significant) to 01 (least significant). Note 1. Characters – For TTL high level are: H or 1 Characters – For TTL low are L or 0. "Don't Care" is X.

Col. 13: (Blank)

Col. 14-21: Word Data – same format as 5-12.

Col. 22: (Blank)

Col. 23-30: Word Data

Col. 31: (Blank)

Col. 32-39: Word Data

Col. 40: (Blank)

Col. 41-48: Word Data

Col. 49: (Blank)

Col. 50-57: Word Data

Col. 58: (Blank)

Col. 59-66: Word Data

Col. 67: (Blank)

Col. 68-75: Word Data

Col. 76-78: (Blank)

Col. 79-80: Card sequence number. 1 to 64. Leading zeros may be punched or suppressed. (Note 2)

NOTE 1. The words are listed in sequence beginning on the first card with the word associated with address 0 and ending on the last card with the word associated with address 512, if all 4096-bits are programmed Address input A_8 is the most significant, A_0, the least significant.

NOTE 2. Card sequence numbers reference a specific group of 8 words, i e ;

Card 01 Word address 0 to 7
Card 02 Word address 8 to 15
Card 03 Word address 16 to 23

Card 64· Word address 504 to 511

Series 54/74

DM7597/DM8597 TRI-STATE®1024-bit read only memory

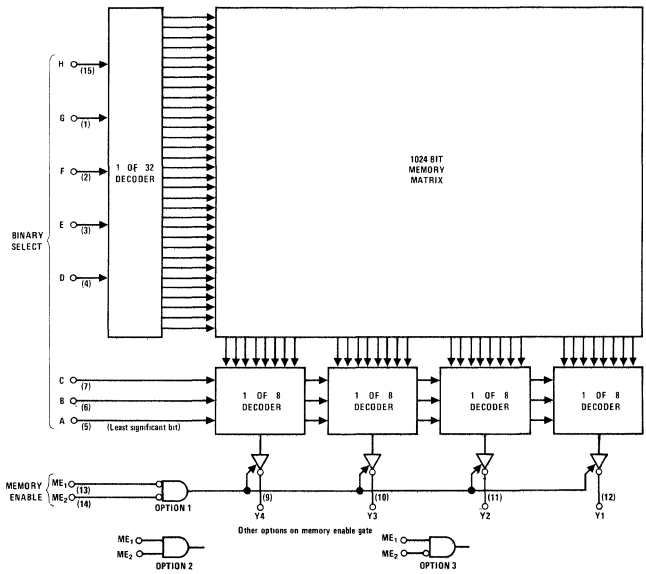
general description

The DM7597/DM8597 is a custom-programmed read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided, which when mask-programmed in one of three options described will cause all four outputs to either read the normal memory contents or go to the "high impedance" state. In this state both the upper and lower output transistors are turned off. The outputs may therefore be paralleled to increase word capacity; since in the high-impedance state they present only a minimal load to the active output.

features

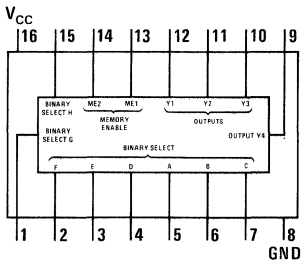
- Pin compatible with SN54187/SN74187
- 35 ns typical delay from address to output
- Can be expanded to 32,768 4-bit words by simple paralleling of outputs
- Programmable memory enable inputs

logic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

truth table

TABLE of Programmable Memory Enable Options

OPTION	ME1	ME2	OUTPUTS
1	0	0	Normal
	1	X	HIGH Impedance
	X	1	HIGH Impedance
2	1	1	Normal
	0	X	HIGH Impedance
	X	0	HIGH Impedance
3	1	0	Normal
	X	1	HIGH Impedance
	0	X	HIGH Impedance

X = don't care

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM7597	−55°C to +125°C
	DM8597	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7597	V_{CC} = 4.5V		2.0			V
	DM8597	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7597	V_{CC} = 4.5V				0.8	V
	DM8597	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7597	V_{CC} = 4.5V	I_O = −2 mA	2.4			V
	DM8597	V_{CC} = 4.75V	I_O = −5.2 mA				
Logical "0" Output Voltage	DM7597	V_{CC} = 4.5V	I_O = 16 mA			0.4	V
	DM8597	V_{CC} = 4.75V					
Third State Output Current	DM7597	V_{CC} = 5.5V	V_O = 2.4V			40	μA
	DM8597	V_{CC} = 5.25V	V_O = 0.4V			−40	μA
Logical "1" Input Current	DM7597	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8597	V_{CC} = 5.25V					
Logical "0" Input Current	DM7597	V_{CC} = 5.5V	V_{IN} = 5.5V			1.0	mA
	DM8597	V_{CC} = 5.25V					
	DM7597	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.0	mA
	DM8597	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7597	V_{CC} = 5.5V	V_O = 0.0V	−20		−70	mA
	DM8597	V_{CC} = 5.25V					
Supply Current	DM7597	V_{CC} = 5.5V	All Inputs at GND		75	110	mA
	DM8597	V_{CC} = 5.25V					
Input Clamp Voltage	DM7597	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM8597	V_{CC} = 4.75V					
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5.0V T_A = 25°C			39	60	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5.0V T_A = 25°C			31	60	ns
Delay from Enable to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V T_A = 25°C			30		ns
Delay from Enable to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V T_A = 25°C			10		ns
Delay from Enable to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V T_A = 25°C			30		ns
Delay from Enable to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V T_A = 25°C			30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7597 and across the 0°C to 70°C range for the DM8597. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

ordering instructions

Programming instructions for the DM7597 or DM8597 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data, therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

supplementary ordering data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

data card format

Column

1- 3 Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.

4 Punch a "—" (Minus sign)

5- 7 Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.

8- 9 Blank

10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output irrelevant.

14 Blank

15-18 Punch "H", "L", or "X" for the second set of outputs.

19 Blank

20-23 Punch "H", "L", or "X" for the third set of outputs.

24 Blank

25-28 Punch "H", "L", or "X" for the fourth set of outputs.

29 Blank

30-33 Punch "H", "L", or "X" for the fifth set of outputs.

34 Blank

35-38 Punch "H", "L", or "X" for the sixth set of outputs.

39 Blank

40-43 Punch "H", "L", or "X" for the seventh set of outputs.

44 Blank

45-48 Punch "H", "L", or "X" for the eighth set of outputs.

49 Blank

50-51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53-55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57-58 Punch the last two digits of the current year.

59 Blank

60-61 Punch "DM"

62-65 Punch 7597 or 8597

66-70 Blank

71 Punch 1, 2, or 3 for memory enable option desired (assumed 1 if not punched)

Series 54/74

DM7598/DM8598 TRI-STATE® 256-bit read only memory

general description

The DM7598/DM8598 is a customer programmed 256-bit read-only memory organized as 32 8-bit words. A five-bit input code selects the appropriate word which then appears on the eight outputs. An enable input overrides the select inputs and blanks all outputs.

Although the DM7598/DM8598 can have its outputs tied together for word-expansion, the outputs are not open-collector, but rather the familiar totem-pole output with the capability of being placed in a "third-state". This unique three state concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If however, on all but one of the connected devices both the upper and lower output transistors are turned off, then the one remaining device in the normal low impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7598/DM8598.

A typical system connection demonstrating expansion to greater numbers of words is shown in Figure 1. While it is true that in a TTL system open-collector gates could be used to perform the logic function of these three-state elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7598/DM8598 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level thus assuring both speed and waveform integrity.

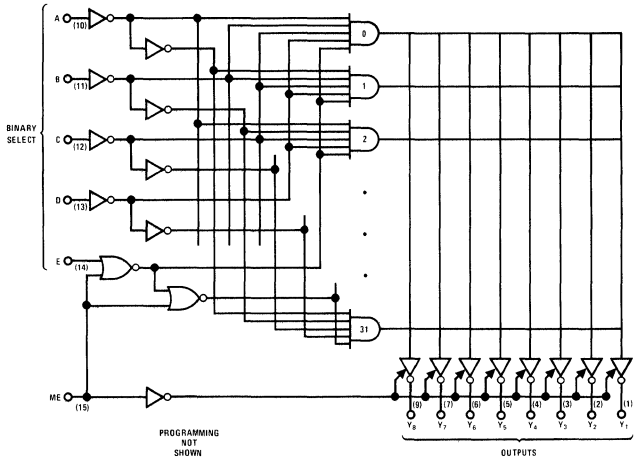
It is possible to connect as many as 128 DM8598s to a common bus line and still have adequate drive capability to allow fan out from the bus. The example shown in Figure 2 indicates how this guarantee can be made under worst-case conditions.

Figure 3 indicates how multiple packages can be used to increase word length.

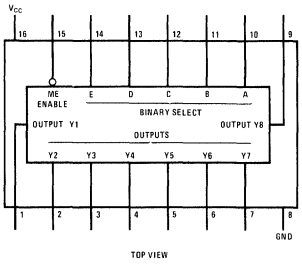
features

- Pin compatible with SN5488/SN7488
- Organized as 32 8-bit words
- Full internal decoding
- 30 ns typical access time
- 350 mW typical power dissipation
- Input clamp diodes
- Designed for bus-organized systems
- Strobe override

logic and connection diagrams



Dual-In-Line Package



absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5 5V
Operating Temperature Range	DM7598	−55°C to +125°C
	DM8598	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7598 / DM8598	V_{CC} = 4 5V / V_{CC} = 4 75V		2 0			V
Logical "0" Input Voltage	DM7598 / DM8598	V_{CC} = 4 5V / V_{CC} = 4 75V				0 8	V
Logical "1" Output Voltage	DM7598 / DM8598	V_{CC} = 4 5V / V_{CC} = 4 75V	I_O = −2 mA / I_O = −5 2 mA	2 4			V
Logical "0" Output Voltage	DM7598 / DM8598	V_{CC} = 4 5V / V_{CC} = 4 75V	I_O = +12 mA			0 4	V
Third State Output Current	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_O = 2 4V / V_O = 0 4V			±40 / ±40	μA / μA
Logical "1" Input Current							
Address Inputs	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			40	μA
Enable Input	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 2 4V			80	μA
Any Input	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Logical "0" Input Current							
Address Inputs	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 0 4V			−1 6	mA
Enable Input	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_{IN} = 0 4V			−3 2	mA
Output Short Circuit Current (Note 3)	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	V_O = 0V	−20		−70	mA
Supply Current	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	Inputs Grounded		70	99	mA
Input Clamp Voltage	DM7598 / DM8598	V_{CC} = 4 5V / V_{CC} = 4 75V	I_{IN} = −12 mA			−1 5	V
Output V_{CC} Clamp Voltage	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	I_O = +12 mA			V_{CC} +1 5	V
Output Ground Clamp Voltage	DM7598 / DM8598	V_{CC} = 5 5V / V_{CC} = 5 25V	I_O = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C			29	50	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5 0 V, T_A = 25°C			33	50	ns
Delay from Enable to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0 V, T_A = 25°C	C_L = 5 pF		13	20	ns
Delay from Enable to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V, T_A = 25°C	C_L = 5 pF		24	36	ns
Delay from Enable to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF		16	25	ns
Delay from Enable to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF		26	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7598 and across the 0°C to 70°C range for the DM8598 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted.

typical applications

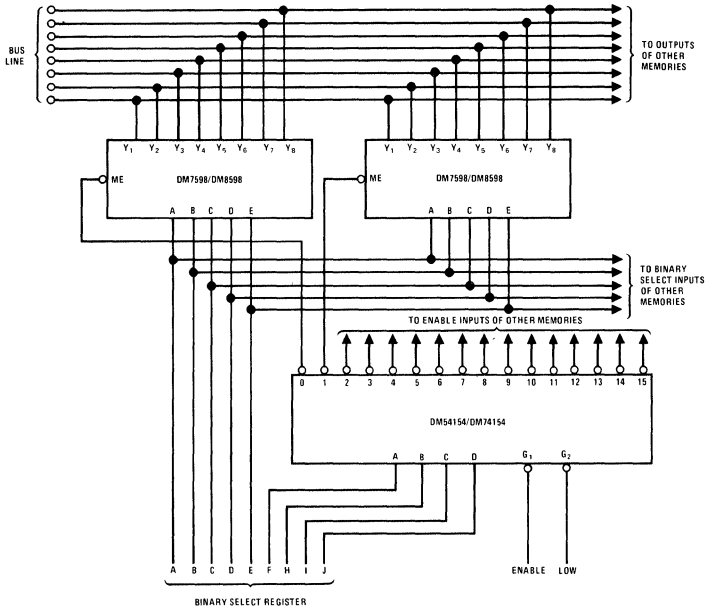


FIGURE 1. Expansion to Larger Word Capacity

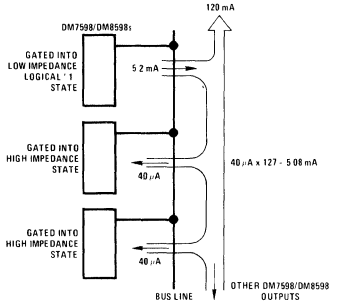


FIGURE 2.

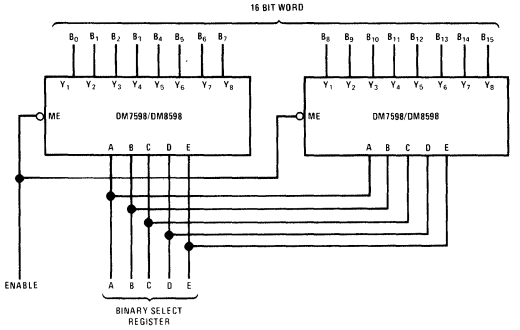


FIGURE 3.

DM7598AA TRUTH TABLE

A special pattern has been generated for the DM7598/DM8598 The AA pattern provides a sine table The 5-bit input code linearly divides 90° into 32 equal segments Each 8-bit output is therefore the sine of the angle applied

EXAMPLE Input 11010 means 26/32 of 90°, or about 73° The corresponding output 11110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about 95, which is close to the sine of 73° Rounding-off has not been employed, since without rounding-off it is possible to extend the accuracy with additional ROMs

The truth table is shown

	INPUTS						OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	ME	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
2	0	0	0	1	0	0	0	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	0	1	0	0	1	0	1
4	0	0	1	0	0	0	0	0	1	1	0	0	0	1
5	0	0	1	0	1	0	0	0	1	1	1	1	1	0
6	0	0	1	1	0	0	0	1	0	0	1	0	1	0
7	0	0	1	1	1	0	0	1	0	1	0	1	1	0
8	0	1	0	0	0	0	0	1	1	0	0	0	0	1
9	0	1	0	0	1	0	0	1	1	0	1	1	0	1
10	0	1	0	1	0	0	0	1	1	1	1	0	0	0
11	0	1	0	1	1	0	1	0	0	0	0	0	1	1
12	0	1	1	0	0	0	1	0	0	0	1	1	1	0
13	0	1	1	0	1	0	1	0	0	1	1	0	0	0
14	0	1	1	1	0	0	1	0	1	0	0	0	1	0
15	0	1	1	1	1	0	1	0	1	0	1	0	1	1
16	1	0	0	0	0	0	1	0	1	1	0	1	0	1
17	1	0	0	0	1	0	1	0	1	1	1	1	0	1
18	1	0	0	1	0	0	1	1	0	0	0	1	0	1
19	1	0	0	1	1	0	1	1	0	0	1	1	0	1
20	1	0	1	0	0	0	1	1	0	1	0	1	0	0
21	1	0	1	0	1	0	1	1	0	1	1	0	1	1
22	1	0	1	1	0	0	1	1	1	0	0	0	0	1
23	1	0	1	1	1	0	1	1	1	0	0	1	1	1
24	1	1	0	0	0	0	1	1	1	0	1	1	0	0
25	1	1	0	0	1	0	1	1	1	1	0	0	0	1
26	1	1	0	1	0	0	1	1	1	1	0	1	0	0
27	1	1	0	1	1	0	1	1	1	1	1	0	0	0
28	1	1	1	0	0	0	1	1	1	1	1	0	1	1
29	1	1	1	0	1	0	1	1	1	1	1	1	0	1
30	1	1	1	1	0	0	1	1	1	1	1	1	1	0
31	1	1	1	1	1	0	1	1	1	1	1	1	1	1
All	X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

X = Don't Care

TRUTH TABLE/ORDER BLANK

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits) The customer does this by filling out the Truth Table on this data sheet, and sending it in with his purchase order.

	INPUTS						OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	ME	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
All	X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

X = Don't Care

Notice This sheet must be completed and signed by an authorized representative of the customer's company before an order can be entered

To be used by National only

_____ Part Number

_____ S O Number

_____ Date Received

_____ Authorized Representative _____ Date

_____ Company

Desired Part ☐ DM7598 ☐ DM8598

Series 54/74

DM7599/DM8599 TRI-STATE®
64-bit random access read/write memory

general description

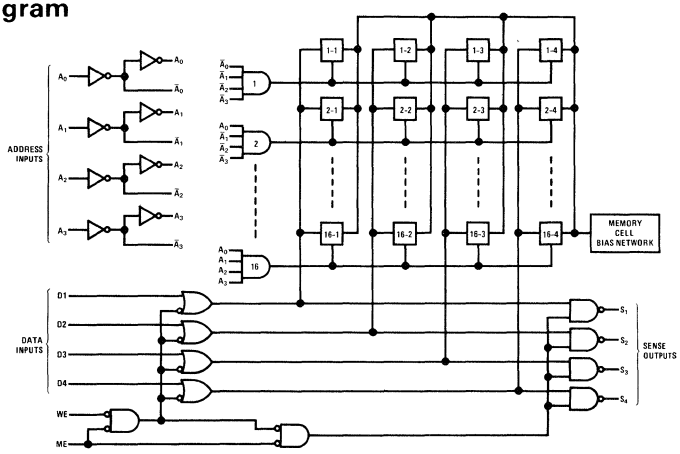
The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

features

- Series 54/74 compatible
- Same pin-out as SN5489/SN7489
- Organized as 16 4-bit words
- Expandable to 2048 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns
- Typical power dissipation 400 mW

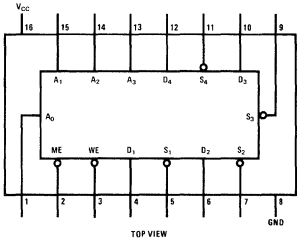
1

block diagram



connection diagram

Dual-In-Line Package



truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

absolute maximum ratings (Note 1)

Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Input Voltage	5 5V	Operating Temperature Range	
Output Voltage	5 5V	DM7599	−55°C to +125°C
Time that two bus-connected devices may be in opposite low impedance states simultaneously	Indefinite	DM8599	0°C to +70°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7599	V_{CC} = 4 5V		2 0			V
	DM8599	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM7599	V_{CC} = 4 5V				0 8	V
	DM8599	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM7599	V_{CC} = 4 5V	I_O = −2 mA	2 4			V
	DM8599	V_{CC} = 4 75V	I_O = −5 2 mA	2 4			V
Logical "0" Output Voltage	DM7599	V_{CC} = 4 5V	I_O = 12 mA			0 4	V
	DM8599	V_{CC} = 4 75V					
Third State Output Current	DM7599	V_{CC} = 5 5V	V_O = 0 4V			±40	μA
	DM8599	V_{CC} = 5 25V	V_O = 2 4V			±40	
Logical "1" Input Current	DM7599	V_{CC} = 5 5V	V_{IN} = 2 4V			40	μA
	DM8599	V_{CC} = 5 25V					
	DM7599	V_{CC} = 5 5V	V_{IN} = 5 5V			1	mA
	DM8599	V_{CC} = 5 25V					
Logical "0" Input Current	DM7599	V_{CC} = 5 5V	V_{IN} = 0 4V			−1 6	mA
	DM8599	V_{CC} = 5 25V					
Output Short Circuit Current (Note 3)	DM7599	V_{CC} = 5 5V		−30		−70	mA
	DM8599	V_{CC} = 5 25V					
Supply Current	DM7599	V_{CC} = 5 5V	All Inputs at GND		80	120	mA
	DM8599	V_{CC} = 5 25V					
Input Clamp Voltage	DM7599	V_{CC} = 4 5V	I_{IN} = −12 mA			−1 5	V
	DM8599	V_{CC} = 4 75V					
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5 0V T_A = 25°C			28	45	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5 0V T_A = 25°C			27	45	ns
Delay from Memory Enable to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0V T_A = 25°C			12	20	ns
Delay from Memory Enable to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V T_A = 25°C			21	30	ns
Delay from Memory Enable to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5 0V T_A = 25°C			14	20	ns
Delay from Memory Enable to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5 0V T_A = 25°C			19	30	ns
Write Enable Pulsewidth, t_{WP}				40	23		ns
Setup Time, Data				0	−15		ns
Hold Time, Data				0	−14		ns
Setup Time Address				0	−17		ns
Hold Time, Address				5	−7		ns
Sense Recovery Time					42	60	ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7599 and across the 0°C to 70°C range for the DM8599 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3 Only one output at a time should be shorted

Series 54/74

DM7800/DM8800 dual voltage translator

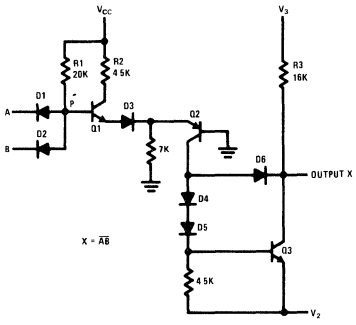
general description

The DM7800/DM8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

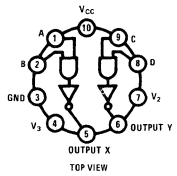
features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DM7800 −55°C to +125°C
  DM8800 0°C to +70°C
- Compatible with all MOS devices

schematic and connection diagrams

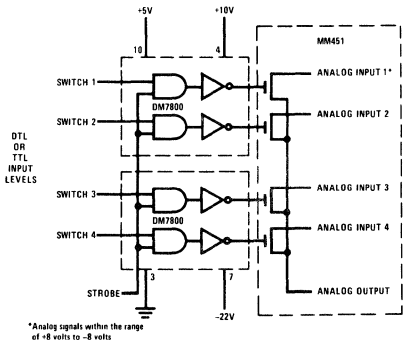


Metal Can Package

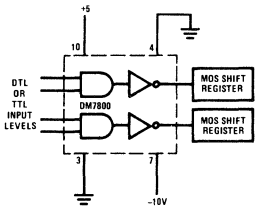


typical applications

4-Channel Analog Switch



Bipolar to MOS Interfacing



absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V_2 Supply Voltage	−30V
V_3 Supply Voltage	+30V
V_3-V_2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7800	−55°C to +125°C
DM8800	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Logical "1" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.4V		−0.2	−0.4	mA
Output Leakage Current (Note 2)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.8V (Note 5)			10	μA
Output Collector Resistor		T_A = 25°C	11.5	16.0	20.0	kΩ
Logical "0" Output Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V V_{IN} = 2.0V (Note 5)			V_2 + 2.0	V
Power Supply Current Logical "0" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "1" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0V		0.22	0.41	mA
Transition Time to Logical "0" Output		T_A = 25°C C = 15 pF (Note 6)	25	70	125	ns
Transition Time to Logical "1" Output		T_A = 25°C C = 15 pF (Note 7)	25	62	125	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7800 and 0°C to +70°C for the DM8800 unless otherwise specified.
Note 2: Current measured is drawn from V_3 supply
Note 3: Current measured is drawn from V_{CC} supply.
Note 4: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.
Note 5: Specification applies for all allowable values of V_2 and V_3.
Note 6: Measured from 1.5V on input to 50% level on output.
Note 7: Measured from 1.5V on input to logic "0" voltage, plus 1V.

theory of operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2 The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

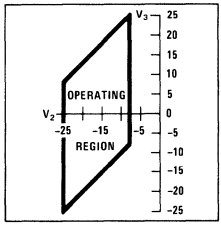
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3 And when Q_3 turns on the output voltage drops to the logical "0" level

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2 Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



Series 54/74

DM7806/DM8806 high speed MOS to TTL level converter

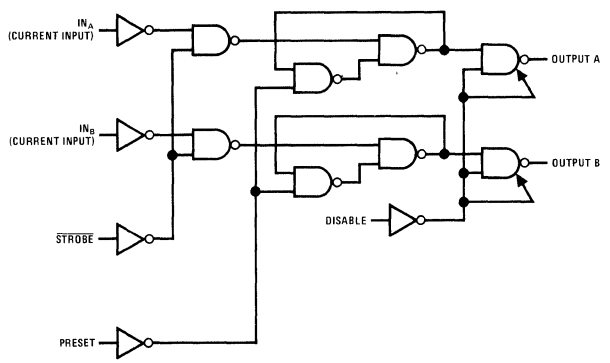
general description

The DM7806/DM8806 is a high speed MOS to TTL level converter. This circuit acts as an interface level converter between MOS & TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

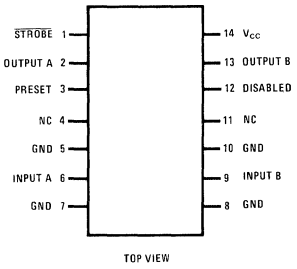
features

- Very low output impedance — high drive capability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

truth table

IN A OR B	ST	P	D	Q_A OR Q_B
0	1	1	0	1
1	1	1	0	1
0	0	1	0	0
1	0	1	0	1
X	X	X	1	Hi-Z

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7806	4 5	5 5	V
DM8806	4 75	5 25	V
Temperature (T_A)			
DM7806	−55	+125	°C
DM8806	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Current Pin 6, 9	V_{CC} = Min	500			μA
Logical "0" Input Current Pin 6, 9	V_{CC} = Min			200	μA
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			8	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1 5 mA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0 4	V
Third State Output Current	V_{CC} = Max, V_O = 2 4V			40	μA
	V_{CC} = Max, V_O = 0 4V			−40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Supply Current	V_{CC} = Max, $V_{IN(DISABLE)}$ = 2V, Other Inputs = 0V			40	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1 5	V
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_O = 0V DM7806	−20		−70	mA
	DM8806	−18		−70	mA
Propagation Delay to a Logical "0" from STROBE to Output, t_{ds}	V_{CC} = 5 0V (See Figure 1) T_A = 25°C		17	25	ns
Propagation Delay to a Logical "1" from Preset to Output, t_{dp}	V_{CC} = 5 0V (See Figure 1) T_A = 25°C		22	32	ns
Delay from Disable Input to High Impedance State (from Logical ',1" Level), t_{1H}	V_{CC} = 5 0V (See Figure 2) T_A = 25°C		7	11	ns
Delay from Disable Input to High Impedance State (from Logical "0" Level), t_{0H}	V_{CC} = 5 0V (See Figure 3) T_A = 25°C		17	25	ns
Delay from Disable Input to Logical "1" Level (from High Impedance State), t_{H1}	V_{CC} = 5 0V (See Figure 2) T_A = 25°C		9	14	ns
Delay from Disable Input to Logical "0" Level (from High Impedance State), t_{H0}	V_{CC} = 5 0V (See Figure 3) T_A = 25°C		13 5	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7806 and across the 0°C to 70°C range for the DM8806 All typicals are given for V_{CC} = 5 0V, T_A = 25°C.

Note 3: Only one output at a time should be shorted

Series 54/74

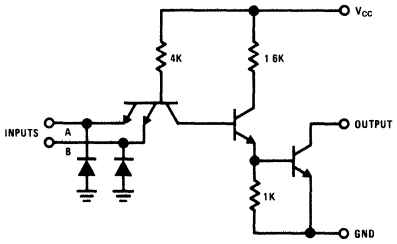
DM7810/DM8810 quad 2-input TTL-MOS interface gate
DM7811/DM8811 quad 2-input TTL-MOS interface gate
DM7812/DM8812 TTL-MOS hex inverter

general description

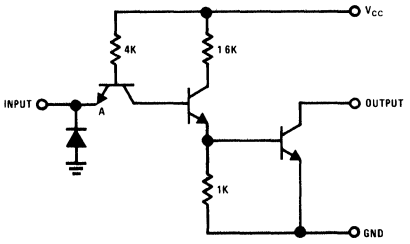
These Series 54/74 compatible gates are high output voltage versions of the DM5401/DM7401 (SN5401/SN7401), DM5403/DM7403 (SN5403/SN7403), and DM5405/DM7405 (SN5405/SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

schematic and connection diagrams

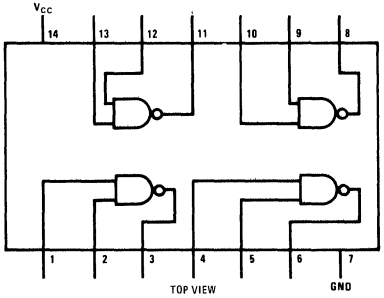


DM7810/DM8810, DM7811/DM8811



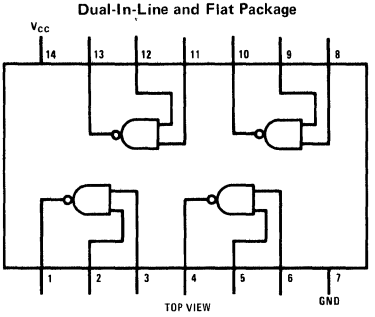
DM7812/DM8812

Dual-In-Line Package



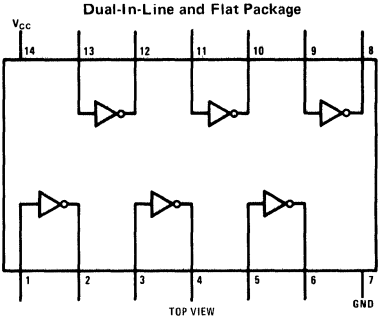
DM7810/DM8810

Dual-In-Line and Flat Package



DM7811/DM8811

Dual-In-Line and Flat Package



DM7812/DM8812

absolute maximum ratings

V_{CC}	7V
Input Voltage	5 5V
Output Voltage	14V
Storage Temperature Range	−65°C to +150°C
Lead TEmperature (Soldering, 10 sec)	300°C

operating conditions

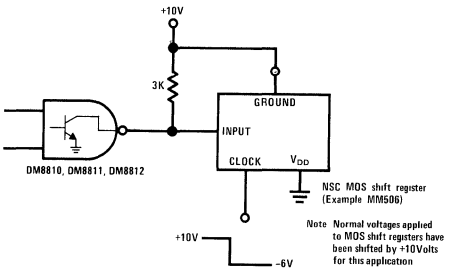
	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM78XX	4 75	5 25	V
DM88XX	4 75	5 25	V
Temperature (T_A)			
DM78XX	−55	+125	°C
DM88XX	0	70	°C

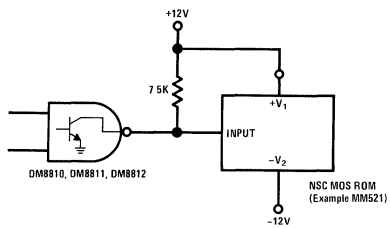
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5 0V, T_A = 25°C I_{IN} = −12 mA			−1 5	V
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Current	V_{CC} = Min V_{IN} = 0 8V V_{OUT} = 10V V_{IN} = 0.0V			250 40	μA μA
Logical "1" Output Breakdown Voltage	V_{CC} = Min, V_{IN} = 0V I_{OUT} = 1 mA	14			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1 6	mA
Supply Current — Logical "0" (Each Gate)	V_{CC} = Max, V_{IN} = 5 0V		3.0	5.1	mA
Supply Current — Logical "1" (Each Gate)	V_{CC} = Max, V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5 0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78XX and across the 0°C to 70°C range for the DM88XX All typicals are given for V_{CC} = 5 0V and T_A = 25°C

typical applications





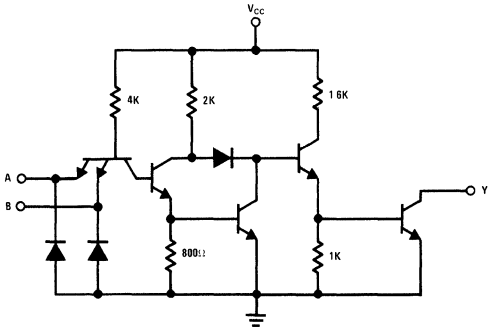
Series 54/74

DM7819/DM8819 quad 2-input TTL-MOS AND gate

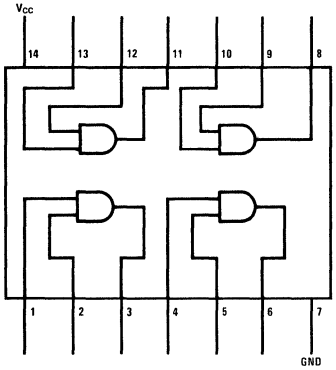
general description

The DM7819 is the high output voltage version of the SN5409. Its open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7 0V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7819	4 5	5 5	V
DM8819	4 75	5 25	V
Temperature (T_A)			
DM7819	−55	+125	°C
DM8819	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Current	V_{CC} = Min, V_{IN} = 2 0V, V_{OUT} = 10V			40 0	μA
	V_{CC} = Min, V_{IN} = 4 5V, V_{OUT} = 14V			1 0	mA
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40 0	μA
	V_{CC} = Max, V_{IN} = 5 5V			1 0	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1.6	mA
Supply Current — Logical "1"	V_{CC} = Max, V_{IN} = 5V		11 0	21 0	mA
Logical "0"	V_{CC} = Max, V_{IN} = 0V		20 0	33 0	mA
Input Clamp Voltage	V_{CC} = 5 0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" t_{pd0}					
DM7819 / DM8819	V_{CC} = 5 0V, T_A = 25°C		16 0	24 0	ns
Propagation Delay to a Logical "1" t_{pd1}					
DM7819 / DM8819	V_{CC} = 5 0V, T_A = 25°C		16 0	32 0	ns

Note 1 "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2 Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7819 and across the 0°C to 70°C range for the DM8819 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Series 54/74

DM7820/DM8820 dual line receiver

general description

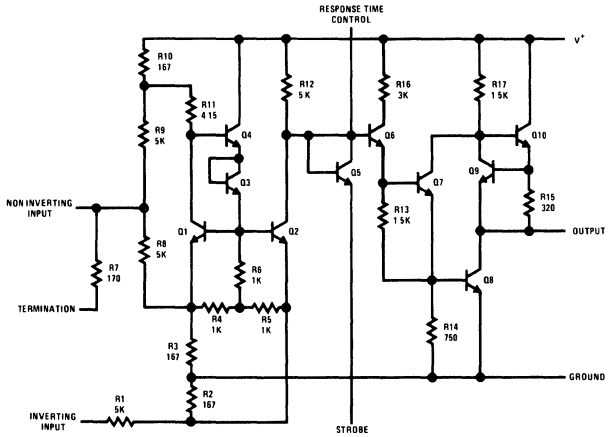
The DM7820, specified from -55°C to 125°C, and the DM8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

features

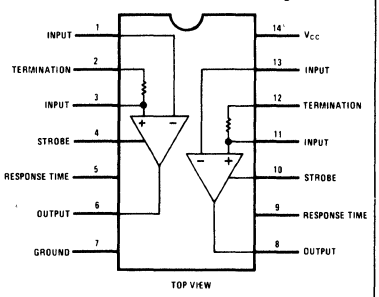
- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fanout of two with either DTL or TTL integrated circuits

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DM7820 and the DM8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

schematic and connection diagrams

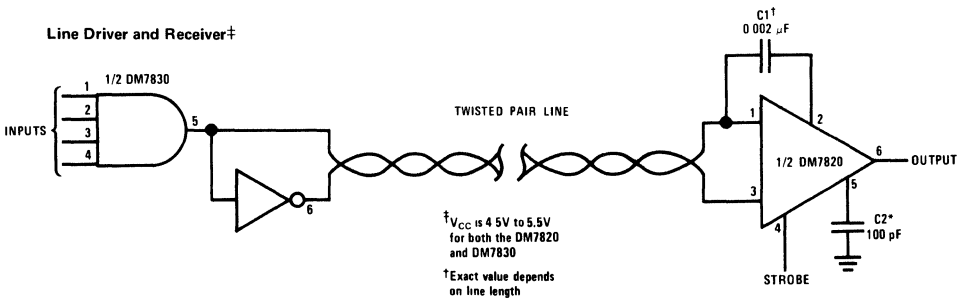


Dual-In-Line and Flat Package



typical application

Line Driver and Receiver‡



‡V_{CC} is 4.5V to 5.5V for both the DM7820 and DM7830

†Exact value depends on line length

*Optional to control response time

absolute maximum ratings

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Power Dissipation (Note 1)	600 mW
Operating Temperature Range	
DM7820	−55°C to +125°C
DM8820	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

electrical characteristics (Notes 2 & 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Threshold Voltage	$V_{IN} = 0$	−0.5	0	0.5	V
	$-15V \leq V_{IN} \leq 15V$	−1.0	0	1.0	V
High Output Level	$I_{OUT} \leq 0.2$ mA	2.5		5.5	V
Low Output Level	$I_{sink} \leq 3.5$ mA	0		0.4	V
Inverting Input Resistance		3.6	5.0		kΩ
Non-inverting Input Resistance		1.8	2.5		kΩ
Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
Response Time	$C_{delay} = 0$		40		ns
	$C_{delay} = 100$ pF		150		ns
Strobe Current	$V_{strobe} = 0.4V$		1.0	1.4	mA
	$V_{strobe} = 5.5V$			−5.0	μA
Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
	$V_{IN} = 0$		5.8	10.2	mA
	$V_{IN} = -15V$		8.3	15.0	mA
Non-inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
	$V_{IN} = 0$	−1.6	−1.0		mA
	$V_{IN} = -15V$	−9.8	−7.0		mA
Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
	$V_{IN} = 0$		0	−0.5	mA
	$V_{IN} = -15V$	−4.2	−3.0		mA

Note 1 For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the DM7820 or 105°C for the DM8820

Note 2. These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq 125°C$ for the DM7820 or $0°C \leq T_A \leq 70°C$ for the DM8820 unless otherwise specified typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently

Note 3. The specifications and curves given are for one side only Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions

Series 54/74

DM7820A/DM8820A dual line receiver

general description

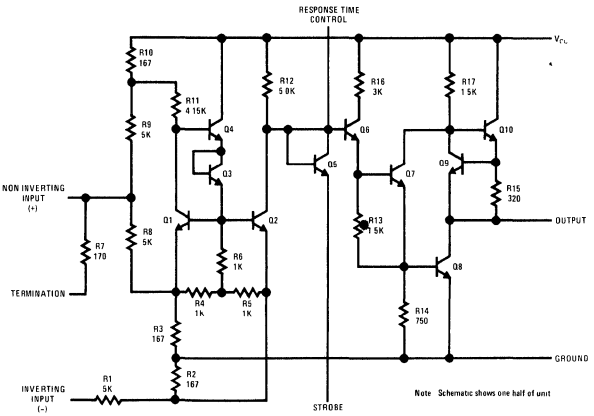
The DM7820A and the DM8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals The output is directly compatible with RTL, DTL or TTL integrated circuits.

features

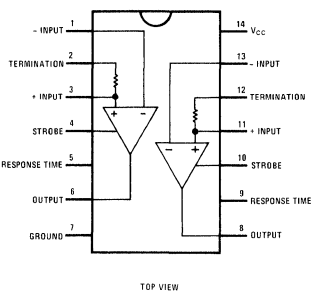
- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed, 3 (max)
- Series 54/74 compatible

The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DM7820A and the DM8820A are specified, worst case, over their full operating temperature range (−55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

schematic and connection diagrams

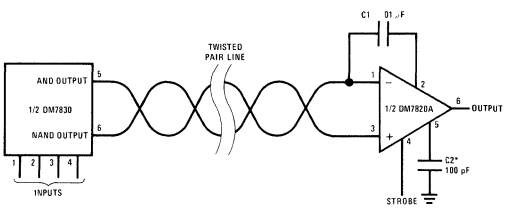


Dual-In-Line and Flat Packages



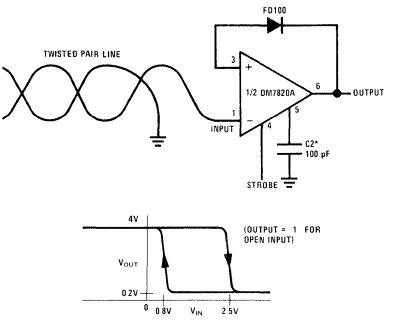
typical applications

Differential Line Driver and Receiver



*Optional to control response time

Single Ended (EIA-RS232C) Receiver with Hysteresis



absolute maximum ratings

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation (Note 1)	600 mW
Operating Temperature Range	
DM7820A	−55°C to 125°C
DM8820A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2, 3 & 4)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	V_{CM}	OUTPUT	OTHER				
Differential Threshold Voltage	$-3V \le V_{CM} \le +3V$	−400 μA	$V_{OUT} \ge 2.5V$		+0.06	+0.5	V
	$-15V \le V_{CM} \le +15V$	−400 μA	$V_{OUT} \ge 2.5V$		+0.06	+1.0	V
	$-3V \le V_{CM} \le +3V$	+16 mA	$V_{OUT} \le 0.4V$		−0.08	−0.5	V
	$-15V \le V_{CM} \le +15V$	+16 mA	$V_{OUT} \le 0.4V$		−0.08	−1.0	V
Inverting Input Resistance	$-15V \le V_{CM} \le +15V$			3.6	5		kΩ
Non-Inverting Input Resistance	$-15V \le V_{CM} \le +15V$			1.8	2.5		kΩ
Line Termination Resistance			$T_A = 25°C$	120	170	250	Ω
Inverting Input Current	+15V				+3.0	+4.2	mA
	0V				0	−0.5	mA
	−15V				−3.0	−4.2	mA
Non-Inverting Input Current	+15V				+5.0	+7.0	mA
	0V				−1.0	−1.6	mA
	−15V				−7.0	−9.8	mA
Power Supply Current	+15V	Logic "0"	$V_{DIFF} = -1V$		+3.9	+6.0	mA
	0V	Logic "0"	$V_{DIFF} = -0.5V$		+6.5	+10.2	mA
	−15V	Logic "0"	$V_{DIFF} = -1V$		+9.2	+14.0	mA
Logical "1" Output Voltage		−400 μA	$V_{DIFF} = +1V$	2.5	4.0	5.5	V
Logical "0" Output Voltage		+16 mA	$V_{DIFF} = -1V$	0	0.22	0.4	V
Logical "1" Strobe Input Voltage		+16 mA	$V_{OUT} \le 0.4V$, $V_{DIFF} = -3V$	2.1			V
Logical "0" Strobe Input Voltage		−400 μA	$V_{OUT} \ge 2.5V$, $V_{DIFF} = -3V$			0.9	V
Logical "1" Strobe Input Current			$V_{STROBE} = 5.5V$, $V_{DIFF} = +3V$		0.01	5.0	μA
Logical "0" Strobe Input Current			$V_{STROBE} = 0V$, $V_{DIFF} = -3V$		−1.0	−1.4	mA
Output Short Circuit Current		0V	$V_{CC} = 5.5V$, $V_{STROBE} = 0V$	−2.8	−4.5	−6.7	mA
Propagation Delays (see waveforms)							
Differential Input to "0" Output			$V_{CC} = 5V$, $T_A = 25°C$		30	45	ns
Differential Input to "1" Output			$V_{CC} = 5V$, $T_A = 25°C$		24	40	ns
Strobe Input to "0" Output			$V_{CC} = 5V$, $T_A = 25°C$		16	25	ns
Strobe Input to "1" Output			$V_{CC} = 5V$, $T_A = 25°C$		18	30	ns

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the DM7820A, or 150°C/W and 115°C maximum junction temperature for the DM8820A

Note 2: These specifications apply for $4.5V \le V_{CC} \le 5.5V$, $-15V \le V_{CM} \le 15V$ and $-55°C \le T_A \le 125°C$ for the DM7820A or $0°C \le T_A \le 70°C$ for the DM8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently

Note 3: The specifications and curves given are for one side only Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Note 4: Min and max limits apply to absolute values.

Series 54/74

DM7822/DM8822 dual line receiver

general description

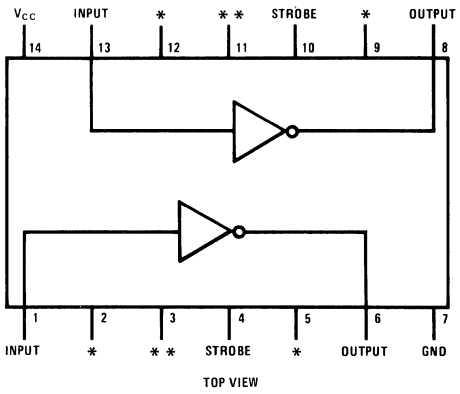
The DM7822/DM8822 is a dual inverting line receiver which meets the requirements of EIA specification RS232 Revision B The device contains both receivers on a single monolithic silicon chip The receivers share common power supply and ground connections, otherwise their operation is fully independent.

In addition to meeting the requirements of RS232, the DM7822/DM8822 also has independent strobe inputs which allow the receiver to be placed in the high state independent of the information being received at the input.

The output of the DM7822/DM8822 is completely compatible with five volt DTL and TTL logic families.

connection diagram

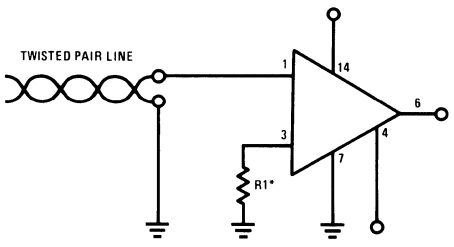
Dual-In-Line Package



TOP VIEW

*Make no connection to these pins.
**For operation requiring "Mark Hold" with the input open connect 470Ω resistors from each of these pins to ground

typical connection



*For Mark Hold R1 = 470Ω, otherwise connect pin 3 to ground

absolute maximum ratings

Supply Voltage		8 0V
Input Voltage		±30V
Strobe Voltage		8 0V
Output Sink Current		25 mA
Power Dissipation (Note 1)		600 mW
Operating Temperature Range	DM7822	−55°C to +125°C
	DM8822	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER	PARAGRAPH IN RS-232	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Input Threshold Voltage	4.8 (8)	$V_{OUT} \geq 2\ 5V$	−2 0			V
Positive Input Threshold Voltage (Note 3)		$V_{OUT} \leq 0\ 4V$			2 0	V
Input Resistance	4 5 and 4 8 (5)		3 0	5 0	7 0	kΩ
Input Current		V_{IN} = 25V V_{IN} = 0V V_{IN} = −25V	3.57 −8.33	5 0 −5	8 33 −3 57	mA mA mA
Open Circuit Input Voltage	4.5 and 4.8 (4)	V_{IN} = 0V		.03	0 5	V
Logical "1" Output Voltage		$I_{OUT} \leq -0.2$ mA	2 5			V
Logical "0" Output Voltage		I_{OUT} = 3 5 mA			0 4	V
Strobe Current		V_{STROBE} = 0V V_{STROBE} = 5.5V		1 0 −5 0 μA	1 4 −1 0 mA	mA
Power Supply Current (Both Receivers)		$-25V \leq V_{IN} \leq 25V$			24 0	mA
Response Time, t_1 or t_2		T_A = 25°C V_{CC} = 5 0V Input Ramp Rate ≤ 10 ns		65	125	ns

Note 1. For operating at elevated temperatures, the device must be derated in accordance with the "Maximum Power Dissipation" curve

Note 2. Min/Max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7822 and 0°C to 70°C for the DM8822 unless otherwise specified Likewise the limits apply across the guaranteed V_{CC} range of 4 5V to 5 5V for the DM7822 and 4 75V to 5 25V for the DM8822 unless otherwise specified Typical values are given for V_{CC} = 5 0V and T_A = 25°C

Note 3. Since the EIA RS-232 specification requires the threshold to be between −3V and +3V, the immunity limits shown here guarantee 1 volt additional noise immunity

Series 54/74

DM7830/DM8830 dual differential line driver

general description

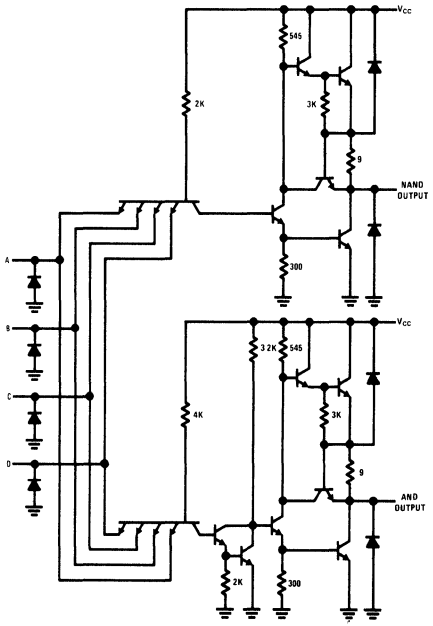
The DM7830/DM8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

features

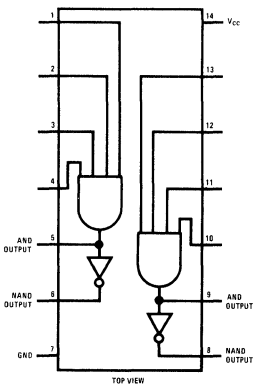
- Single 5 volt power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High Speed
- Short Circuit Protection

schematic* and connection diagrams



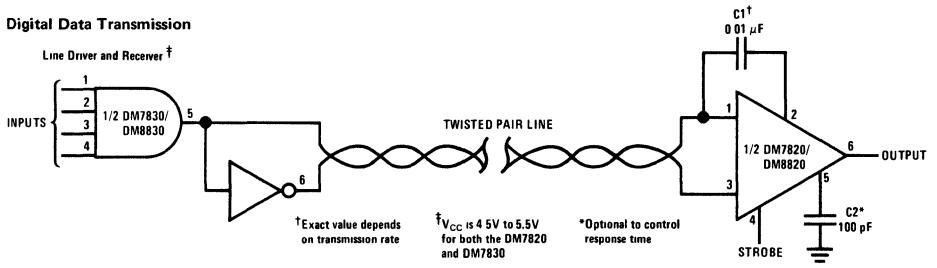
*2 per package

Dual-In-Line and Flat Package



typical application

Digital Data Transmission



absolute maximum ratings

V_{CC}		7.0V
Input Voltage		5.5V
Operating Temperature	DM7830	−55°C to +125°C
	DM8830	0°C to 70°C
Storage Temperature		−65°C to +150°C
Lead Temperature (soldering, 60 sec)		300°C
Output Short Circuit Duration (125°C)		1 second

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.0			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage	V_{IN} = 0.8V I_{OUT} = −0.8 mA	2.4			V
Logical "1"Output Voltage	V_{IN} = 0.8V I_{OUT} = 40 mA	1.8	3.3		V
Logical "0" Output Voltage	V_{IN} = 2.0V I_{OUT} = +32 mA		0.2	0.4	V
Logical "0" Output Voltage	V_{IN} = 2.0V I_{OUT} = +40 mA		0.22	0.5	V
Logical "1" Input Current	V_{IN} = +2.4V			120	μA
Logical "1" Input Current	V_{IN} = 5.5V			2	mA
Logical "0" Input Current	V_{IN} = 0.4V			4.8	mA
Output Short Circuit Current	V_{CC} = 5.0V	Note 2 40	100	Note 2 120	mA
Supply Current	V_{IN} = 5.0V (Each Driver)		11	18	mA
Propagation Delay AND Gate t_{pd1}	T_A = 25°C		8	12	ns
t_{pd0}	V_{CC} = 5.0V		11	18	ns
Propagation Delay NAND Gate t_{pd1}	C_L = 15 pF		8	12	ns
t_{pd0}	See Figure 1		5	8	ns
Differential Delay t_1	Load, 100Ω and 5000 pF		12	16	ns
Differential Delay t_2	See Figure 2		12	16	ns

Note 1: Specifications apply for DM7830 −55°C ≤ T_A ≤ +125°C, V_{CC} = +5V ±10%, DM8830 0°C ≤ T_A ≤ 70°C, V_{CC} = +5V ±5% unless otherwise stated. Typical values given are for T_A = 25°C, V_{CC} = 5.0V.

Note 2: Applies for T_A = +125°C only

Series 54/74

DM7831/DM8831,DM7832/DM8832 TRI-STATE® line drivers

general description

Through simple logic control, the DM7831/DM8831, DM7832/DM8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DM7832/DM8832 does not have the V_{CC} clamp diodes found on the DM7831/DM8831.

The DM7831 & DM7832 are specified for operation over the −55°C to +125°C military temperature range. The DM8831 & DM8832 are specified for operation over the 0°C to +70°C temperature range.

features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

mode of operation

To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

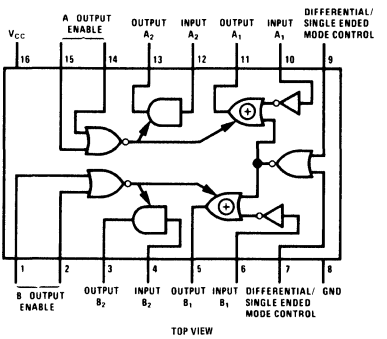
To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected to-In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(Continued)

connection and logic diagram

Dual-In-Line and Flat Package



TOP VIEW

truth-table (Shown for A Channels Only)

"A" OUTPUT DISABLE		DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL		INPUT A_1	OUTPUT A_1	INPUT A_2	OUTPUT A_2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A_1	Logical "1" or Logical "0"	Same as Input A_2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A_1	Logical "1" or Logical "0"	Same as Input A_2
1 X	X 1	X	X	X	High impedance state	X	High impedance state

X = Don't Care

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5 5V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7831, DM7832	−55°C to +125°C
	DM8831, DM8832	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously		∞

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7831,DM7832	V_{CC} = 4 5V		2 0			V
	DM8831,DM8832	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM7831,DM7832	V_{CC} = 4 5V				0 8	V
	DM8831,DM8832	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM7831,DM7832	V_{CC} = 4 5V	I_0 = −40 mA	1 8	2 3		V
			I_0 = −2 mA	2 4	2 7		V
	DM8831,DM8832	V_{CC} = 4 75V	I_0 = −40 mA	1 8	2 5		V
			I_0 = −5 2 mA	2 4	2 9		V
Logical "0" Output Voltage	DM7831,DM7832		I_0 = 40 mA		0 29	0 50	V
			I_0 = 32 mA			40	V
	DM8831,DM8832		I_0 = 40 mA		0 29	0 50	V
			I_0 = 32 mA			40	V
Logical "1" Input Current	DM7831,DM7832	V_{CC} = 5 5V	V_{IN} = 5 5V			1	mA
	DM8831,DM8832	V_{CC} = 5 25V	V_{IN} = 2 4V			40	μA
Logical "0" Input Current	DM7831,DM7832	V_{CC} = 5 5V	V_{IN} = 0 4V		−1 0	−1 6	mA
	DM8831,DM8832	V_{CC} = 5 25V					
Output Disable Current	DM7831,DM7832	V_{CC} = 5 5V	V_O = 2 4V or 0 4V	−40		40	μA
	DM8831,DM8832	V_{CC} = 5 25V					
Output Short Circuit Current	DM7831,DM7832	V_{CC} = 5 5V		−40	−100	−120	mA
	DM8831,DM8832	V_{CC} 5 25V		(Note 2)		(Note 2)	
Supply Current	DM7831,DM7832	V_{CC} = 5 5V			65	90	mA
	DM8831,DM8832	V_{CC} = 5 25V					
Input Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C I_{IN} = −12 mA				−1 5	V
Output Diode Clamp Voltage	DM7831,DM7832	I_{OUT} = −12 mA, V_{CC} = 5 0V, T_A = 25°C				−1 5	V
	DM8831,DM8832	I_{OUT} = +12 mA, V_{CC} = 5 0V, T_A = 25°C				V_{CC}+1 5	V
Propagation Delay to a Logical "0" from Inputs A_1, A_2, B_1, B_2 Differential Single-ended Mode Control to Outputs, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C			13	25	ns
Propagation Delay to a Logical "1" from Inputs A_1, A_2, B_1, B_2 Differential Single-ended Mode Control to Outputs, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C			13	25	ns
Delay from Disable Inputs to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0V, T_A = 25°C			6	12	ns
Delay from Disable Inputs to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V, T_A = 25°C			14	22	ns
Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5,0V, T_A = 25°C			14	22	ns
Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State), t_{HO}		V_{CC} = 5 0V, T_A = 25°C			18	27	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7831, DM7832 and across the 0°C to 70°C temperature range for the DM8831, DM8832. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 2. Applies for T_A = 125°C only Only one output should be shorted at a time

mode of operation (cont.)

DM7831/DM8831's, DM7832/DM8832's (Figure 1), all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DM7831/DM8831's, DM7832/DM8832's (Figure 2).

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs 400 μA), the output is easily able to supply that leakage current for several hundred other DM7831/DM8831's, DM7832/DM8832's and still have available drive for the bus line (Figure 3).

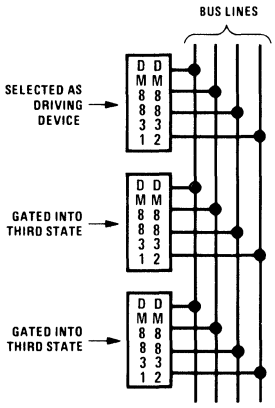


Figure 1

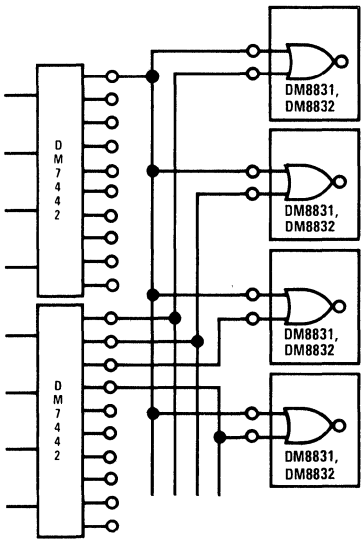


Figure 2

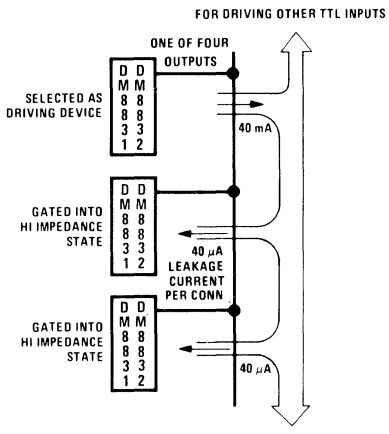


Figure 3

Series 54/74

DM7836/DM8836 quad NOR unified bus receiver

general description

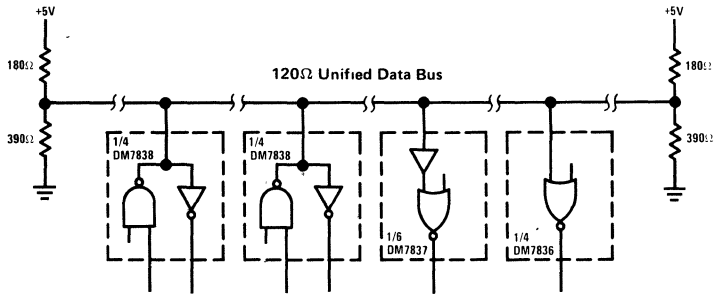
The DM7836/DM8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. This receiver has been specifically configured to replace the SP380 gate pin-for-pin to provide the distinct advantages of the DM7837 receiver design in existing systems.

features

- Plug-in replacement for SP380 gate
- Low input current with normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- DTL/TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

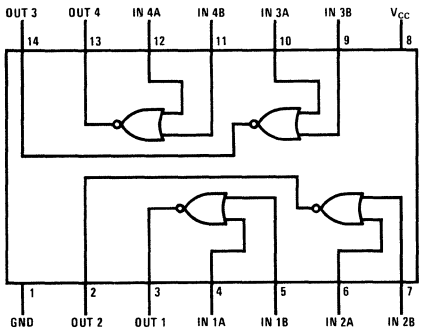
1

typical application



connection diagram

Dual-In-Line Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Power Dissipation	600 mW
Operating temperature range:	
DM7836	−55°C to +125°C
DM8836	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$, unless otherwise specified (Note 2)

PARAMETER	INPUT	OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
High Level Input Threshold							
DM7836	V_{TH}	16 mA	Output < 0 4V	1.65	2 25	2.65	V
DM8836	V_{TH}	16 mA	Output < 0 4V	1 80	2.25	2 50	V
Low Level Input Threshold							
DM7836	V_{TH}	−400 μA	Output > 2 4V	0 97	1 30	1.63	V
DM8836	V_{TH}	−400 μA	Output > 2 4V	1.05	1 30	1.55	V
Maximum Input Current	4V		$V_{CC} = V_H$		15	50	μA
Maximum Input Current	4V		$V_{CC} = 0V$		1	50	μA
Logic "1" Output Voltage	0 5V	−400 μA		2 4			V
Logic "0" Output Voltage	4V	16 mA			0 25	0.4	V
Output Short Circuit Current	0 5V	0V	$V_{CC} = V_H$	−18		- 55	mA
Power Supply Current	4V		Per Package		25	40	mA
Input Clamp Diode Voltage	−12 mA		$T_A = 25°C$		−1	−1 5	V
The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified							
Propagation Delays							
Input to Logic "1" Output			Note 3		20	30	ns
Input to Logic "0" Output			Note 4		18	30	ns

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the reference pin.
Note 2: For DM7836: $V_L = 4.5V$, $V_H = 5.5V$, $T_L = -55°C$, $T_H = +125°C$.
For DM8836. $V_L = 4.75V$, $V_H = 5.25V$, $T_L = 0°C$, $T_H = +70°C$.
Note 3: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.
Note 4: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Series 54/74

DM7837/DM8837 hex unified bus receiver

general description

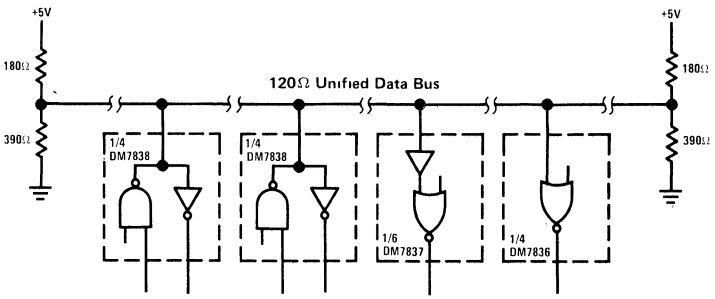
The DM7837/DM8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are DTL/TTL compatible.

features

- Low receiver input current for normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- DTL/TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

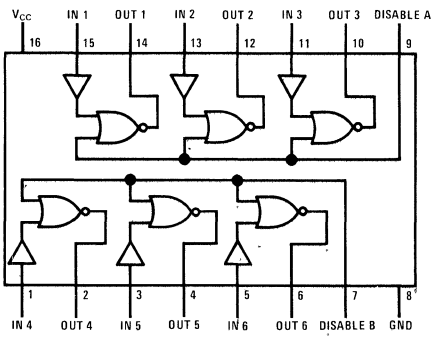
1

typical application



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Power Dissipation	600 mW
Operating Temperature Range	
DM7837	−55°C to +125°C
DM8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$, unless otherwise specified (Note 2)

PARAMETER	RECEIVER INPUT	DISABLE INPUT	OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
High Level Receiver Threshold DM7837	V_{TH}	0 8V	16 mA	Output < 0 4V	1 65	2 25	2 65	V
High Level Receiver Threshold DM8837	V_{TH}	0 8V	16 mA	Output < 0 4V	1 80	2 25	2 50	V
Low Level Receiver Threshold DM7837	V_{TH}	0 8V	−400 mA	Output > 2 4V	0 97	1 30	1 63	V
Low Level Receiver Threshold DM8837	V_{TH}	0 8V	−400 mA	Output > 2 4V	1 05	1 30	1 55	V
Maximum Receiver Input Current	4V			$V_{CC} = V_H$		15 0	50 0	μA
Maximum Receiver Input Current	4V			V_{CC} = 0V		1 0	50 0	μA
Logic "1" Input Voltage Disable	0 5V	V_{IN}	16 mA	Output < 0 4V	2 0			V
Logic "0" Input Voltage Disable	0 5V	V_{IN}	−400 μA	Output > 2 4V			0 8	V
Logic "1" Output Voltage	0 5V	0 8V	−400 μA		2 4			V
Logic "0" Output Voltage	4V	0 8V	16 mA			0 25	0 4	V
Logic "1" Input Current Disable		2 4V					80 0	μA
Logic "1" Input Current: Disable		5 5V					2.0	mA
Logic "0" Input Current Disable	4V	0 4V					−3 2	mA
Output Short Circuit Current	0 5V	0V	0V	$V_{CC} = V_H$	−18 0		−55 0	mA
Power Supply Current	4V	0V		Per Package		45 0	60.0	mA
Input Clamp Diode	−12 mA	−12 mA		T_A = 25°C		−1 0	−1 5	V
The following apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified								
Propagation Delays								
Receiver Input to Logic "1" Output		0V		Note 3		20	30	ns
Receiver Input to Logic "0" Output		0V		Note 4		18	30	ns
Disable Input to Logic "1" Output	0V			Note 5		9	15	ns
Disable Input to Logic "0" Output	0V			Note 5		4	10	ns

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: For DM7837: V_L = 4.5V, V_H = 5.5V, T_L = −55°C, T_H = +125°C
For DM8837: V_L = 4.75V, V_H = 5.25V, T_L = 0°C, T_H = +70°C

Note 3: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 4: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Series 54/74

DM7838/DM8838 quad unified bus transceiver

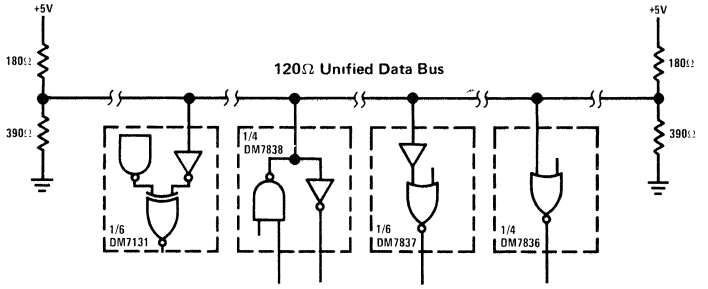
general description

The DM7838/DM8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously

features

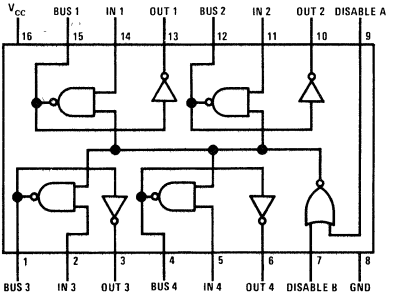
- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

typical application



connection diagram

Dual In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Supply Voltage	7V	Operating Temperature Range	
Input and Output Voltage	5 5V	DM7838	−55°C to +125°C
Power Dissipation	600 mW	DM8838	0°C to +70°C
		Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

DM7838/DM8838 The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$ unless otherwise specified (Note 2).

PARAMETER	DISABLE INPUT	DRIVER INPUT	BUS PIN	RECEIVER OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
Logic "1" Input Voltage Disable	V_{IN}	2V	4V		Bus < 100 μA	2 0			V
Logic "0" Input Voltage Disable	V_{IN}	2V	50 mA		Bus < 0 7V			0 8	V
Logic "1" Input Voltage. Driver	0.8V	V_{IN}	50 mA		Bus < 0 7V	2 0			V
Logic "0" Input Voltage Driver	0 8V	V_{IN}	4V		Bus < 100 μA			0 8	V
High Level Receiver Threshold DM7838		0 8V	V_{TH}	16 mA	Receiver output < 0 4V	1 65	2 25	2 65	V
High Level Receiver Threshold DM8838		0 8V	V_{TH}	16 mA	Receiver output < 0 4V	1 80	2 25	2 50	V
Low Level Receiver Threshold. DM7838		0 8V	V_{TH}	−400 μA	Receiver output > 2 4V	0 97	1 30	1 63	V
Low Level Receiver Threshold DM8838		0 8V	V_{TH}	−400 μA	Receiver output > 2 4V	1 05	1 30	1 55	V
Logic "1" Input Current Disable and Driver	5 5V	5 5V						1	mA
Logic "1" Input Current. Disable and Driver	2 4V	2 4V						40	μA
Logic "0" Input Current Disable and Driver	0 4V	0 4V						−1 6	mA
Maximum Bus Current	0 8V	0 8V	4V		$V_{CC} = V_H$		20	100	μA
Maximum Bus Current	0 8V	0 8V	4V		$V_{CC} = 0V$		2	100	μA
Low Level Bus Voltage	0 8V	2V	50 mA				0 4	0 7	V
Logic "1" Output Voltage Receiver	0 8V	0 8V	0 5V	−400 μA		2 4			V
Logic "0" Output Voltage Receiver	0 8V	0 8V	4V	16 mA			0 25	0.4	V
Output Short Circuit Current. Receiver	0.8V	0.8V	0 5V	0V	$V_{CC} = V_H$	−18		−55	mA
Supply Current	0V	2V			Per Package		50	70	mA
Input Diode Clamp Voltage	−12 mA	−12 mA	−12 mA		$T_A = 25°C$		−1	−1 5	V
The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified									
Propagation Delays									
Disable to Bus "1"					Note 3		19	30	ns
Disable to Bus "0"					Note 3		15	23	ns
Driver Input to Bus "1"					Note 3		17	25	ns
Driver Input to Bus "0"					Note 3		9	15	ns
Bus to Logic "1" Receiver Output					Note 4		20	30	ns
Bus to Logic "0" Receiver Output					Note 5		18	30	ns

Note 1 Voltage values are with respect to network ground terminal Positive current is defined as current into the referenced pin

Note 2: For DM7838 $V_L = 4\ 5V$, $V_H = 5\ 5V$, $T_L = -55°C$, $T_H = 125°C$
For DM8838 $V_L = 4\ 75V$, $V_H = 5\ 25$, $T_L = 0°C$, $T_H = 70°C$

Note 3 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 1\ 5V$ to $V_{BUS} = 1\ 5V$, $V_{IN} = 0V$ to 3V pulse

Note 4 Fan-out of 10 load, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 1\ 3V$ to $V_{OUT} = 1\ 5V$, $V_{IN} = 0V$ to 3V pulse

Note 5 Fan-out of 10 load, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 2\ 3V$ to $V_{OUT} = 1\ 5V$, $V_{IN} = 0V$ to 3V pulse

Series 54/74

DM7875A/DM8875A and DM7875B/DM8875B TRI-STATE® 4-bit multipliers

general description

The DM7875A/DM8875A & DM7875B/DM8875B are two integrated circuits which together will multiply two four-bit binary numbers. Since the largest number that can be obtained by multiplying two four-bit numbers is 225 (15 x 15), the eight output pins (four from each package) are sufficient to produce this number. Both multiplier and multiplicand are connected to the eight input pins of each package

A gated two-input strobe control is provided. When either of the two inputs is taken to the logical "1" state, the outputs will all be placed in the high impedance state. In this state both the upper and lower output transistors are turned off, providing a high output impedance. This allows multiple devices to be connected to a common bus line, and since only one multiplier-pair at a time is allowed to be in the conventional low-impedance state, the advantages of TTL outputs can be combined with a bus structured system.

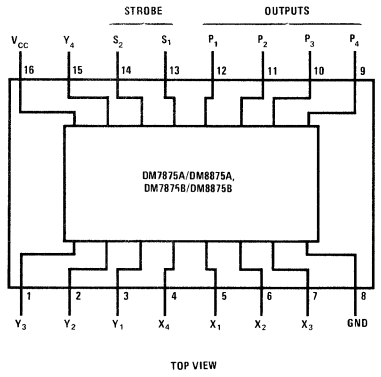
The DM7875A/DM8875A provides the most significant four bits and the DM7875B/DM8875B the least significant four bits.

features

- 36 ns typical propagation delay
- 375 mW typical power dissipation (each package)
- Series 54/74 compatible
- Outputs directly connectable to a common bus line

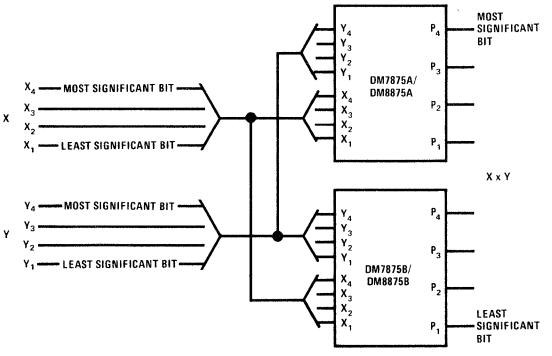
connection diagram

Dual-In-Line Package



TOP VIEW

typical application



absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM7875A, DM7875B	−55°C to +125°C
	DM8875A, DM8875B	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7875A, DM7875B	V_{CC} = 4.5V		2.0			V
	DM8875A, DM8875B	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7875A/DM7875B	V_{CC} = 4.5V				0.8	V
	DM8875A, DM8875B	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7875A, DM7875B	V_{CC} = 4.5V, I_O = −2.0 mA		2.4			V
	DM8875A, DM8875B	V_{CC} = 4.75V, I_O = −5.2 mA					
Logical "0" Output Voltage	DM7875A, DM7875B	V_{CC} = 4.5V	I_O = 16 mA			0.4	V
	DM8875A, DM8875B	V_{CC} = 4.75V					
Third State Output Current	DM7875A, DM7875B	V_{CC} = 5.5V	V_O = 2.4V			40	μA
	DM8875A, DM8875B	V_{CC} = 5.25V	V_O = 0.4V			−40	μA
Logical "1" Input Current	DM7875A, DM7875B	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8875A, DM8875B	V_{CC} = 5.25V					
	DM7875A, DM7875B	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8875A, DM8875B	V_{CC} = 5.25V					
Logical "0" Input Current	DM7875A, DM7875B	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.2	mA
	DM8875A, DM8875B	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7875A, DM7875B	V_{CC} = 5.5V	V_O = 0.0V	−20		−70	mA
	DM8875A, DM8875B	V_{CC} = 5.25V					
Supply Current (each device)	DM7875A, DM7875B	V_{CC} = 5.5V	All Inputs at GND		75	110	mA
	DM8875A, DM8875B	V_{CC} = 5.25V					
Input Clamp Voltage	DM7875A, DM7875B	V_{CC} = 4.5	I_{IN} = −12 mA			−1.5	V
	DM8875A, DM8875B	V_{CC} = 4.25					
Output V_{CC} Clamp Voltage	DM7875A, DM7875B	V_{CC} = 5.5V	I_O = 12 mA			V_{CC}+1.5	V
	DM8875A, DM8875B	V_{CC} = 5.25V					
Output Ground Clamp Voltage	DM7875A, DM7875B	V_{CC} = 5.5V	I_O = −12 mA			−1.5	V
	DM8875A, DM8875B	V_{CC} = 5.25V					
Propagation Delay to a Logical "0" from X, Y Inputs to Outputs, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C			39	60	ns
Propagation Delay to a Logical "1" from X, Y Inputs to Outputs, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C			31	60	ns
Delay from Strobe to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V, T_A = 25°C			30		ns
Delay from Strobe to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V, T_A = 25°C			10		ns
Delay from Strobe to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V, T_A = 25°C			30		ns
Delay from Strobe to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V, T_A = 25°C			30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7875A, DM7875B and across the 0°C to 70°C range for the DM8875A, DM8875B. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM7880/DM8880 high voltage 7-segment decoder/driver (for driving Sperry and Panaplex II™ displays)

general description

The DM7880/DM8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

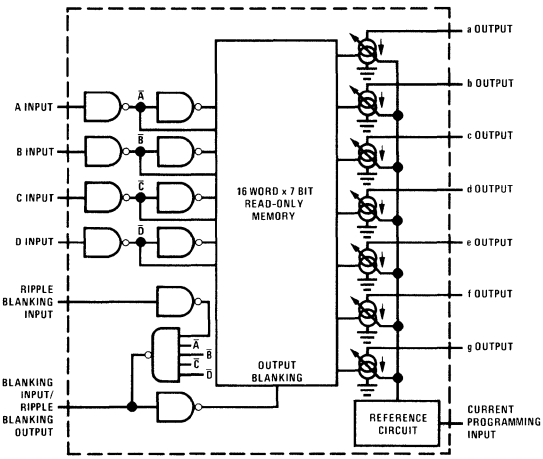
Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

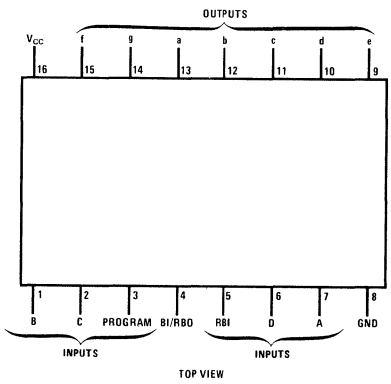
features

- Current sink outputs
- Adjustable output current — 0.2 to 1.5 mA
- High output breakdown voltage — 110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

logic and connection diagrams



Dual-In-Line Package



absolute maximum ratings

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation (Note 1)	600 mW
Transient Segment Output Current (Note 2)	50 mA
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7880	4.5	5.5	V
DM8880	4 75	5.25	V
Temperature (T_A)			
DM7880	−55	+125	°C
DM8880	0	+70	°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = Min	2 0			V
Logic "0" Input Voltage	V_{CC} = Min			0.8	V
Logic "1" Output Voltage (RBO)	V_{CC} = Min, I_{OUT} = −200 μA	2 4	3 7		V
Logic "0" Output Voltage (RBO)	V_{CC} = Min, I_{OUT} = 8 mA		0.13	0.4	V
Logic "1" Input Current (Except BI)	V_{CC} = Max, V_{IN} = 2 4V V_{CC} = Max, V_{IN} = 5 5V		2 4	15 400	μA μA
Logic "0" Input Current (Except BI)	V_{CC} = Max, V_{IN} = 0 4V		−300	−600	μA
Logic "0" Input Current (BI)	V_{CC} = Max, V_{IN} = 0 4V		−1 2	−2 0	mA
Power Supply Current	V_{CC} = Max, R_P = 2 2k All Inputs = 0V		27	43	mA
Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C I_{IN} = −12 mA		−0 9	−1 5	V
Segment Outputs					
Outputs a, f, g ON Current Ratio	All Outputs = 50V Output b Curr. = Ref	0.84	0.93	1.02	
Output c ON Current Ratio	All Outputs = 50V, Output b Curr = Ref.	1.12	1.25	1.38	
Output d ON Current Ratio	All Outputs = 50V Output b Curr = Ref.	0.90	1 00	1.10	
Output e ON Current Ratio	All Outputs = 50V Output b Curr = Ref.	0.99	1 10	1.21	
Output b ON Current	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 18 1k	0 18	0 20	0.22	mA
	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 7 03k	0 45	0 50	0.55	mA
	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 3 40k	0.90	1 00	1 10	mA
	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 2 20k	1 35	1.50	1 65	mA
Output Saturation Voltage	V_{CC} = Min, R_P = 1k±5% I_{OUT} b = 2 mA (Note 4)		0.8	2 5	V
Output Leakage Current	V_{OUT} = 75V, BI = 0V		.003	3	μA
Output Breakdown Voltage	I_{OUT} = 250 μA, BI = 0V	80	110		V
Propagation Delays					
BCD Input to Segment Output	V_{CC} = 5V, T_A = 25°C		0.4	10	μs
BI to Segment Output	V_{CC} = 5V, T_A = 25°C		0.4	10	μs
RBI to Segment Output	V_{CC} = 5V, T_A = 25°C		0.7	10	μs
RBI to RBO	V_{CC} = 5V, T_A = 25°C		0 4	10	μs

Note 1 Maximum junction temperature for DM7880 is 150°C whereas that for DM8880 is 130°C For operating at elevated temperatures the device must be derated based on a thermal resistance of 85°C/W Θ_{JA} for DM7880 and 150°C/W Θ_{JA} for DM8880

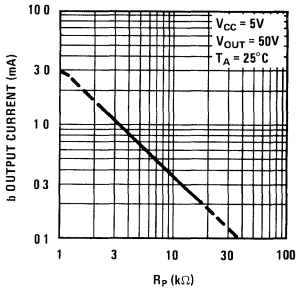
Note 2 In all applications transient segment output current must be limited to 50 mA This may be accomplished in DC applications by connecting a 2 2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications

Note 3 Min/max limits apply across the guaranteed operating temperature range of −55°C to 125°C for DM7880 and 0°C to 70°C for DM8880, unless otherwise specified Typicals are for V_{CC} = 5V, T_A = 25°C Positive current is defined as current into the referenced pin

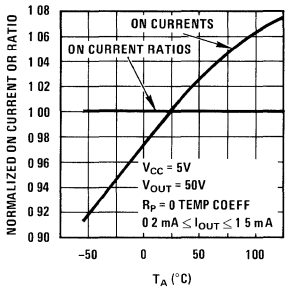
Note 4 For saturation mode the segment output currents are externally limited and ratioed

typical performance characteristics

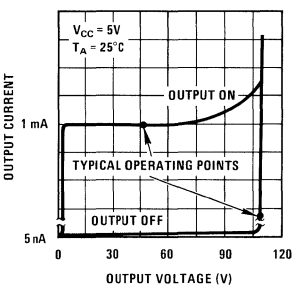
Output Current Programming



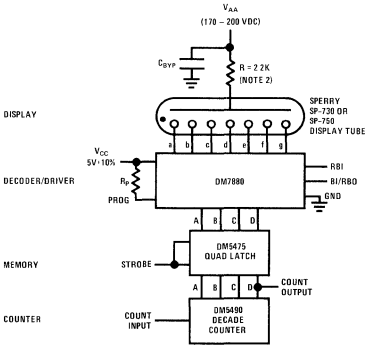
On Currents vs Temperature



Output Characteristic

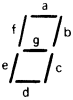


typical application



truth table

DECIMAL OR FUNCTION	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI	X	X	X	X	X	0	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	



SEGMENT IDENTIFICATION

Series 54/74

DM8884A high voltage cathode decoder/driver (for driving Sperry and Panaplex II™ displays) general description

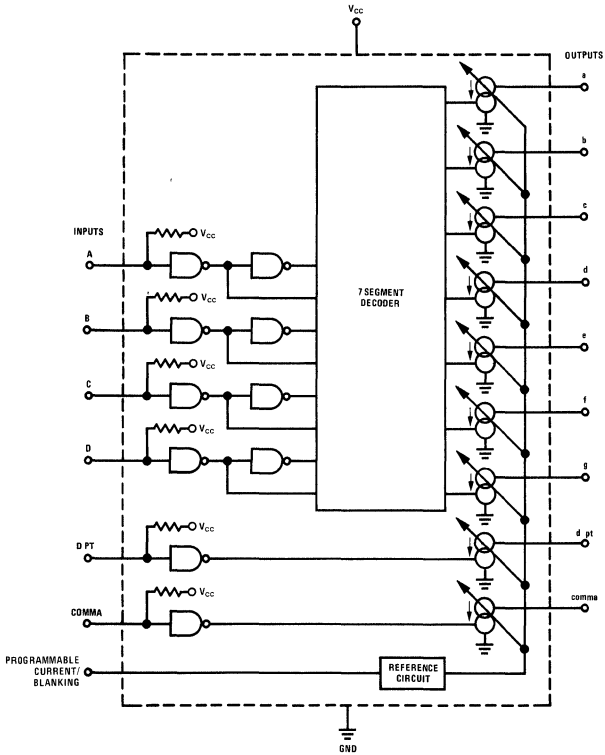
The DM8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays. Two separate inputs are provided for driving the decimal point and comma cathodes.

All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve.

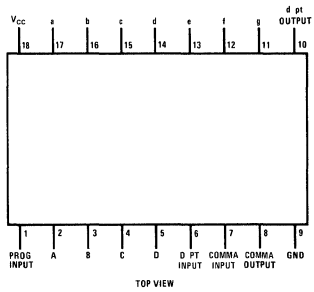
features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation.
- Input pullups increase noise immunity

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

V_{CC}	7V
Input Voltage (Note 1)	V_{CC}
Segment Output Voltage	80V
Power Dissipation (Note 2)	600 mW
Transient Segment Output Current (Note 3)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics ($0°C \leq T_A \leq 70°C$ – Unless otherwise noted), $V_{CC} = 5V \pm 5\%$

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = 4 75V	2 0		V
Logic "0" Input Voltage	V_{CC} = 4 75V		1 0	V
Logic "1" Input Current	V_{CC} = 5 25V, V_{IN} = 2 4V		15	μA
Positive Input Clamp Voltage	V_{CC} = 4 75, I_{IN} = 1 mA	5 0		V
Logic "0" Input Current	V_{CC} = 5 25V, V_{IN} = 0 4V		−250	μA
Power Supply Current	V_{CC} = 5 25V, R_P = 2 8k, All Inputs = 5V		40	mA
Negative Input Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C		−1 5	V
Segment Outputs				
All Outputs ON Current Ratio	All Outputs = 50V Output b Current = Ref	0 9	1 1	
Output b ON Current	V_{CC} = 5V, V_{OUT} b = 50V,			
	T_A = 25°C, R_P = 18 1k	0 18	0 22	mA
	R_P = 7 03k	0 45	0 55	mA
	R_P = 3 40k	0 90	1 10	mA
	R_P = 2 80k	1 08	1 32	mA
Output Leakage Current	V_{OUT} = 75V		5	μA
Output Breakdown Voltage	I_{OUT} = 250 μA	80		V
Propagation Delay.				
Any Input to Segment Output	V_{CC} = 5V, T_A = 25°C		10	μs

Note 1 This limit can be higher for a current limiting voltage source

Note 2 The maximum junction temperature is 140°C For operation at elevated temperatures, the device must be derated based on a thermal resistance of 140°C/W θ JA

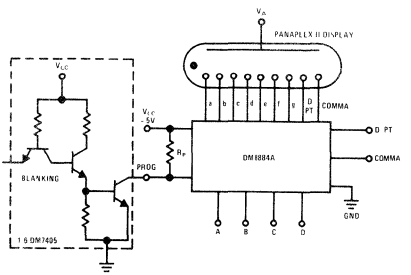
Note 3 In all applications transient segment output current must be limited to 50 mA This may be accomplished in DC applications by connecting a 2 2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications

truth table

FUNCTION	D PT	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	1	1	0	0	1	1	1	1	1
2	1	1	0	0	1	0	0	0	1	0	0	1	0	2
3	1	1	0	0	1	1	0	0	0	0	1	1	0	3
4	1	1	0	1	0	0	1	0	0	1	1	0	0	4
5	1	1	0	1	0	1	0	1	0	0	1	0	0	5
6	1	1	0	1	1	0	0	1	0	0	0	0	0	6
7	1	1	0	1	1	1	0	0	0	1	1	1	1	7
8	1	1	1	0	0	0	0	0	0	0	0	0	0	8
9	1	1	1	0	0	1	0	0	0	0	1	0	0	9
10	1	1	1	0	1	0	1	1	0	0	0	1	1	-
11	1	1	1	0	1	1	1	1	0	0	0	1	0	-
12	1	1	1	1	0	0	0	0	1	1	1	0	0	-
13	1	1	1	1	0	1	0	1	1	0	0	0	0	-
14	1	1	1	1	1	0	1	1	1	1	1	1	0	-
15	1	1	1	1	1	1	1	1	1	1	1	1	1	
*D PT	0	1	X	X	X	X	X	X	X	X	X	X	X	.
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	,

*Decimal point and comma can be displayed with or without any numeral

typical application



typical performance characteristics (see DM7880 data sheet)

Series 54/74

DM8885 MOS to high voltage cathode buffer

general discription

The DM8885 interfaces MOS calculator or counter-latch-decoder-driver circuits directly to seven-segment high-voltage gas-filled displays The six inputs A, B, D, E, F, G are decoded to drive the seven segments of the tube.

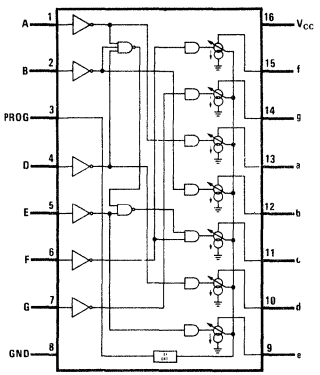
Each output constitutes a switchable, adjustable current source which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation These current sources have a voltage compliance from 3V to at least 80V. Each current source is ratioed to the b-output current as required for even illumination of all segments. Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting a program resistor (R_P) from V_{CC} to the program input.

features

- Current source outputs
- Adjustable output currents 0.2 to 1.5 mA
- High output breakdown voltage 80V min
- Suitable for multiplex operation
- Low fan-in and low power
- Blanking via program input
- Also drives overrange, polarity, decimal point cathodes

connection diagram

Dual-In-Line Package



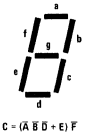
TOP VIEW

truth tables

A	B	D	E	F	G	DISPLAY
1	1	1	1	1	0	0
0	1	0	0	0	0	1
1	1	1	1	0	1	2
1	1	1	0	0	1	3
0	1	0	0	1	1	4
1	0	1	0	1	1	5
1	0	1	1	1	1	6
1	1	0	0	0	0	7
1	1	1	1	1	1	8
1	1	1	0	1	1	9
0	0	1	1	1	1	b
1	1	0	0	1	1	q
1	1	0	1	1	1	A
0	1	0	1	1	1	H
0	1	1	1	1	0	U
0	0	0	0	0	1	-
0	0	0	0	0	0	

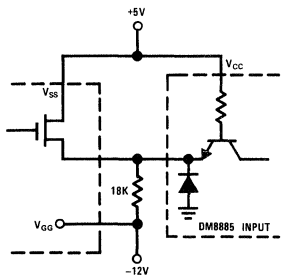
INPUT*	OUTPUT*
0	1 (OFF)
1	0 (ON)

*Positive Logic

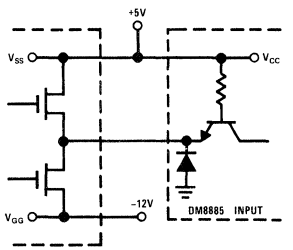


$C = (\bar{A}\,\bar{B}\,\bar{D} + E)\,\bar{F}$

typical applications



Open-Drain MOS Output



Push-Pull MOS Output

absolute maximum ratings

V_{CC}	7V
Input Voltage	6V
Segment Output Voltage	80V
Power Dissipation (Note 1)	600 mW
Transient Segment Output Current (Note 2)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = 4 75V	2 0			V
Logic "0" Input Voltage	V_{CC} = 4 75V			0 8	V
Logic "1" Input Current	V_{CC} = 5 25V, V_{IN} = 2 4V		2	15	μA
	V_{CC} = 5 25V, V_{IN} = 5 5V		4	400	μA
Logic "0" Input Current	V_{CC} = 5 25V, V_{IN} = 0 4V		-300	-600	μA
Power Supply Current	V_{CC} = 5 25V, All Inputs = 0V, R_P = 2 2k		22	31	mA
Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C		-0 9	-1 5	V
Segment Outputs					
Outputs a, f, g On Current Ratio	All Outputs = 50V, Output b Curr = Ref	0 84	0 93	1 02	
Output c On Current Ratio	All Outputs = 50V, Output b Curr = Ref	1 12	1 25	1 38	
Output d On Current Ratio	All Outputs = 50V, Output b Curr = Ref	0 90	1 00	1 10	
Output e On Current Ratio	All Outputs = 50V, Output b Curr = Ref	0 99	1 10	1 21	
Output b On Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 18 1k	0 18	0 20	0 22	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 7 03k	0 45	0 50	0 55	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 3 40k	0 90	1 00	1 10	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 2 20k	1 35	1 50	1 65	mA
Output Saturation Voltage	V_{CC} = 4 75V, I_{OUT} b = 2 mA, R_P = 1k ± 5% (Note 4)		0 8	2 5	V
Output Leakage Current	V_{OUT} = 75V, V_{IN} = 0 8V, $R_P \geq$ 1k		0 003	3	μA
	V_{OUT} = 75V, V_{PROG} = 0 4V		0 003	3	μA
Output Breakdown Voltage	I_{OUT} = 250 μA, V_{IN} = 0 8V	80	110		V
Propagation Delays					
Input to Segment Output	V_{CC} = 5V, T_A = 25°C		0 4	10	μs

Note 1: Maximum junction temperature is 130°C. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 150°C/W θ_{JA}.

Note 2: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in DC applications by connecting a 2 2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +70°C, unless otherwise specified Typicals are for V_{CC} = 5V, T_A = 25°C Positive current is defined as current into the referenced pin

Note 4: For saturation mode the segment output currents are externally limited and ratioed

typical performance characteristics (see DM7880 data sheet)

Series 54H/74H

REFERENCE

The following table references all Physical Dimension Drawings, Waveforms, and Test Circuits for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
		Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type		Fig.	Pg.	Fig.	Pg.
DM54H00	2-1	3	II	11	IV	J								2-9		2-7	
DM74H00	2-1	3	II	11	IV	J								2-9		2-7	
DM54H01	2-1	3	II	11	IV	J								2-9		2-7	
DM74H01	2-1	3	II	11	IV	J								2-9		2-7	
DM54H04	2-1	3	II	11	IV	J								2-9		2-7	
DM74H04	2-1	3	II	11	IV	J								2-9		2-7	
DM54H05	2-1	3	II	11	IV	J								2-9		2-7	
DM74H05	2-1	3	II	11	IV	J								2-9		2-7	
DM54H08	2-1	3	II	11	IV	J								2-9		2-7	
DM74H08	2-1	3	II	11	IV	J								2-9		2-7	
DM54H10	2-1	3	II	11	IV	J								2-9		2-7	
DM74H10	2-1	3	II	11	IV	J								2-9		2-7	
DM54H11	2-1	3	II	11	IV	J								2-9		2-7	
DM74H11	2-1	3	II	11	IV	J								2-9		2-7	
DM54H20	2-1	3	II	11	IV	J								2-9		2-7	
DM74H20	2-1	3	II	11	IV	J								2-9		2-7	
DM54H21	2-1	3	II	11	IV	J								2-9		2-7	
DM74H21	2-1	3	II	11	IV	J								2-9		2-7	
DM54H22	2-1	3	II	11	IV	J								2-9		2-7	
DM74H22	2-1	3	II	11	IV	J								2-9		2-7	
DM54H30	2-1	3	II	11	IV	J								2-9		2-7	
DM74H30	2-1	3	II	11	IV	J								2-9		2-7	
DM54H40	2-1	3	II	11	IV	J								2-9		2-7	
DM74H40	2-1	3	II	11	IV	J								2-9		2-7	
DM54H50	2-6	3	II	11	IV	J								2-9		2-7	
DM74H50	2-6	3	II	11	IV	J								2-9		2-7	
DM54H51	2-6	3	II	11	IV	J								2-9		2-7	
DM74H51	2-6	3	II	11	IV	J								2-9		2-7	
DM54H52	2-6	3	II	11	IV	J								2-9		2-7	
DM74H52	2-6	3	II	11	IV	J								2-9		2-7	
DM54H53	2-6	3	II	11	IV	J								2-9		2-7	
DM74H53	2-6	3	II	11	IV	J								2-9		2-7	
DM54H54	2-6	3	II	11	IV	J								2-9		2-7	
DM74H54	2-6	3	II	11	IV	J								2-9		2-7	
DM54H55	2-6	3	II	11	IV	J								2-9		2-7	
DM74H55	2-6	3	II	11	IV	J								2-9		2-7	
DM54H60	2-6	3	II	11	IV	J								2-9		2-7	
DM74H60	2-6	3	II	11	IV	J								2-9		2-7	
DM54H61	2-6	3	II	11	IV	J								2-9		2-7	
DM74H61	2-6	3	II	11	IV	J								2-9		2-7	
DM54H62	2-6	3	II	11	IV	J								2-9		2-7	
DM74H62	2-6	3	II	11	IV	J								2-9		2-7	
DM54H71	2-6	3	II	11	IV	J								2-9		2-7	
DM74H71	2-6	3	II	11	IV	J								2-9		2-7	
DM54H72	2-6	3	II	11	IV	J								2-9		2-7	
DM74H72	2-6	3	II	11	IV	J								2-9		2-7	
DM54H73	2-6	3	II	11	IV	J								2-9		2-7	
DM74H73	2-6	3	II	11	IV	J								2-9		2-7	
DM54H74	2-6	3	II	11	IV	J								2-9		2-7	
DM74H74	2-6	3	II	11	IV	J								2-9		2-7	
DM54H76	2-6	5	II	12	IV	J								2-9		2-7	
DM74H76	2-6	5	II	12	IV	J								2-9		2-7	
DM54H78	2-6	3	II	11	IV	J								2-9		2-7	
DM74H78	2-6	3	II	11	IV	J								2-9		2-7	

*Order Numbers: use Device No. suffixed with package letter, i.e. DM54H00J.

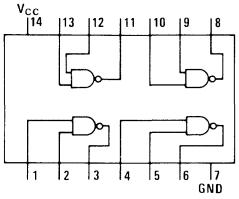
Series 54H/74H

Series DM54H/DM74H

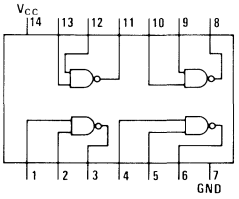
general description

The Series 54H/74H extends the breadth of the Series 54/74 Family by adding a product line which is approximately twice as fast as the basic series. The products are completely miscible within a system, and it is generally considered good engineering to optimize a design by utilizing the Series 54H/74H only where needed for higher speed.

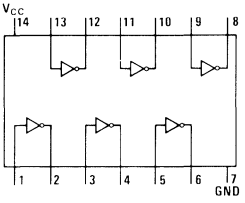
connection diagrams Dual-In-Line Package Only (Con't on Page 2-6)



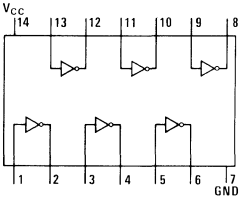
DM54H00/DM74H00
quad 2-input NAND gate



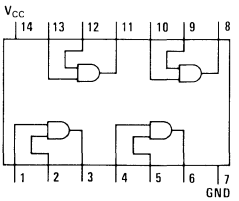
DM54H01/DM74H01
quad 2-input NAND gate
(open collector)



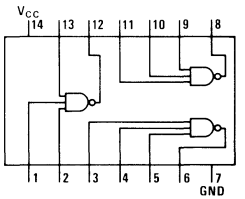
DM54H04/DM74H04
hex inverter



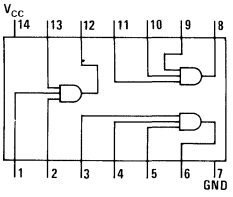
DM54H05/DM74H05
hex inverter
(open collector)



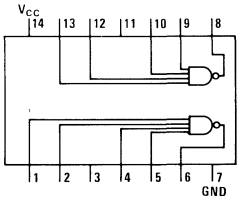
DM54H08/DM74H08
quad 2-input AND gate



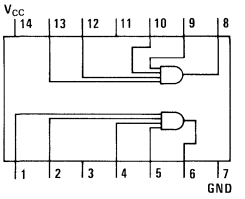
DM54H10/DM74H10
triple 3-input NAND gate



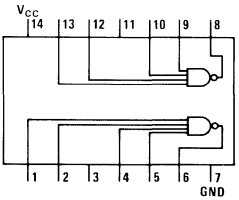
DM54H11/DM74H11
triple 3-input AND gate



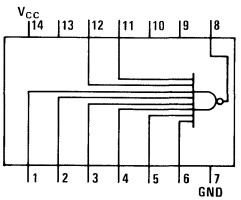
DM54H20/DM74H20
dual 4-input NAND gate



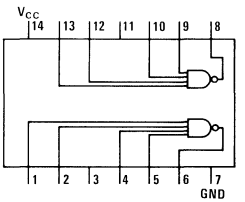
DM54H21/DM74H21
dual 4-input AND gate



DM54H22/DM74H22
dual 4-input NAND gate
(open collector)



DM54H30/DM74H30
8-input NAND gate



DM54H40/DM74H40
dual 4-input NAND buffer

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
Series 54H	−55°C to +125°C
Series 74H	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM54HXX	4.5	5.5	V
DM74HXX	4.75	5.25	V
Temperature			
DM54HXX	−55	125	°C
DM74HXX	0	70	°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage					
All Devices, Except DM54H40/DM74H40 and Open Collector Circuits	V_{CC} = Min, I_O = −500 μA, V_{IN} = 2.0V or 0.8V	2.4			V
DM54H40/DM74H40	V_{CC} = Min, I_O = −1.5 mA, V_{IN} = 2.0V or 0.8V	2.4			V
Logical "0" Output Voltage					
All Devices, Except DM54H40/DM74H40	V_{CC} = Min, I_O 20 mA, V_{IN} = 2.0V or 0.8V			0.4	V
DM54H40/DM74H40	V_{CC} = Min, I_O = 60 mA, V_{IN} = 2.0V or 0.8V			0.4	V
Logical "1" Output Current					
All Open Collector Circuits	V_{CC} = Min, V_{OUT} = 5.5V, V_{IN} = 2.0V or 0.8V			250	μA
Except DM54H60,DM54H62	@ −55°C			320	μA
DM74H60,DM74H62	@ 0°C			570	μA
DM54H61/DM74H61	V_{OUT} = 2.2V			50	μA
Output Short Circuit Current (Note 1)					
All Circuits Except DM54H40/DM74H40 and Open Collector Circuits	V_{CC} = Max, V_{OUT} = 0V	−40		−100	mA
DM54H40/DM74H40		−40		−125	mA
Supply Current	V_{CC} Max				
DM54H00/DM74H00					
Logical "0"			26	40	mA
Logical "1"			10	16.8	mA
DM54H01/DM74H01					
Logical "0"			26	40	mA
Logical "1"			6.8	10	mA
DM54H04/DM74H04					
Logical "0"			40	58	mA
Logical "1"			16	26	mA
DM54H05/DM74H05					
Logical "0"			40	58	mA
Logical "1"			16	26	mA
DM54H08/DM74H08					
Logical "0"			42	64	mA
Logical "1"			28	40	mA
DM54H10/DM74H10					
Logical "0"			19.5	30	mA
Logical "1"			7.5	12.6	mA
DM54H20/DM74H20					
Logical "0"			13	20	mA
Logical "1"			5.0	8.4	mA
DM54H21/DM74H21					
Logical "0"			20	32	mA
Logical "1"			12	20	mA
DM54H22/DM74H22					
Logical "0"			13	20	mA
Logical "1"			3.4	5.0	mA

Note 1: Not more than one output shorted at a time, duration of short-circuit test not to exceed 1 second, and all typical values are at V_{CC} = 5V, T_A = 25°C

electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DM54H30/DM74H30					
Logical "0"			6.5	10	mA
Logical "1"			2.5	4.2	mA
DM54H40/DM74H40					
Logical "0"			25	40	mA
Logical "1"			10.4	16	mA
DM54H50/DM74H50					
DM54H51/DM74H51					
Logical "0"			15.2	24	mA
Logical "1"			8.2	12.8	mA
DM54H52/DM74H52					
Logical "0"			15.2	24	mA
Logical "1"			20	31	mA
DM54H53/DM74H53					
DM54H54/DM74H54					
Logical "0"			9.4	14	mA
Logical "1"			7.1	11	mA
DM54H55/DM74H55					
Logical "0"			7.5	12	mA
Logical "1"			4.5	6.4	mA
DM54H60/DM74H60					
On Level Current			1.9	3.5	mA
Off Level Current			3.0	4.5	mA
DM54H61/DM74H61					
On Level Current			11	16	mA
Off Level Current			5.0	7.0	mA
DM54H62/DM74H62					
On Level Current			3.8	7.0	mA
Off Level Current			6.0	9.0	mA
DM54H71/DM74H71			19	30	mA
DM54H72/DM74H72			16	25	mA
DM54H73/DM74H73			32	50	mA
DM54H74/DM74H74			30	50	mA
DM54H76/DM74H76			32	50	mA
DM54H78/DM74H78			32	50	mA

switching characteristics $T_A = 25°C$, $V_{CC} = 5V$, N = 10, C = 25 pF, $R_L = 280\Omega$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DM54H00/DM74H00					
t_{pd0}			6.2	10	ns
t_{pd1}			5.9	10	ns
DM54H01/DM74H01					
t_{pd0}			7.5	12	ns
t_{pd1}			10	15	ns
DM54H04/DM74H04					
t_{pd0}			6.5	10	ns
t_{pd1}			6.0	10	ns
DM54H05/DM74H05					
t_{pd0}			7.5	12	ns
t_{pd1}			10	15	ns
DM54H08/DM74H08					
t_{pd0}			8.8	12	ns
t_{pd1}			7.6	12	ns

switching characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DM54H10/DM74H10					
t_{pd0}			6 3	10	ns
t_{pd1}			5 9	10	ns
DM54H11/DM74H11					
t_{pd0}			8.8	12	ns
t_{pd1}			7 6	12	ns
DM54H20/DM74H20					
t_{pd0}			7 0	10	ns
t_{pd1}			6 0	10	ns
DM54H21/DM74H21					
t_{pd0}			8 8	12	ns
t_{pd1}			7 6	12	ns
DM54H22/DM74H22					
t_{pd0}			7 5	12	ns
t_{pd1}			10	15	ns
DM54H30/DM74H30					
t_{pd0}			8 9	12	ns
t_{pd1}			6 8	10	ns
DM54H40/DM74H40					
t_{pd0}			6 5	12	ns
t_{pd1}			8 5	12	ns
DM54H50/DM74H50					
t_{pd0}			6 2	11	ns
t_{pd1}			6 8	11	ns
DM54H51/DM74H51					
t_{pd0}			6 2	11	ns
t_{pd1}			6 8	11	ns
DM54H52/DM74H52					
t_{pd0}			9 2	15	ns
t_{pd1}			10 6	15	ns
DM54H53/DM74H53					
t_{pd0}			6 2	11	ns
t_{pd1}			7 0	11	ns
DM54H54/DM74H54					
t_{pd0}			6 2	11	ns
t_{pd1}			7 0	11	ns
DM54H55/DM74H55					
t_{pd0}			6 5	11	ns
t_{pd1}			7 0	11	ns
DM54H60/DM74H60 (Thru Expandable Gates)					
t_{pd0}			7 4		ns
t_{pd1}			11 4		ns
DM54H61/DM74H61 (Thru Expandable Gates)					
t_{pd0}			9 8		ns
t_{pd1}			14 8		ns
DM54H62/DM74H62 (Thru Expandable Gates)					
t_{pd0}			7 4		ns
t_{pd1}			11.4		ns
DM54H71/DM74H71					
$t_{pd0(CLOCK)}$			22	27	ns
$t_{pd1(CLOCK)}$			14	21	ns
$t_{pd0(PRESET)}$			12	24	ns
$t_{pd1(PRESET)}$			6 0	13	ns

switching characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Clock Frequency		25	30		ns
DM54H72/DM74H72 DM54H73/DM74H73 DM54H76/DM74H76 DM54H78/DM74H78					
$t_{pd0(CLOCK)}$			22	27	ns
$t_{pd1(CLOCK)}$			14	21	ns
$t_{pd0(CLEAR,PRESET)}$			12	24	ns
$t_{pd1(CLEAR,PRESET)}$			6 0	13	ns
Maximum Clock Frequency		25	30		ns
DM54H74/DM74H74					
$t_{pd0(CLOCK)}$			13	20	ns
$t_{pd1(CLOCK)}$			8 5	15	ns
$t_{pd0(CLEAR,PRESET)}$				30	ns
$t_{pd1(CLEAR,PRESET)}$				20	ns
Maximum Clock Frequency		35	43		ns

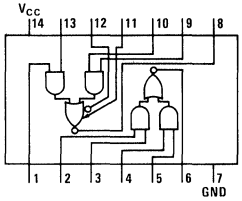
loading table

DEVICES	WEIGHTED LOADS
DM54H00/DM74H00	1
DM54H01/DM74H01	1
DM54H04/DM74H04	1
DM54H05/DM74H05	1
DM54H08/DM74H08	1
DM54H10/DM74H10	1
DM54H11/DM74H11	1
DM54H20/DM74H20	1
DM54H21/DM74H21	1
DM54H22/DM74H22	1
DM54H30/DM74H30	1
DM54H40/DM74H40	2
DM54H50/DM74H50	1
DM54H51/DM74H51	1
DM54H52/DM74H52	1
DM54H53/DM74H53	1
DM54H54/DM74H54	1
DM54H55/DM74H55	1
DM54H60/DM74H60	1
DM54H61/DM74H61	1
DM54H62/DM74H62	1
DM54H71/DM74H71	1
All Inputs Except	
Preset and Clock	1
Preset	3
Clock	2
DM54H72/DM74H72	
All Inputs Except	
Preset and Clear	1
Preset, Clear	2
DM54H73/DM74H73	
J, K, and Clock	1
Clear	2
DM54H74/DM74H74	
D	1
Preset and Clock	2
Clear	3
DM54H76/DM74H76	
J, K, and Clock	1
Preset and Clear	2
DM54H78/DM74H78	
J and K	1
Preset and Clock	2
Clear	4

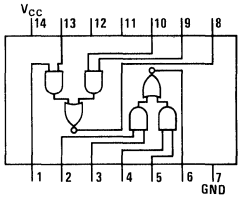
1 Load = 50 μA @ 2 4V Logical "1" Input Current
= 2 mA @ 0 4V Logical "0" Input Current

(All inputs are guaranteed 1 mA @ 5 5V for Logical "1" breakdown test)

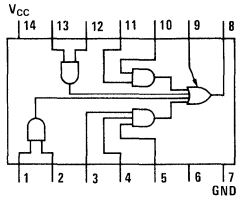
connection diagrams (con't)



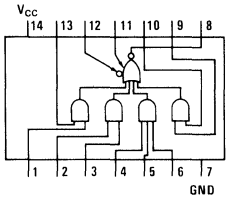
DM54H50/DM74H50
expandable dual 2-wide
2-input AND-OR-INVERT gate



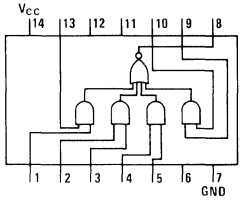
DM54H51/DM74H51
dual 2-wide 2-input
AND-OR-INVERT gate



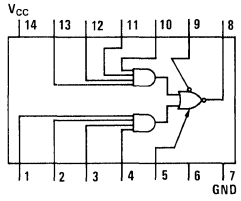
DM54H52/DM74H52
expandable 2-2-2-3-input
AND-OR gate



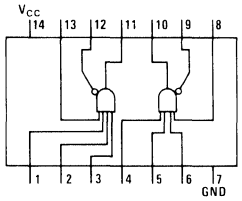
DM54H53/DM74H53
expandable 2-2-2-3-input
AND-OR-INVERT gate



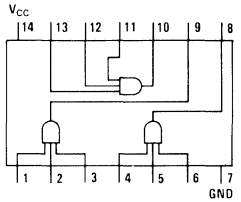
DM54H54/DM74H54
4-wide 2-input
AND-OR-INVERT gate



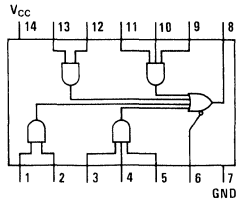
DM54H55/DM74H55
expandable 2-wide 4-input
AND-OR-INVERT gate



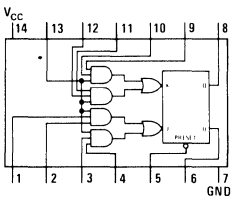
DM54H60/DM74H60
dual 4-input expander



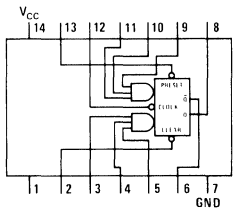
DM54H61/DM74H61
triple 3-input expander



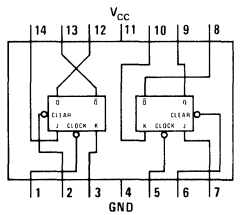
DM54H62/DM74H62
3-2-2-3-input expander



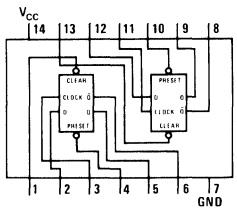
DM54H71/DM74H71
J-K flip flop with AND-OR inputs



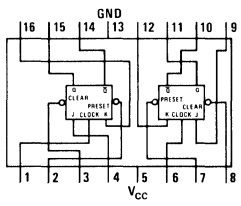
DM54H72/DM74H72
J-K master-slave flip flop



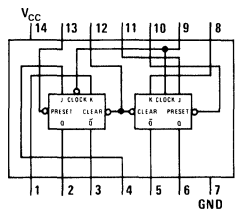
DM54H73/DM74H73
dual J-K flip flop with
separate clocks



DM54H74/DM74H74
dual D edge-triggered flip flop

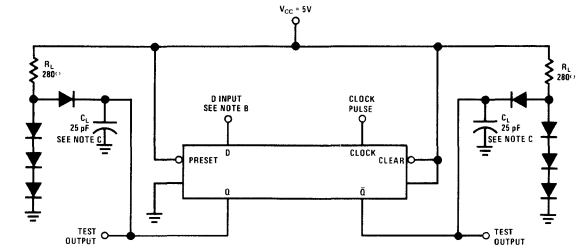


DM54H76/DM74H76
dual J-K master-slave flip flop



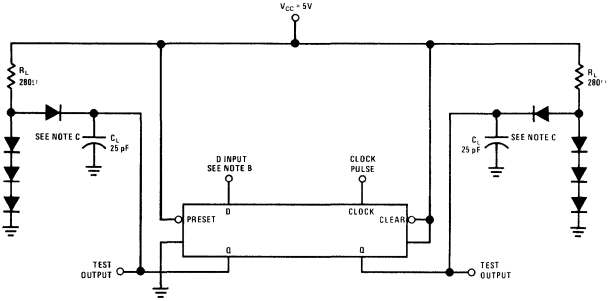
DM54H78/DM74H78
dual J-K flip flop with preset
and clear inputs

ac test circuits



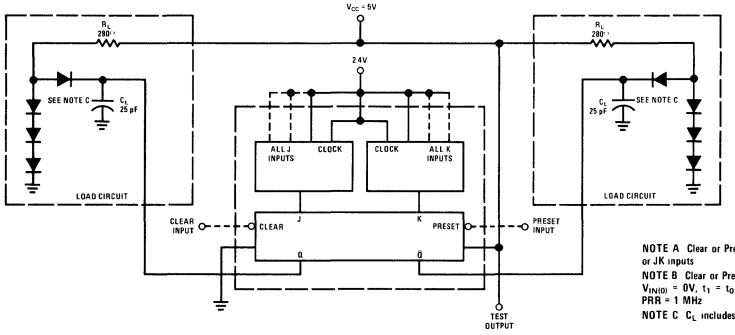
NOTE A Clock input pulse has the following characteristics $t_{W(CLOCK)}$ = 20 ns, PRR = 1 MHz
NOTE B D input (pulse A) has the following characteristics t_{SETUP} = 10 ns, t_W = 60 ns, PRR is 50% of clock PRR D input (pulse B) has the following characteristics t_{HOLD} = 0 ns, t_W = 60 ns, PRR is 50% of clock PRR
NOTE C C_L includes probe and jig capacitance

Switching Characteristics, Clock and Synchronous Inputs (High Level Data)



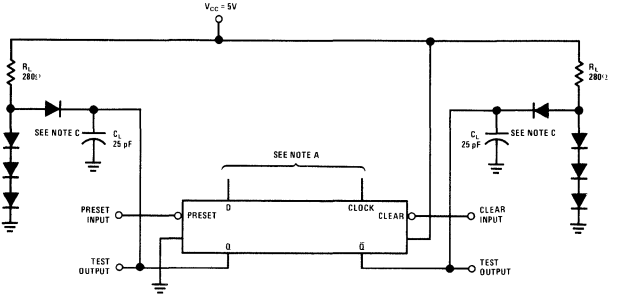
NOTE A Clock input pulse has the following characteristics t_W = 20 ns, PRR = 1 MHz
NOTE B D input (pulse A) has the following characteristics t_{SETUP} = 15 ns, t_W = 60 ns, PRR = 1 MHz and PRR is 50% of the clock PRR D input (pulse B) has the following characteristics t_{HOLD} = 0 ns, t_W = 60 ns, and PRR is 50% of clock PRR
NOTE C C_L includes probe and jig capacitance

Switching Characteristics, Clock and Synchronous Inputs (Low-Level Data)



NOTE A Clear or Preset inputs are dominate regardless of clock or JK inputs
NOTE B Clear or Preset input pulse characteristics $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 7 ns $t_{P(CLEAR)}$ = $t_{P(PRESET)}$ = 16 ns, PRR = 1 MHz
NOTE C C_L includes jig capacitance

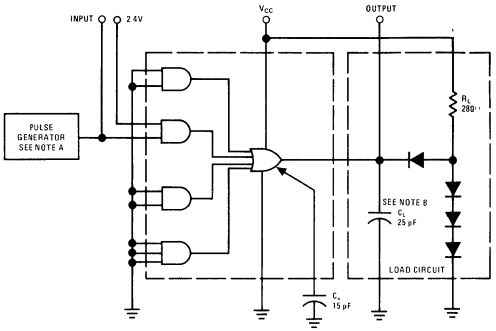
Flip Flop Preset/Clear Propagation Delay Times



NOTE A Clear and Preset input dominate clock or D inputs
NOTE B Clear or Preset inputsline characteristics $t_{W(CLEAR)}$ = $t_{W(PRESET)}$ = 25 ns, PRR = 1 MHz
NOTE C C_L includes probe and jig capacitance

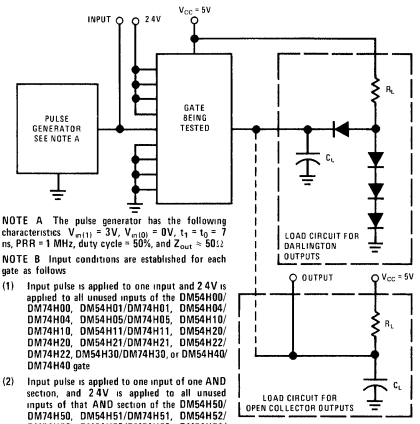
Asynchronous Inputs Switching Characteristics

ac test circuits (con't)



NOTE A $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_0 = t_1 = 7 ns, duty cycle = 50%, PRR = 1 MHz, Z_{OUT} ≈ 50Ω
NOTE B C_L includes jig capacitance
NOTE C C_x includes jig capacitance

DM54H52/DM74H52



NOTE A The pulse generator has the following characteristics $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, t_1 = t_0 = 7 ns, PRR = 1 MHz, duty cycle = 50%, and Z_{out} ≈ 50Ω

NOTE B Input conditions are established for each gate as follows

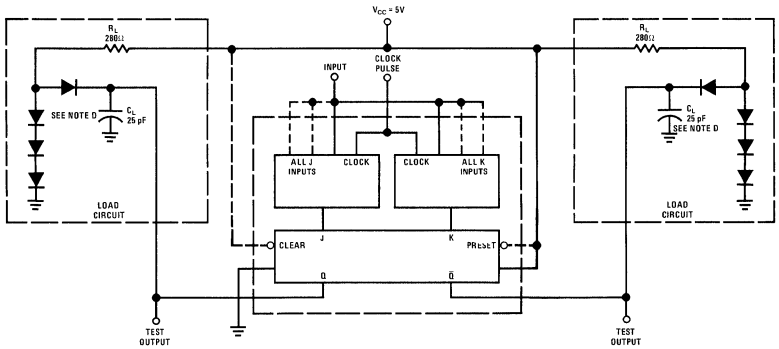
(1) Input pulse is applied to one input and 2.4V is applied to all unused inputs of the DM54H00/DM74H00, DM54H01/DM74H01, DM54H04/DM74H04, DM54H05/DM74H05, DM54H10/DM74H10, DM54H11/DM74H11, DM54H20/DM74H20, DM54H21/DM74H21, DM54H22/DM74H22, DM54H30/DM74H30, or DM54H40/DM74H40 gate

(2) Input pulse is applied to one input of one AND section, and 2.4V is applied to all unused inputs of that AND section of the DM54H50/DM74H50, DM54H51/DM74H51, DM54H52/DM74H52, DM54H53/DM74H53, DM54H54/DM74H54, or DM54H55/DM74H55 gate All inputs of all unused AND sections are grounded

NOTE C All gates are inverting except the DM54H11/DM74H11, DM54H21/DM74H21, and DM54H52/DM74H52 only

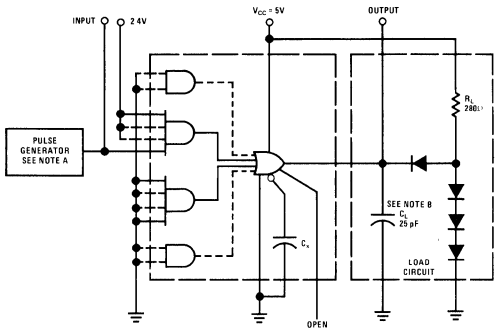
NOTE D C_L includes probe and jig capacitance

DM54H52/DM74H52 Loading For Gates



NOTE A When testing t_{pd0} and t_{pd1} (all types), the clock input pulse characteristics are $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 7 ns, $t_{p(CLOCK)}$ = 20 ns, and PRR = 1 MHz
NOTE B All J and K inputs are at 2.4V
NOTE C When testing f_{CLOCK} the clock input characteristics are $V_{IN(0)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 3 ns, $t_{p(CLOCK)}$ = 10 ns, PRR = 40 MHz All J and K inputs are at 2.4V
NOTE D C_L includes probe and jig capacitance

Flip Flop Propagation Delay Times



NOTE A $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_0 = t_1 = 7 ns, duty cycle = 50%, PRR = 1 MHz
NOTE B C_L includes probe and jig capacitance
NOTE C C_x includes jig capacitance

DM54H50, DM54H53, DM54H55

truth tables

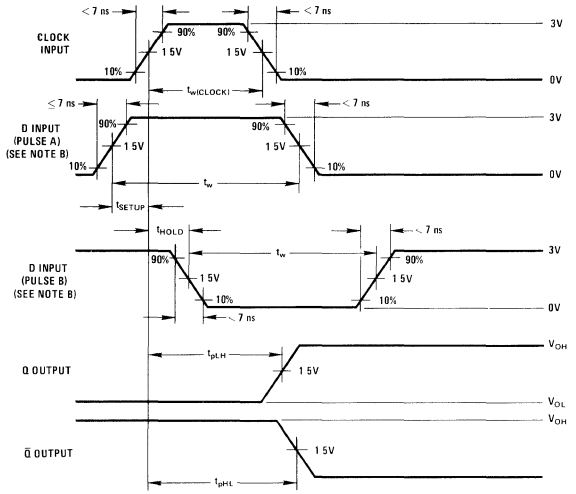
t_n		t_{n+1}
J	K	Q
0	0	Q_N
0	1	0
1	0	1
1	1	$\bar{Q}_N$

all J-K flip flops

t_n	t_{n+1}	
D	Q	$\bar{Q}$
0	0	1
1	1	0

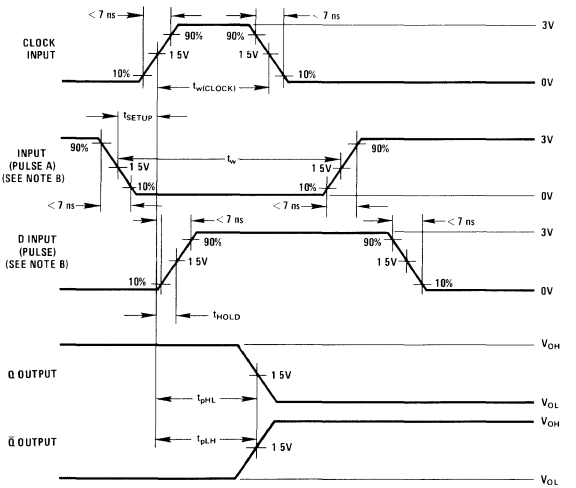
DM74H74 only

switching time waveforms



NOTE A Clock input pulse has the following characteristics $t_{w(CLOCK)}$ = 20 ns, PRR = 1 MHz
NOTE B D input (pulse A) has the following characteristics t_{SETUP} = 10 ns, t_w = 60 ns, PRR is 50% of clock PRR D input (pulse B) has the following characteristics t_{HOLD} = 0 ns t_w = 60 ns, PRR is 50% of clock PRR
NOTE C C_L includes probe and jig capacitance

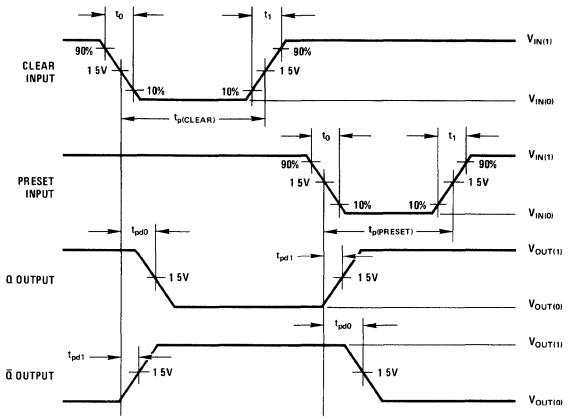
Switching Characteristics, Clock and Synchronous Inputs
(High Level Data)



NOTE A Clock input pulse has the following characteristics t_w = 20 ns, PRR = 1 MHz
NOTE B D input (pulse A) has the following characteristics t_{SETUP} = 15 ns, t_w = 60 ns, PRR = 1 MHz and PRR is 50% of the clock PRR D input (pulse B) has the following characteristics t_{HOLD} = 0 ns, t_w = 60 ns, and PRR is 50% of clock PRR
NOTE C C_L includes probe and jig capacitance

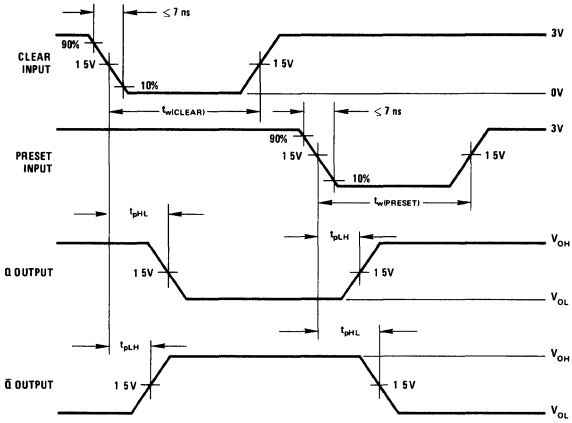
Switching Characteristics, Clock and Synchronous Inputs
(Low Level Data)

switching time waveforms (con't)



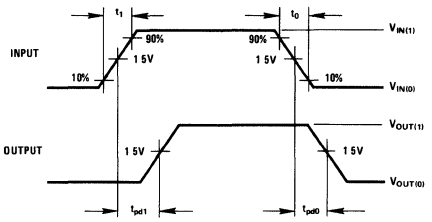
NOTE A Clear or Preset inputs are dominate regardless of clock or JK inputs
NOTE B Clear or Preset input pulse characteristics $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 7 ns, $t_{p(CLEAR)}$ = $t_{p(PRESET)}$ = 16 ns, PRR = 1 MHz
NOTE C C_L includes jig capacitance

Flip Flop Preset/Clear Propagation Delay Times



NOTE A Clear and Preset input dominate clock or D inputs
NOTE B Clear or Preset inpulse characteristics $t_{w(CLEAR)}$ = $t_{w(PRESET)}$ = 25 ns, PRR = 1 MHz
NOTE C C_L includes probe and jig capacitance

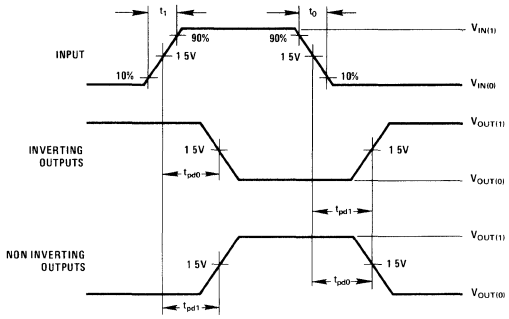
Asynchronous Inputs Switching Characteristics



NOTE A $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_0 = t_1 = 7 ns, duty cycle = 50%, PRR = 1 MHz, Z_{OUT} ≈ 50Ω
NOTE B C_L includes jig capacitance
NOTE C C_x includes jig capacitance

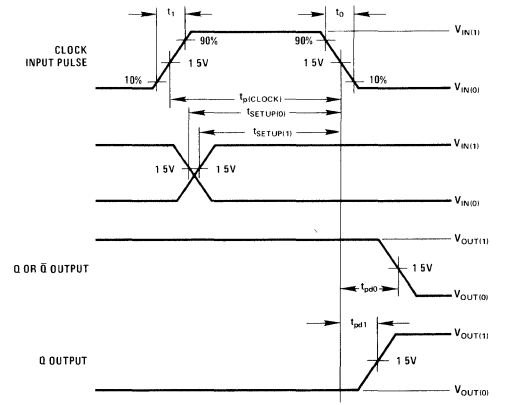
DM54H52/DM74H52

switching time waveforms (con't)



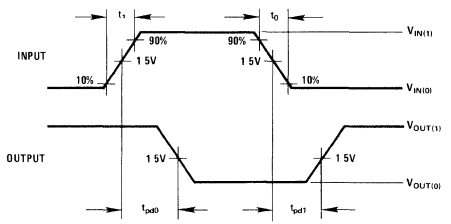
NOTE A $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 7 ns, PRR = 1 MHz, duty cycle = 50%, $Z_{OUT} \approx 50\Omega$
NOTE B C_L includes probe and jig capacitance, R_L = 280Ω on all gates except DM54H40 where R_L = 93Ω
NOTE C C_L = 25 pF on all devices
NOTE D C_S = 1 3 pF typical for expanders

DM54H52/DM74H52 Propagation Delays



NOTE A When testing t_{pd0} and t_{pd1} (all types), the clock input pulse characteristics are $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 7 ns, $t_{pICLOCK)}$ = 20 ns, and PRR = 1 MHz
NOTE B All J and K inputs are at 2 4V
NOTE C When testing f_{CLOCK} the clock input characteristics are $V_{IN(0)}$ = 3V, $V_{IN(0)}$ = 0V, t_1 = t_0 = 3 ns, $t_{pICLOCK)}$ = 10 ns, PRR = 40 MHz All J and K inputs are at 2 4V
NOTE D C_L includes probe and jig capacitance

Flip Flop Propagation Delay Times



NOTE A $V_{IN(1)}$ = 3V, $V_{IN(0)}$ = 0V, t_0 = t_1 = 7 ns, duty cycle = 50%, PRR = 1 MHz
NOTE B C_L includes probe and jig capacitance
NOTE C C_S includes jig capacitance

DM54H50, DM54H53, DM54H55

Series 54L/74L

REFERENCE

The following table references all Physical Dimension Drawings for the devices in this section For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function Packages (pages I thru VI) are in the back of the catalog

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
Devices	Pg	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
		Fig	Pg.	Fig.	Pg	Type	Fig.	Pg.	Type	Fig	Pg	Type		Fig	Pg	Fig	Pg
DM54L00	3-3	3	II	11	IV	J	15	IV	F								
DM74L00	3 3	3	II	11	IV	J	15	IV	F								
DM54L01	3 3						15	IV	F								
DM74L01	3-3						15	IV	F								
DM54L02	3 3	3	II	11	IV	J	15	IV	F								
DM74L02	3-3	3	II	11	IV	J	15	IV	F								
DM54L03	3 3	3	II	11	IV	J											
DM74L03	3 3	3	II	11	IV	J											
DM54L04	3 3	3	II	11	IV	J	15	IV	F								
DM74L04	3-3	3	II	11	IV	J	15	IV	F								
DM54L10	3 3	3	II	11	IV	J	15	IV	F								
DM74L10	3-3	3	II	11	IV	J	15	IV	F								
DM54L20	3 3	3	II	11	IV	J	15	IV	F								
DM74L20	3 3	3	II	11	IV	J	15	IV	F								
DM54L30	3-3	3	II	11	IV	J	15	IV	F								
DM74L30	3-3	3	II	11	IV	J	15	IV	F								
DM54L42A	3-31	5	II	9	III	J	16	V	F								
DM74L42A	3-31	5	II	9	III	J	16	V	F								
DM54L51	3-7	3	II	11	IV	J	15	IV	F								
DM74L51	3-7	3	II	11	IV	J	15	IV	F								
DM54L54	3-7	3	II	11	IV	J	15	IV	F								
DM74L54	3 7	3	II	11	IV	J	15	IV	F								
DM54L55	3-7	3	II	11	IV	J	15	IV	F								
DM74L55	3-7	3	II	11	IV	J	15	IV	F								
DM54L71	3-10	3	II	11	IV	J	15	IV	F								
DM74L71	3-10	3	II	11	IV	J	15	IV	F								
DM54L72	3 10	3	II	11	IV	J	15	IV	F								
DM74L72	3-10	3	II	11	IV	J	15	IV	F								
DM54L73	3-10	3	II	11	IV	J	15	IV	F								
DM74L73	3-10	3	II	11	IV	J	15	IV	F								
DM54L74	3-10	3	II	11	IV	J	15	IV	F								
DM74L74	3-10	3	II	11	IV	J	15	IV	F								
DM54L78	3-10	3	II	11	IV	J	15	IV	F								
DM74L78	3-10	3	II	11	IV	J	15	IV	F								
DM54L85	3-34	5	II	9	III	J	16	V	F								
DM74L85	3-34	5	II	9	III	J	16	V	F								
DM54L86	3-22	3	II	11	IV	J	15	IV	F								
DM74L86	3-22	3	II	11	IV	J	15	IV	F								
DM54L90	3-37	3	II	11	IV	J	15	IV	F								
DM74L90	3-37	3	II	11	IV	J	15	IV	F								
DM54L91	3-40	3	II	11	IV	J	15	IV	F								
DM74L91	3-40	3	II	11	IV	J	15	IV	F								
DM54L93	3-42	3	II	11	IV	J	15	IV	F								
DM74L93	3-42	3	II	11	IV	J	15	IV	F								
DM54L95	3-25	3	II	11	IV	J	15	IV	F								
DM74L95	3-25	3	II	11	IV	J	15	IV	F								
DM54L98	3-45	5	II	12	IV	J	16	V	F								
DM74L98	3-45	5	II	12	IV	J	16	V	F								
DM54L154A	3-47	7	III	10	III	D	17	V	F								
DM74L154A	3-47	7	III	10	III	D	17	V	F								
DM54L165A	3-49	5	II	12	IV	J	16	V	F								
DM74L165A	3-49	5	II	12	IV	J	16	V	F								
DM54L192	3-52	5	II	12	IV	J	16	V	F								
DM74L192	3-52	5	II	12	IV	J	16	V	F								

*Order Numbers. use Device No suffixed with package letter, i.e DM54L00F

DATA SHEETS		PACKAGES											WAVE-FORMS		TEST CIRCUITS	
Devices	Pg	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)						
		Fig	Pg	Fig	Pg	Type	Fig	Pg	Type	Fig	Pg	Type	Fig.	Pg.	Fig	Pg.
DM54L193	3-52	5	II	12	IV	J	16	V	F							
DM74L193	3-52	5	II	12	IV	J	16	V	F							
DM71L22	3-59	5	II	12	IV	J	16	V	F							
DM81L22	3-59	5	II	12	IV	J	16	V	F							
DM71L23	3-59	5	II	12	IV	J	16	V	F							
DM81L23	3-59	5	II	12	IV	J	16	V	F							
DM75L11	3-63	5	II	9	III	D	16	V	F							
DM85L11	3-63	5	II	9	III	D	16	V	F							
DM75L12	3-66	5	II	12	IV	J	16	V	F							
DM85L12	3-66	5	II	12	IV	J	16	V	F							
DM75L51	3-69	5	II	12	IV	J	16	V	F							
DM85L51	3-69	5	II	12	IV	J	16	V	F							
DM75L52	3-74	5	II	12	IV	J	16	V	F							
DM85L52	3-74	5	II	12	IV	J	16	V	F							
DM75L54	3-74	5	II	12	IV	J	16	V	F							
DM85L54	3-74	5	II	12	IV	J	16	V	F							
DM76L70	3-25	3	II	11	IV	J	15	IV	F							
DM86L70	3-25	3	II	11	IV	J	15	IV	F							
DM76L75	3-80	5	II	12	IV	J	16	V	F							
DM86L75	3-80	5	II	12	IV	J	16	V	F							
DM76L76	3-80	5	II	12	IV	J	16	V	F							
DM86L76	3-80	5	II	12	IV	J	16	V	F							
DM76L93	3-42	3	II	11	IV	J	15	IV	F							
DM86L93	3-42	3	II	11	IV	J	15	IV	F							
DM78L12	3-82	3	II	11	IV	J	15	IV	F							
DM88L12	3-82	3	II	11	IV	J	15	IV	F							

Series 54L/74L

LOW POWER TRANSISTOR-TRANSISTOR LOGIC

general description

The Series 54L/74L family is designed for applications requiring very low power dissipation. Typically a system can be built with a factor-of-ten power saving over the conventional TTL integrated circuits, such as Series 54/74. Gates typically draw 0.2 mA from a 5 volt supply thus dissipating 1 mW. Flip flops pull about 1.0 mA and therefore dissipate about 5 mW. Speed however is not proportionately sacrificed. Flip flops can typically be clocked at 11 MHz. Gate delays are typically 25 ns.

The Series is manufactured with TTL circuitry and employs low impedance Darlington outputs which maintain output voltage waveform integrity when capacitively loaded. The Darlington outputs also allow greater guaranteed logical "1" fan out (20) in case it is desirable to connect unused inputs to used inputs.

National's Low Power Series is also guaranteed to drive two standard TTL unit loads from 0°C to 70°C.

features

- Low power dissipation—typically 1 mW/gate, 5 mW/flip flop.
- Relatively high speed
  - Typical gate propagation delay time of 25 ns.
  - Typical flip flop toggle frequency at 11 MHz.
  - Typical MSI shift register toggle frequency at 12 to 14 MHz.
- High dc noise margin—typically 1 volt at $T_A = 25°C$.
- Low impedance Darlington outputs provide low ac noise susceptibility.
- Fan Out
  - 10 Series 54L loads in logical "0" state
  - 20 Series 54L loads in logical "1" state
  - 2 Series 74 loads (74L only)
  - 1 Series 54 load and 2 Series 54L loads
  - 1 Series 54H load.
- TTL and DTL compatible.

Device types specified in the data sheet include:

NAND, NOR GATES

DM54L00/DM74L00 (SN54L00/SN74L00)
Quad 2-Input NAND Gate
DM54L01/DM74L01 (SN54L01/SN74L01)
Quad 2-Input NAND Gate, Open Collector
DM54L02/DM74L02 (SN54L02/SN74L02) Quad 2-Input NOR Gate
DM54L03/DM74L03 (SN54L03/SN74L03) Quad 2-Input NAND Gate, Open Collector
DM54L04/DM74L04 (SN54L04/SN74L04)
Hex Inverter
DM54L10/DM74L10 (SN54L10/SN74L10)
Triple 3-Input NAND Gate
DM54L20/DM74L20 (SN54L20/SN74L20)
Dual 4-Input NAND Gate
DM54L30/DM74L30 (SN54L30/SN74L30)
Eight-Input NAND Gate

AND-OR-INVERT GATES

DM54L51/DM74L51 (SN54L51/SN74L51)
Dual 2-wide AND-OR-INVERT Gate
DM54L54/DM74L54 (SN54L54/SN74L54)
Four-wide 3-2-2-3-Input AND-OR-INVERT Gate

DM54L55/DM74L55 (SN54L55/SN74L55)
Two-wide 4-Input AND-OR-INVERT Gate

table of contents

general description (cont.)

FLIP FLOPS

DM54L71/DM74L71 (SN54L71/SN74L71)
R-S Flip Flop

These R-S flip-flops use master-slave construction so the slave is stable when the clock is held either high or low. Clock disable at data inputs results in hold times of 0 ns, and also clock-controlled data entry.

DM54L72/DM74L72 (SN54L72/SN74L72)
J-K Flip Flop

These J-K flip-flops use master-slave construction so the slave is stable when the clock is held either high or low. Clock disable at data inputs results in hold times of 0 ns, and also clock-controlled data entry.

DM54L73/DM74L73 (SN54L73/SN74L73)
Dual J-K Flip Flop

Operation is the same as the DM54L72/DM74L72 except that only single J and K inputs are available.

DM54L74/DM74L74 (SN54L74/SN74L74)
Dual D Flip Flop

These monolithic, low-power, dual, edge-triggered flip flops utilize TTL circuitry to perform D-type flip flop logic. Each flip flop has individual clear and preset inputs, and complementary Q and $\overline{Q}$ outputs.

Information at D-input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect on the state of the output.

DM54L78/DM74L78 (SN54L78/SN74L78)
Dual J-K Flip Flop

Operation is the same as the DM54L73/DM74L73 except that common CLEAR and CLOCK inputs feed both flip flops. This frees two pins which are used for separate PRESET inputs.

EXCLUSIVE-OR GATES

DM54L86/DM74L86 (SN54L86/SN74L86)
Quad EXCLUSIVE-OR Gate

The DM54L86/DM74L86 (SN54L86/SN74L86) quad EXCLUSIVE-OR circuit performs as a half-adder: the output is a logical "1" only when the inputs are at different logical states.

SHIFT REGISTERS

DM54L95/DM74L95 (SN54L95/SN74L95)
Four-bit Parallel-in Parallel-out Shift Register

Parallel or serial operation is selected by the MODE input, which also enables one of the two clock inputs. Parallel information must be clocked-in allowing shift-left operation by connecting each output to the left-adjacent parallel input.

DM76L70/DM86L70 Eight-Bit Serial-In Parallel-Out Shift Register

The DM76L70/DM86L70 utilizes Series 54L/74L compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical "0", asynchronously sets all flip flops to the logical "0" state.

Because the flip flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical "1" levels on SA and SB enter logical "1's" into the shift register. Clocking occurs on the positive-going edge of the clock pulse.

absolute maximum ratings

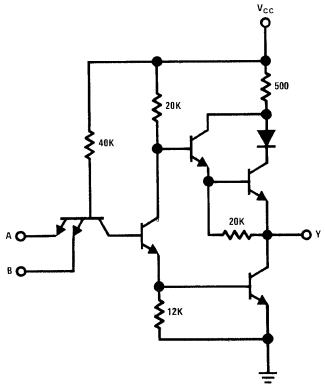
Power Supply Voltage	8.0V
Input Voltage	5.5V
Fan Out Logic "1"	20
Logic "0"	10
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

guaranteed operating conditions

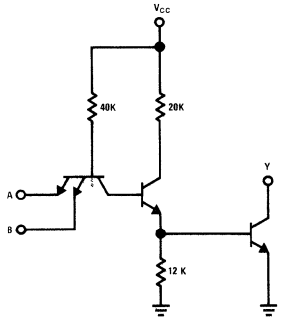
Power Supply Voltage	
DM54LXX, DM7XLXX	4.5V to 5.5V
DM74LXX, DM8XLXX	4.75V to 5.25V
Operating Temperature	
DM54LXX, DM7XLXX	−55°C to 125°C
DM74LXX, DM8XLXX	0°C to 70°C

DM54L00/DM74L00, DM54L01/DM74L01, DM54L02/
DM74L02, DM54L03/DM74L03, DM54L04/DM74L04,
DM54L10/DM74L10, DM54L20/DM74L20,DM54L30/
DM74L30

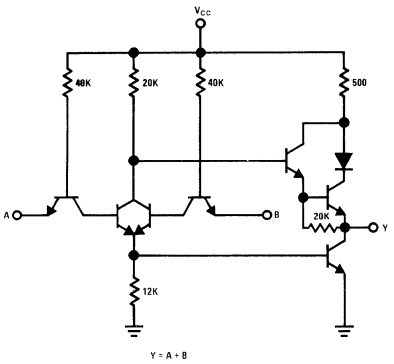
schematic diagrams



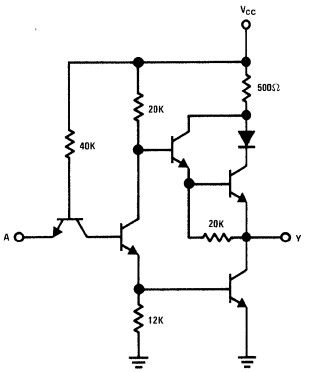
DM54L00/DM74L00, DM54L10/DM74L10
DM54L20/DM74L20, DM54L30/DM74L30



DM54L01/DM74L01
DM54L03/DM74L03

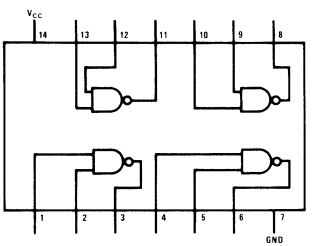


DM54L02/DM74L02

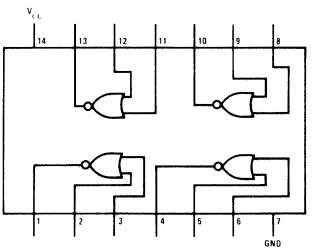


DM54L04/DM74L04

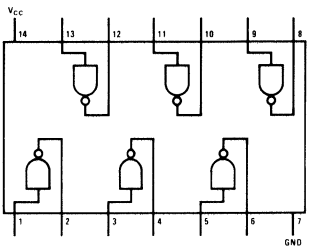
dual-in-line package connection diagrams



DM54L00/DM74L00
DM54L03/DM74L03



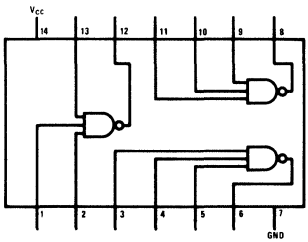
DM54L02/DM74L02



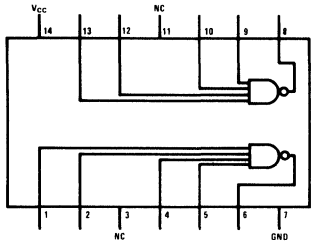
DM54L04/DM74L04

SUMMARY

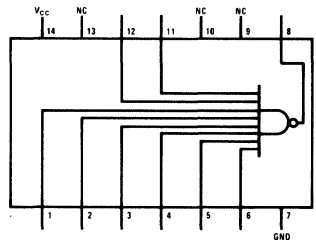
dual-in-line package connection diagrams (cont.)



DM54L10/DM74L10



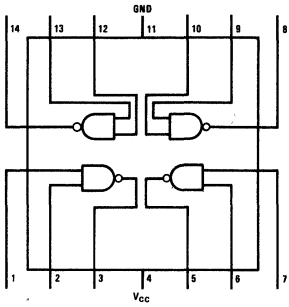
DM54L20/DM74L20



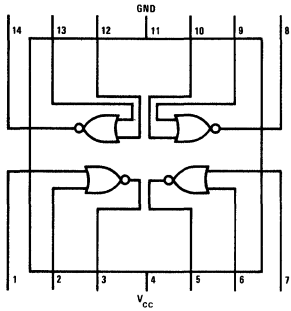
DM54L30/DM74L30

NAND, NOR GATES

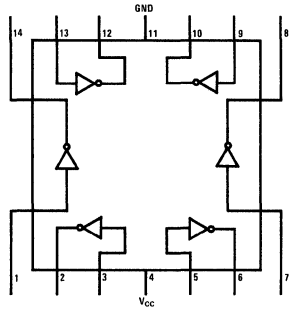
flat package connection diagrams



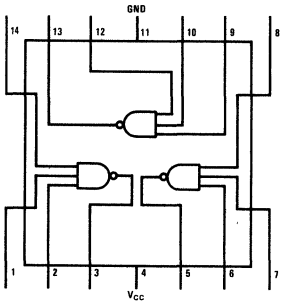
DM54L00/DM74L00
DM54L01/DM74L01



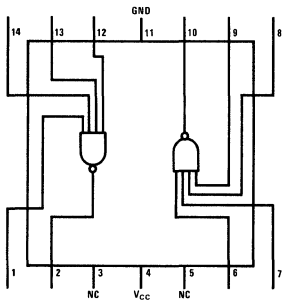
DM54L02/DM74L02



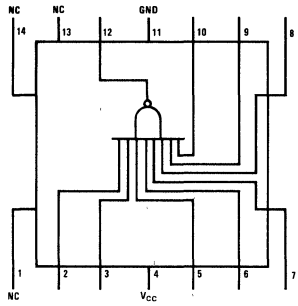
DM54L04/DM74L04



DM54L10/DM74L10



DM54L20/DM74L20



DM54L30/DM74L30

dc electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	TEST FIGURE	MIN	TYP (NOTE 1)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN	1	2	1 3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN	2		1 3	0 7	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except DM54L01/DM74L01, DM54L03/DM74L03)	V_{CC} = MIN, I_{OUT} = -200 μA, V_{IN} = 0 7V, Other Inputs = 2V	2	2 4	2 8		V
$I_{OUT(1)}$	Output Current DM54L01/DM74L03	V_{IN} = 0 3V, V_{CC} = MIN, V_{OUT} = 5 5V	6A			50	μA
	DM54L01/DM54L03	V_{IN} = 0 6V, V_{CC} = MIN, V_{OUT} = 5 5V	6A			200	μA
	DM74L01/DM74L03	V_{IN} = 0 7V, V_{CC} = MIN, V_{OUT} = 5 5V	6A			200	μA
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA, V_{IN} (All Inputs) = 2V	1		0 15	0 3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3 2 mA, V_{IN} (All Inputs) = 2V	1			0 4	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = MAX, V_{IN} = 2 4V, Other Inputs = 0V	4		<1	10	μA
		V_{CC} = MAX, V_{IN} = 5 5V	4			100	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = MAX, V_{IN} = 0 3V, Other Inputs = 4 5V	3		-120	-180	μA
I_{OS}	Logical "1" Output Short Circuit Current (Except DM54L01/DM74L01, DM54L03/DM74L03)	V_{CC} = MAX, V_{IN} = 0V, V_{OUT} = 0V	5	-3	-8	-15	mA
$I_{CC(1)}$	Logical "1" State Power Supply Current (Per Gate) (Except DM54L02/DM74L02) (Note 2)	V_{CC} = MAX, V_{IN} (All Inputs) = 0V, I_{OUT} = 0	6		120	200	μA
$I_{CC(0)}$	Logical "0" State Power Supply Current (Per Gate) (Except DM54L02/DM74L02) (Note 3)	V_{CC} = MAX, V_{IN} (All Inputs) = 5V, I_{OUT} = 0	6		330	510	μA

Note 1: All typicals at T_A = 25°C
Note 2. For the DM54L02/DM74L02, $I_{CC(1)}$ = 400μA Max
Note 3: For the DM54L02/DM74L02, $I_{CC(0)}$ = 600μA Max

ac electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	TEST FIGURE	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical '0' (Except DM54L01/DM74L01 DM54L03/DM74L03)	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	7		30	60	ns
	DM54L30/DM74L30				60	100	ns
t_{pd1}	Propagation Delay to a Logical "1" (Except DM54L01/DM74L01 DM54L03/DM74L03)	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	7		25	60	ns
t_{pd0}	Propagation Delay to a Logical "0" DM54L01/DM74L01 DM54L03/DM74L03	V_{CC} = 5V, R_L = 4k, C_L = 15 pF, T_A = 25°C	(7)		25	60	ns
t_{pd1}	Propagation Delay to a Logical "1" DM54L01/DM74L01 DM54L03/DM74L03	V_{CC} = 5V, R_L = 4k, C_L = 15 pF, T_A = 25°C	(7)		40	90	ns

NAND, NOR GATES

DM54L03/DM74L03 open collector application data

The DM54L03/DM74L03 is an open-collector LP TTL gate, that when supplied with a proper load resistor R_L, can be paralleled with other similar LP TTL gates to perform the wire-AND function, and simultaneously, will drive from one to six loads When only one gate is wire-AND connected, this gate can be used to drive eight LP TTL gates. To meet these conditions, an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined so that sufficient load currents (to LP TTL Gate Loads) and Off Currents (To wire-AND connections) will be available during a logical "1" level at output. Also, a minimum resistor value must be determined which will ensure that currents from the loads will not cause the output voltage to rise above the logical "0" level.

To meet both conditions (logical "0" and logical "1"), the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}} \quad (1)$$

Where;

V_{RL} = Voltage Drop (volts)
I_{RL} = Current (amps)

The following equations will be useful in determining the value of R_L (Max) and R_L (Min):

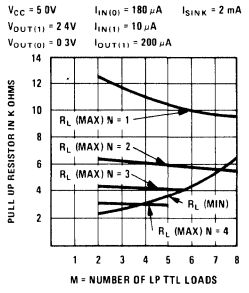
$$R_L\ (\text{Max}) = \frac{V_{CC} - V_{out}(1)}{N \cdot I_{out}(1) + M \cdot I_{in}(1)} \quad (2)$$

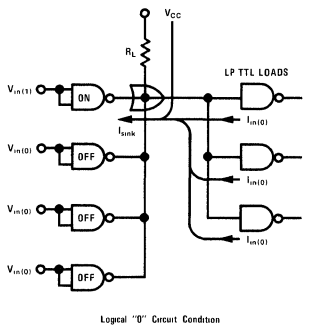
$$R_L\ (\text{Min}) = \frac{V_{CC} - V_{out}(0)}{I_{out}(0) - M\ I_{in}(0)} \quad (3)$$

N = number of gates wire-AND connected
M = number of LP TTL loads

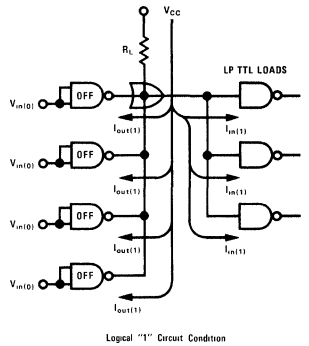
DM54L03/DM74L03 open collector application data

The maximum loads connected (M) under any wire-OR configuration (N) is shown respectively by the intersection of the R_L (Min) and R_L (Max) curves For instance, for N = 2 and M = 5 the maximum loads connected is six



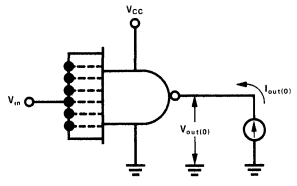


Logical "0" Circuit Condition



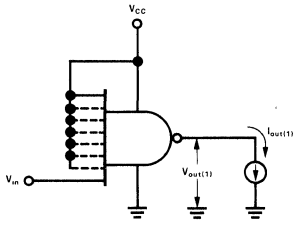
Logical "1" Circuit Condition

dc test circuits



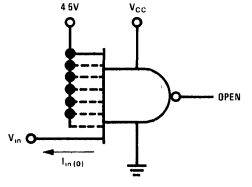
Note All inputs are tested simultaneously

Figure 1



Note Each input is tested separately

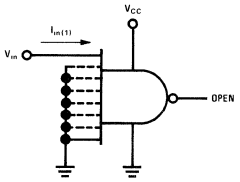
Figure 2



Note Each input is tested separately

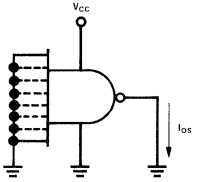
Figure 3

dc test circuits (cont.)



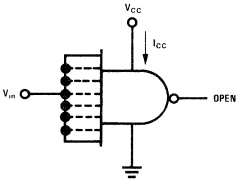
Note Each input is tested separately

Figure 4



Note Each gate is tested separately

Figure 5



Notes 1 Logical "0" and Logical "1" conditions are tested
2 All gates are tested simultaneously

Figure 6

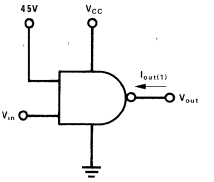
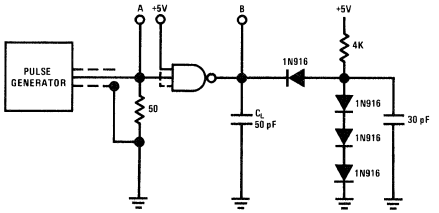
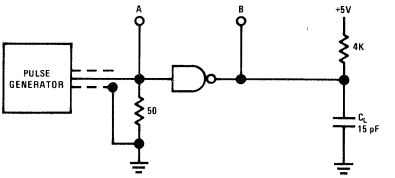


Figure 6a

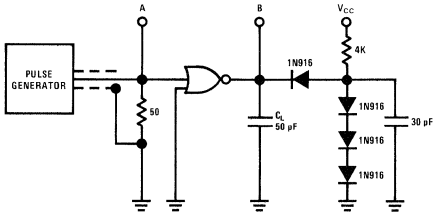
ac test circuits and waveforms



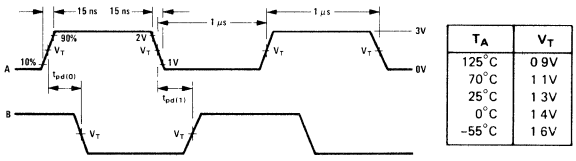
DM54L00/DM74L00, DM54L04/DM74L04
DM54L10/DM74L10, DM54L20/DM74L20
DM54L30/DM74L30



DM54L01/DM74L01
DM54L03/DM74L03



DM54L02/DM74L02



T_A	V_T
125°C	0 9V
70°C	1 1V
25°C	1 3V
0°C	1 4V
−55°C	1 6V

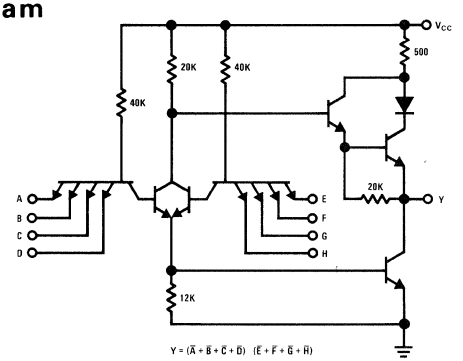
Note C_L includes probe and jig capacitance

Figure 7

AND-OR-INVERT GATES

DM54L51/DM74L51, DM54L54/ DM74L54, DM54L55/DM74L55

schematic diagram

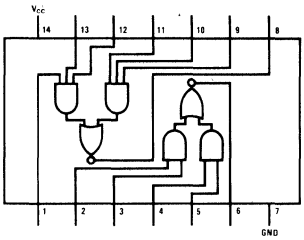


$Y = (\overline{A} + \overline{B} + \overline{C} + \overline{D})\ (\overline{E} + \overline{F} + \overline{G} + \overline{H})$

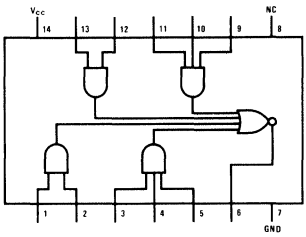
DM54L51/DM74L51, DM54L54/DM74L54, DM54L55/DM74L55
(DM54L55/DM74L55 Shown)

AND-OR-INVERT GATES

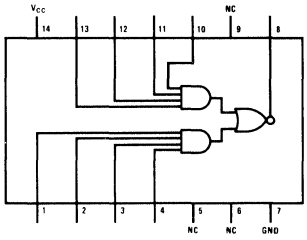
dual-in-line package connection diagrams



DM54L51/DM74L51

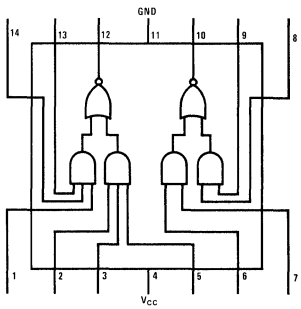


DM54L54/DM74L54

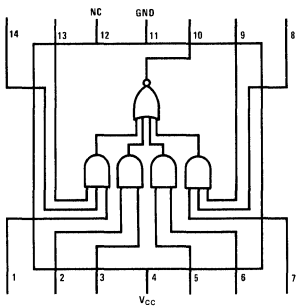


DM54L55/DM74L55

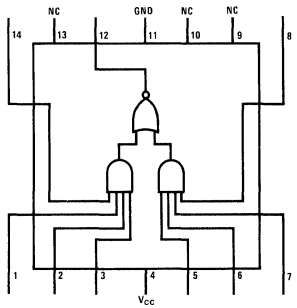
flat package connection diagrams



DM54L51/DM74L51



DM54L54/DM74L54



DM54L55/DM74L55

dc electrical characteristics

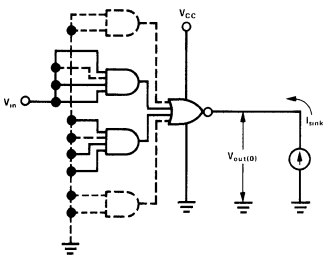
SYMBOL	PARAMETER	CONDITIONS (Note 1)	TEST FIGURE	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Logical 1 Input Voltage	V_{CC} = MIN	8	2	1 3		V
$V_{IN(0)}$	Logical '0 Input Voltage	V_{CC} = MIN	9		1 3	0 7	V
$V_{OUT(1)}$	Logical 1 Output Voltage	V_{CC} = MIN I_{OUT} = -200 μA V_{IN} = 0 7V (Each Input Tested Separately)	9	2 4	2 8		
$V_{OUT(0)}$	Logical '0 Output Voltage	V_{CC} = MIN I_{OUT} = 2 mA, V_{IN} (All Inputs On One Section) = 2 0V, Other Inputs - 0V	8		0 15	0 3	V
$V_{OUT(0)}$	Logical 0 Output Voltage (Series 74L Only)	V_{CC} MIN, I_{OUT} 3 2 mA	1			0 4	V
$I_{IN(1)}$	Logical 1 Input Current	V_{CC} = MAX, V_{IN} = 2 4V, Other Inputs = 0V	11		<1	10	μA
		V_{CC} = MAX V_{IN} = 5 5V, Other Inputs = 0V	11			100	μA
$I_{IN(0)}$	Logical '0 Input Current	V_{CC} = MAX V_{IN} = 0 3V, Other Inputs = 4 5V	10		-120	-180	μA
I_{OS}	Logical 1 Output Short Circuit Current	V_{CC} = MAX, V_{IN} (All Inputs) = 0V, V_{OUT} = 0V	12	-3	-8	-15	mA
$I_{CC(1)}$	Logical 1 ' State Power Supply Current (Per Gate)	V_{CC} = MAX, DM54L51/DM74L51	13		240	400	μA
		V_{IN} (All Inputs) = 0V, DM54L54/DM74L54	13		480	800	μA
		I_{OUT} = 0 DM54L55/DM74L55	13		240	400	μA
$I_{CC(0)}$	Logical "0 State Power Supply Current (Per Gate)	V_{CC} = MAX, DM54L51/DM74L51	13		390	650	μA
		V_{IN} (All Inputs) = 5V, DM54L54/DM74L54	13		600	990	μA
		I_{OUT} = 0 DM54L55/DM74L55	13		390	650	μA

Note 1: Each input "AND" section tested separately
Note 2: All typicals at $T_A = 25^\circ C$

ac electrical characteristics

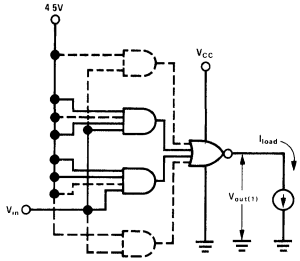
SYMBOL	PARAMETER	TEST CONDITIONS	TEST FIGURE	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay to a Logical 1	V_{CC} 5V C_L 50 pF T_A 25 C	14		40	90	ns
t_{pd0}	Propagation Delay to a Logical '0	V_{CC} 5V C_L - 50 pF T_A 25 C	14		30	60	ns

dc test circuits



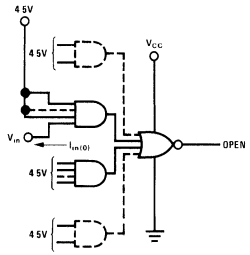
Note Each AND section is tested separately

Figure 8



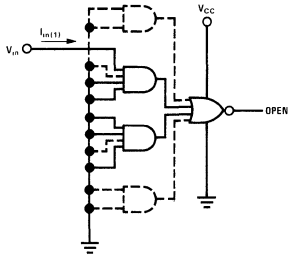
Note Each set of inputs is tested separately

Figure 9



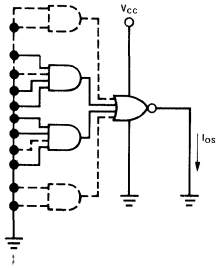
Note Each input is tested separately

Figure 10



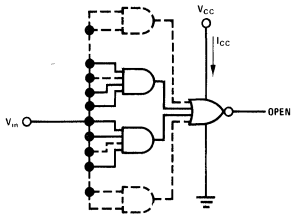
Note Each input is tested separately

Figure 11



Note Each gate is tested separately

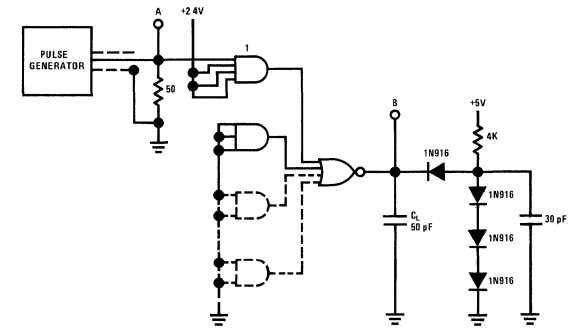
Figure 12

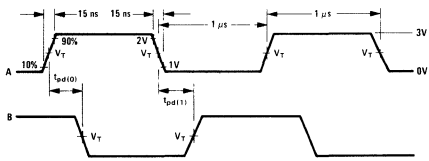


Note All gates are tested simultaneously

Figure 13

ac test circuits and waveforms (cont.)





T_A	V_T
125°C	0 9V
70°C	1 1V
25°C	1 3V
0°C	1 4V
-55°C	1 6V

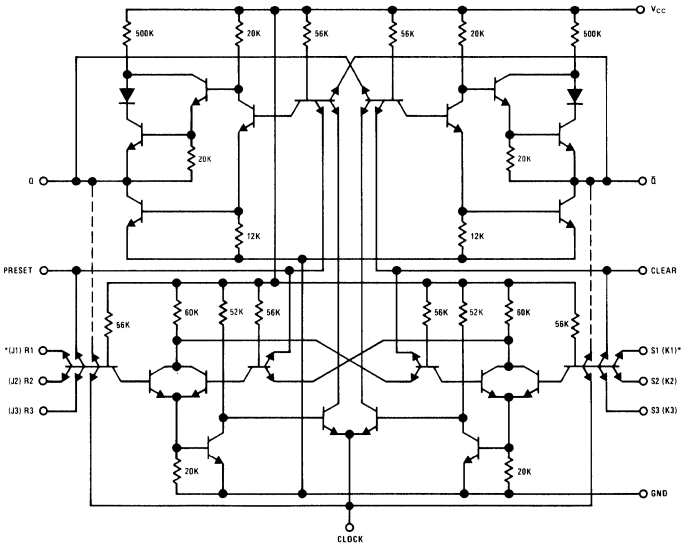
Note C_L includes probe and jig capacitance

Figure 14

FLIP FLOPS

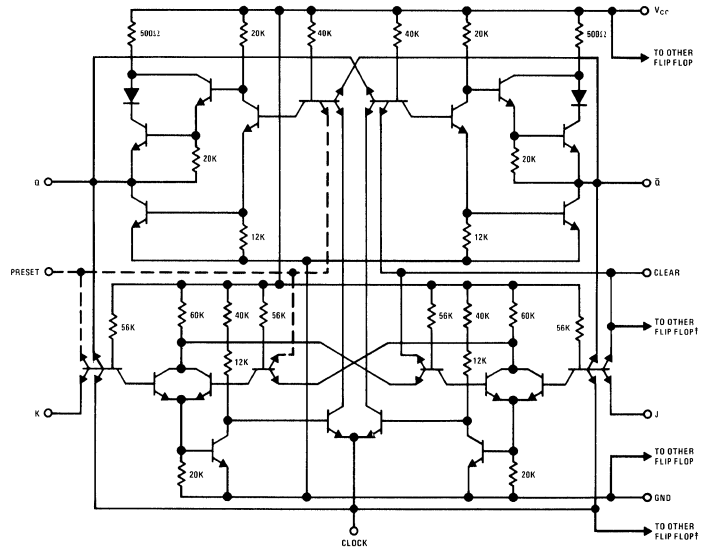
DM54L71/DM74L71, DM54L72/DM74L72, DM54L73/
DM74L73, DM54L74/DM74L74, DM54L78/DM74L78

schematic diagrams



Note Dotted connections refer to
DM54L72/DM74L72 only

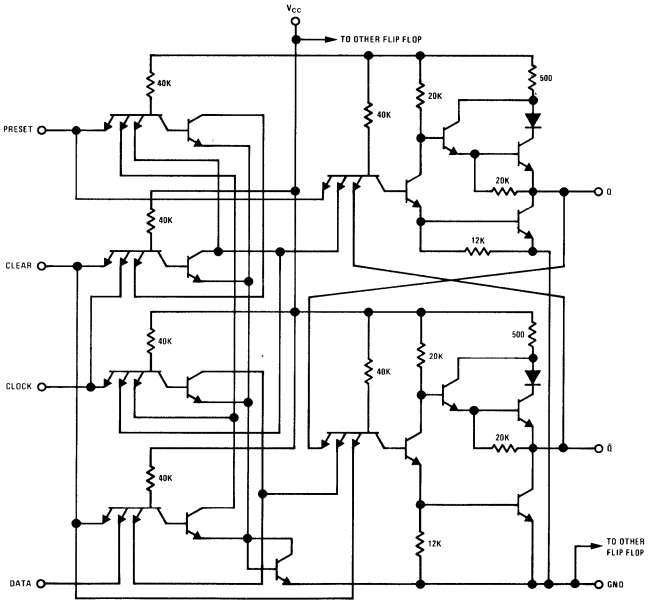
DM54L71/DM74L71, DM54L72/DM74L72



Note Dotted connections refer to
DM54L78/DM74L78 only

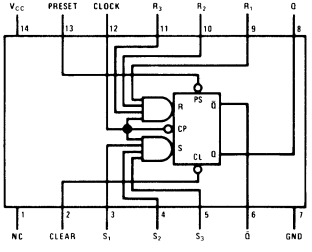
DM54L73/DM74L73, DM54L78/DM74L78

schematic diagrams (cont.)

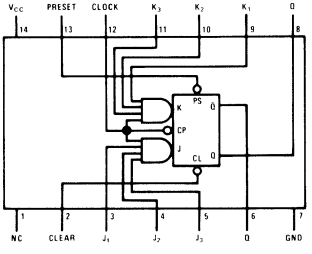


DM54L74/DM74L74
(Shows one flip flop only)

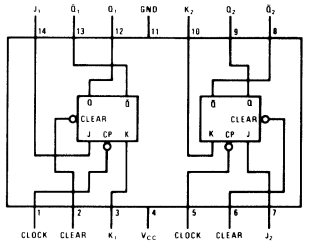
dual-in-line package connection diagrams



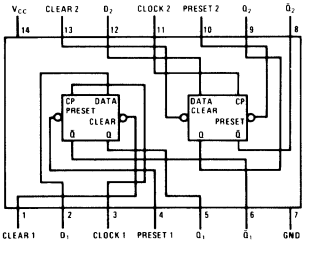
DM54L71/DM74L71



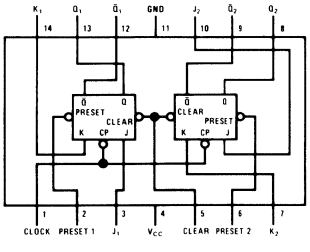
DM54L72/DM74L72



DM54L73/DM74L73



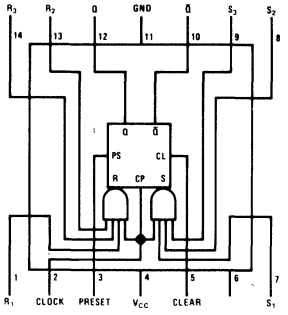
DM54L74/DM74L74



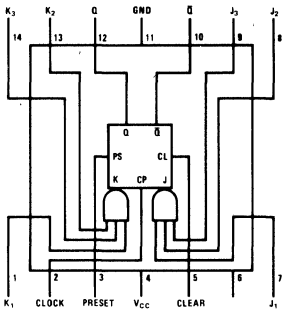
DM54L78/DM74L78

FLIP FLOPS

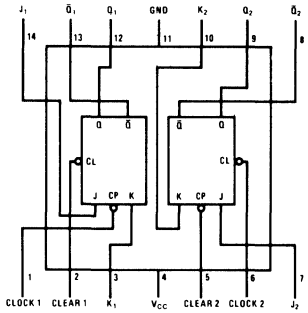
flat package connection diagrams



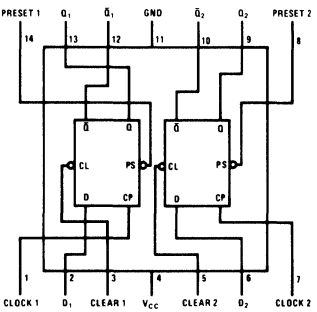
DM54L71/DM74L71



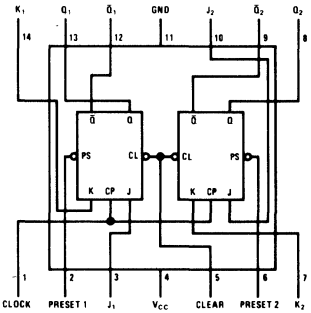
DM54L72/DM74L72



DM54L73/DM74L73



DM54L74/DM74L74



DM54L78/DM74L78

dc electrical characteristics

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE DM54L71/ DM74L71	DM54L72/ DM74L72	DM54L73/ DM74L73	DM54L74/ DM74L74	DM54L78/ DM74L78	MIN	TYP (Note 1)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN		15, 16	20, 21	25, 26	31, 32	25, 26	2	1 3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN		15, 16	20, 21	25, 26	31, 32	25, 26		1 3	0 7	V
$V_{IN(0)CP}$	Logical "0" Input Voltage at Clock	V_{CC} = MIN		15, 16	20, 21	25, 26	31, 32	25, 26		1 2	0 6	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN, I_{OUT} = −200 μA		15	20	25	31	25	2 4	2 8		V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA		16	21	26	32	26		0 15	0 3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3 2 mA, V_{IN} (All Inputs) = 2V		16	21	26	32	26			0 4	V
$I_{IN(1)RSJKD}$	Logical "1" Input Current at R,S,J,K, or Data	V_{CC} = MAX, V_{IN} = 2 4V V_{CC} = MAX, V_{IN} = 5 5V		18 18	23 23	28 28	34 34	28 28		<1	10 100	μA μA
$I_{IN(1)P}$	Logical "1" Input Current at Preset	V_{CC} = MAX, V_{IN} = 2 4V V_{CC} = MAX, V_{IN} = 5 5V		18 18	23 23	– –	34 –	28 –		<2	20 200	μA μA
$I_{IN(1)C}$	Logical "1" Input Current at Clear	V_{CC} = MAX, V_{IN} = 2 4V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73	18	23	28	–	–		<2	20	μA
			DM54L74/DM74L74	–	–	–	34	–		<3	30	μA
			DM54L78/DM74L78	–	–	–	–	28		<4	40	μA
		V_{CC} = MAX, V_{IN} = 5 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73	18	23	28	–	–			200	μA
			DM54L74/DM74L74	–	–	–	34	–			300	μA
			DM54L78/DM74L78	–	–	–	–	28			400	μA
$I_{IN(1)CP}$	Logical "1" Input Current at Clock	V_{CC} = MAX, V_{IN} = 2 4V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73	18	23	28	–	–	0	−50	−200	μA
			DM54L74/DM74L74	–	–	–	34	–		<2	20	μA
			DM54L78/DM74L78	–	–	–	-	28	0	−100	−400	μA
		V_{CC} = MAX, V_{IN} = 5 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L74/DM74L74	18	23	28	34	–			200	μA
			DM54L78/DM74L78	–	–	–	-	28			400	μA
$I_{IN(0)RSJKD}$	Logical "0" Input Current at R,S,J,K or Data	V_{CC} = MAX, V_{IN} = 0 3V		17	22	28	33	27		−120	−180	μA
$I_{IN(0)P}$	Logical "0" Input Current at Preset	V_{CC} = MAX, V_{IN} = 0 3V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L78/DM74L78	17	22	–	–	27		−240	−360	μA
			DM54L74/DM74L74	–	–	–	33	–		−120	−180	μA
$I_{IN(0)C}$	Logical "0" Input Current at Clear	V_{CC} = MAX, V_{IN} = 0 3V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L74/DM74L74	17	22	27	33	–		−240	−360	μA
			DM54L78/DM74L78	–	–	–	–	27		−480	−720	μA
$I_{IN(0)CP}$	Logical "0" Input Current at Clock	V_{CC} = MAX, V_{IN} = 0 3V	L71, 72, 73 74 L78	–	–	–	–	–			360 720	μA μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX		19	24	29	35	30	−3	-9	−15	mA
I_{CC}	Power Supply Current (per F/F)	V_{CC} = MAX, V_{IN} CLOCK = 0V		18	23	28	34	28			1 44	mA

Note 1: All typicals at $T_A = 25°C$, $V_{CC} = 5V$

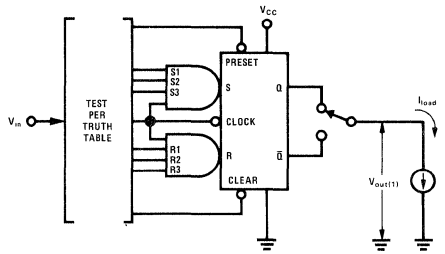
FLIP FLOPS

switching characteristics

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE DM54L71/ DM74L71	DM54L72/ DM74L72	DM54L73/ DM74L73	DM54L74/ DM74L74	DM54L78/ DM74L78	MIN	TYP (Note 1)	MAX	UNITS
F_{CLOCK}	Maximum Clock Frequency	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V All F/F		36	36	36	38	36	6	11		MHz
$t_{pd0\ CLOCK}$	Propagation Delay to a Logical "0" From Clock	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36	–	36	10	60	150	ns
			DM54L74/DM74L74	–	–	–	38	–	25	75	120	ns
$t_{pd1\ CLOCK}$	Propagation Delay to a Logical "1" From Clock		DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36		36	10	30	75	ns
			DM54L74/DM74L74	–	–	–	38	–	15	40	90	ns
$t_{pd1\ CLEAR\ PRESET}$	Propagation Delay to a Logical "1" From Clear		DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	37	37	37	–	37		30	75	ns
			DM54L74/DM74L74	–	–	–	37	–		25	60	ns
$t_{pd0\ CLEAR\ PRESET}$	Propagation Delay to a Logical "0" From Preset	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V $V_{IN\ CLOCK}$ = 2.4 or 0V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	37	37	37	–	37		70	150	ns
			DM54L74/DM74L74	–	–	–	37	–		60	120	ns
t_{pW}	Minimum Clock Pulse Width	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36	–	36	100	65		ns
			DM54L74/DM74L74	–		–	38	–	75	40		ns
$t_{pW\ CLEAR\ PRESET}$	Minimum Clear or Preset Pulse Width	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	37	37	37	–	37	100	60		ns
			DM54L74/DM74L74	–	–	–	37	–	75	40		ns
t_{SETUP}	Data Setup Time	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71	36	–	–	-	–	100			ns
			DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	-	36	36	–	36	$\geq t_{pW\ CLOCK}$			ns
			DM54L74/DM74L74	–	–	-	38	–	30	15		ns
t_{HOLD}	Data Hold Time	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36	–	36	0			ns
		Logical "1"	DM54L74/DM74L74	–	–	–	38	–		10	15	ns
		Logical "0"	DM54L74/DM74L74	–	–	–	38	–		5	10	ns

Note 1: Switching parameter limits, switching parameter typicals, and electrical parameter typicals are given for V_{CC} = 5V at T_A = 25°C only

dc test circuits



Note Each input is tested separately

TEST TABLE

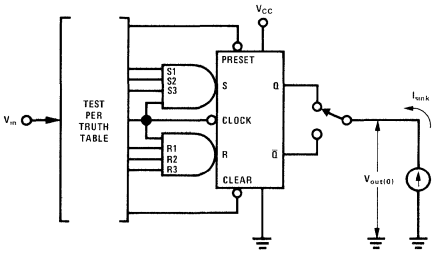
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	INDETERMINATE	

Positive logic. $R = R_1 \cdot R_2 \cdot R_3$
$S = S_1 \cdot S_2 \cdot S_3$

Figure 15

Note: H = high level (steady state), L = low level (steady state), X = irrelevant.
⎍ = high level pulse; data inputs should be held constant while clock is high, data is transferred to output on the falling edge of the pulse
↑ = transition from low to high level, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established
TOGGLE. Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

dc test circuits (cont.)



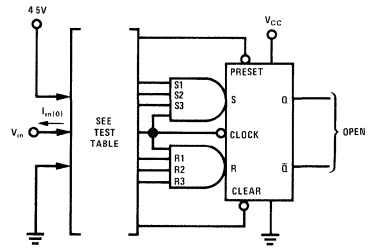
Note Each input is tested separately

TEST TABLE **

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\bar{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	INDETERMINATE	

Positive logic $R = R_1 \cdot R_2 \cdot R_3$
$S = S_1 \cdot S_2 \cdot S_3$

Figure 16

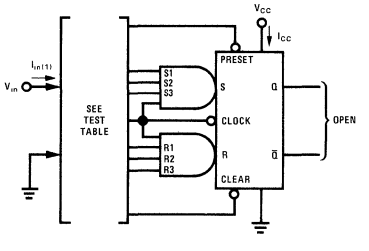


Note Each input is tested separately

TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
RI	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

Figure 17



Note Each output is tested separately

TEST TABLE

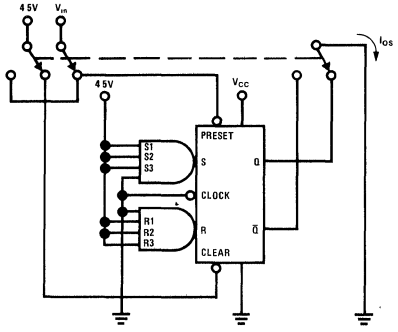
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

Figure 18

**See page 3-14 for notes.

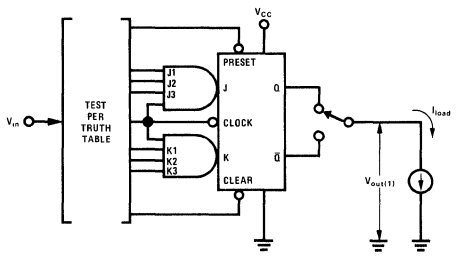
FLIP FLOPS

dc test circuits (cont.)



Note Each output is tested separately

Figure 19



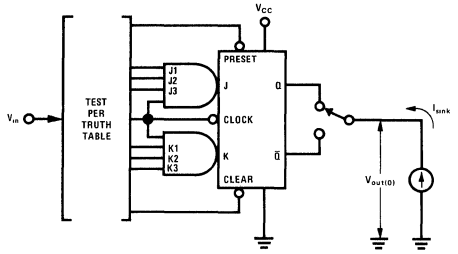
Note Each input is tested separately

TEST TABLE **

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

Positive logic. $J = J_1 \cdot J_2 \cdot J_3$; $K_1 \cdot K_2 \cdot K_3$

Figure 20



Note Each output is tested separately

TEST TABLE **

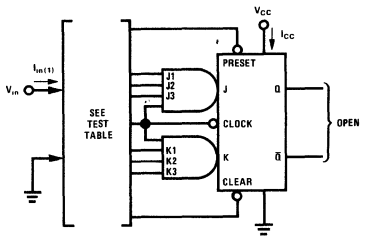
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

Positive logic $J = J_1 \cdot J_2 \cdot J_3$, $K_1 \cdot K_2 \cdot K_3$

Figure 21

**See page 3-14 for notes

dc test circuits (cont.)

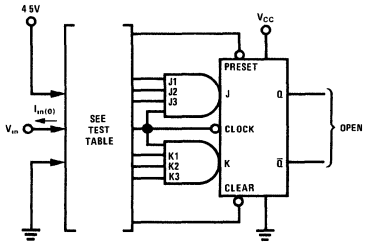


Note Each input is tested separately

TEST TABLE

Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

Figure 22

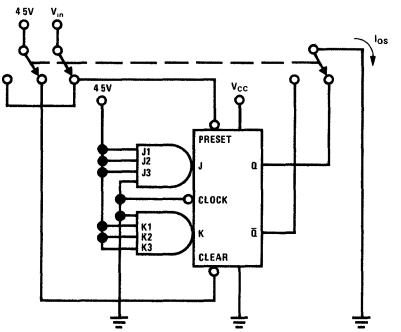


Note Each output is tested separately

TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5V	Apply 4.5V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

Figure 23

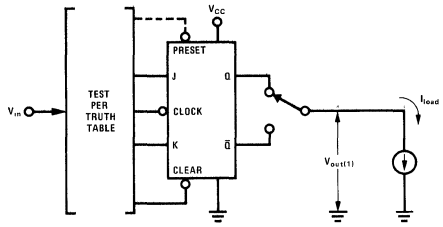


Note Each output is tested separately

Figure 24

FLIP FLOPS

dc test circuits (cont.)



Notes 1 Each flip flop is tested separately
2 Each output is tested separately
3 Preset is applicable for DM54L78/DM74L78 circuits only

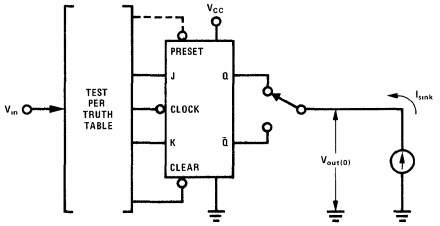
TEST TABLE **

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

'73, 'H73, 'L73 TEST TABLE **

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

Figure 25



Notes. 1 Each flip flop is tested separately
2 Each output is tested separately
3 Preset is applicable for DM54L78/DM74L78 circuits only

TEST TABLE **

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

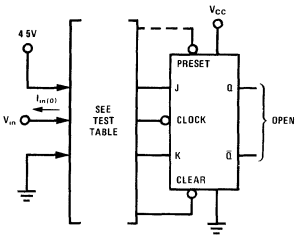
'73, 'H73, 'L73 TEST TABLE **

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

Figure 26

**See page 3-14 for notes

dc test circuits (cont.)

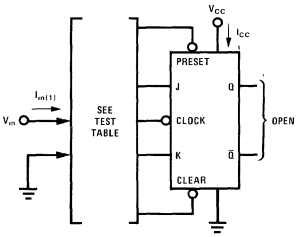


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

Notes 1 Each flip flop is tested separately
2 Apply momentary ground, then 4.5V
3 After application of momentary ground, Q and $\overline{Q}$ are left floating
4 Preset is applicable for DM54L78/DM74L78 circuits only

Figure 27



TEST TABLE

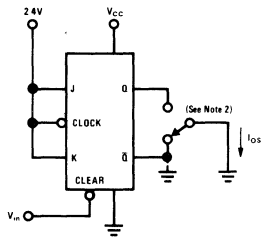
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 3)	Clock and Preset	Clear

Notes 1 Preset is applicable for DM54L78/DM74L78 circuits only
2 I_{CC} is measured (simultaneously for both flip flops) for the following conditions
a J = K = Clock = Clear = Gnd for DM54L78/DM74L78, Preset = 4.5V
b For DM54L73/DM74L73 J = Clear = 4.5V, K = Gnd, and apply momentary 4.5V, then Gnd, to Clock
For DM54L78/DM74L78 J = K = Clock = Preset = Gnd and Clear = 4.5V

Average per flip flop = $\frac{I_{CC}\ total}{2}$

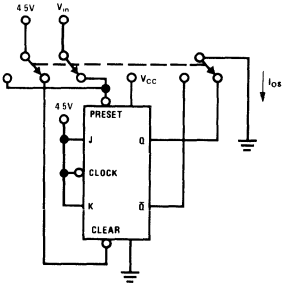
3 Each flip flop is tested separately for $I_{in(1)}$

Figure 28



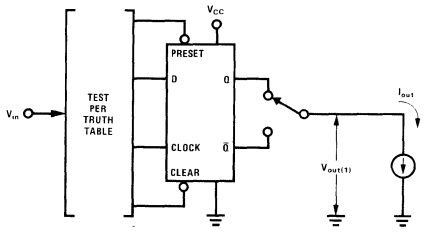
Notes 1 Each flip flop is tested separately
2 Test circuit shows setup for testing $\overline{Q}$. When testing Q, open all inputs and ground $\overline{Q}$

Figure 29



Note Each flip flop is tested separately

Figure 30



Notes 1 Each flip flop is tested separately
2 Each output is tested separately

TEST TABLE **

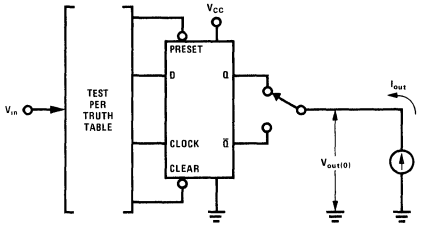
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

**See page 3-14 for notes

Figure 31

FLIP FLOPS

dc test circuits (cont.)

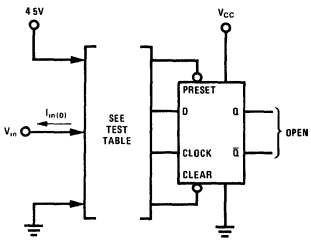


Notes 1 Each flip flop is tested separately
2 Each output is tested separately

TEST TABLE **

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Figure 32

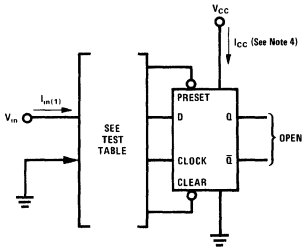


Notes 1 Each flip flop is tested separately
2 Each input is tested separately

TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY 4.5V	APPLY GND
Clock	Clear	Preset and D
Preset	None	Clear, Clock, and D
Clear	Clock and D	Preset
D	Clear and Clock	Preset

Figure 33

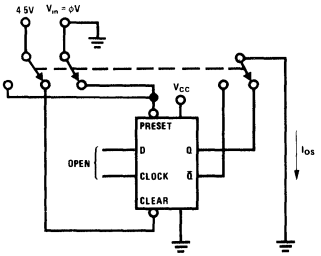


Notes 1 Each flip flop is tested separately
2 Each input is tested separately
3 GND is momentarily applied to clock, then 4.5V
4 I_{CC} is measured with D, clock, and preset at GND, then with D, clock and clear at GND

TEST TABLE

APPLY V_I (TEST I_{IH})	APPLY 4.5V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	Preset	Clock and D
Clear	Preset	D and Clock (See Note 3)
D	Preset and clock	Clear

Figure 34

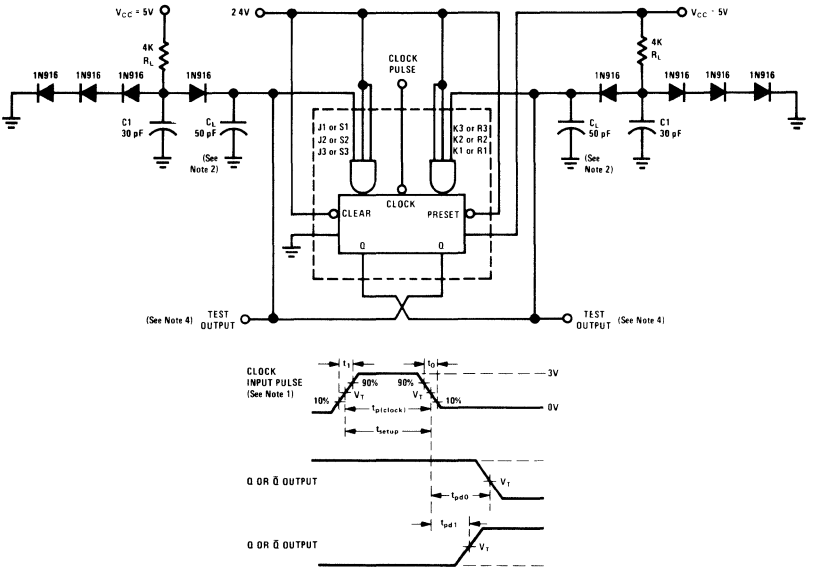


Note Each output is tested separately

Figure 35

**See page 3-14 for notes

ac test circuits and waveforms



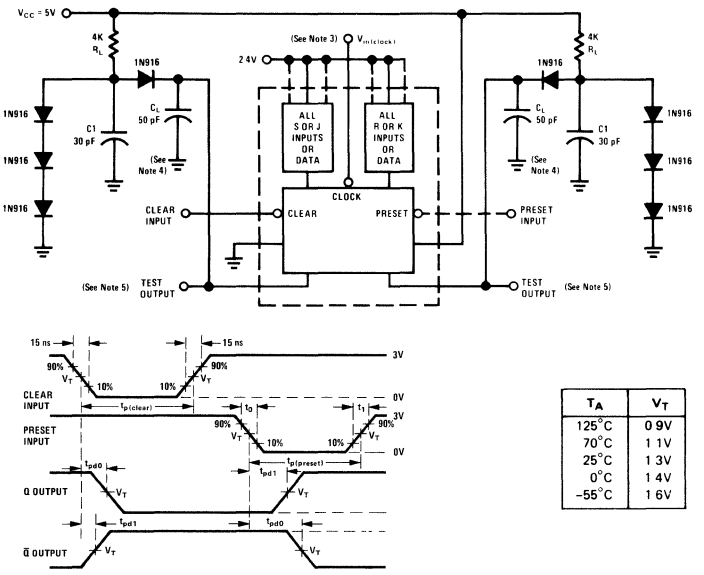
Notes 1 Clock input characteristics $t_1 = t_0 = 15$ ns, $t_p \geq 200$ ns, and PRR = 500 kHz
When testing f_{clock}, use 50% duty cycle

2 C_L includes probe and jig capacitance

3 DM54L73/DM74L73 and DM54L78/DM74L78, J = K = 2.4V

4 Load is applied to both outputs

Figure 36



T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
−55°C	1.6V

Notes 1 Clear or preset inputs dominate regardless of the state of clock or logic inputs

2 Clear or preset input pulse characteristics $t_{p(clear)} = t_{p(preset)} \geq 100$ ns, and PRR = 500 kHz

3 See applicable circuit type for actual synchronous and asynchronous input configuration

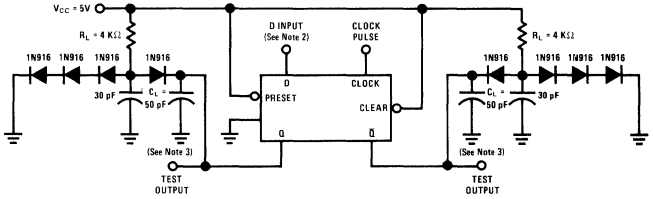
4 C_L includes probe and jig capacitance

5 Load is applied to both outputs

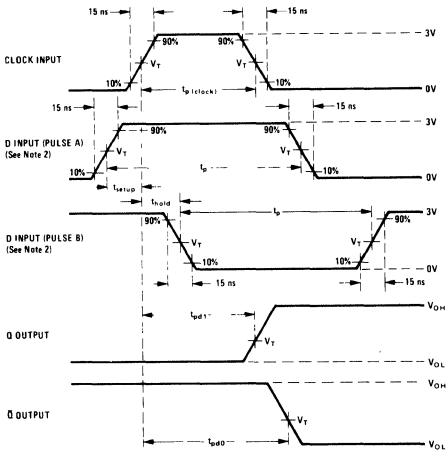
Figure 37

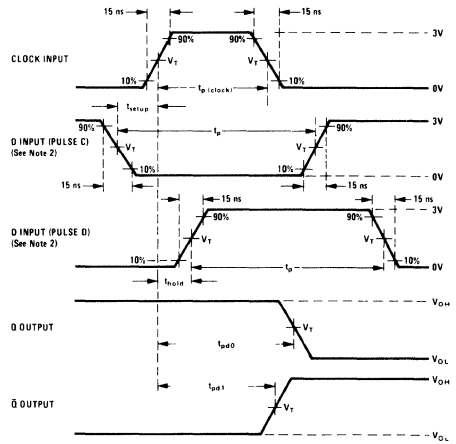
FLIP FLOPS

ac test circuits and waveforms (cont.)



T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
-55°C	1.6V



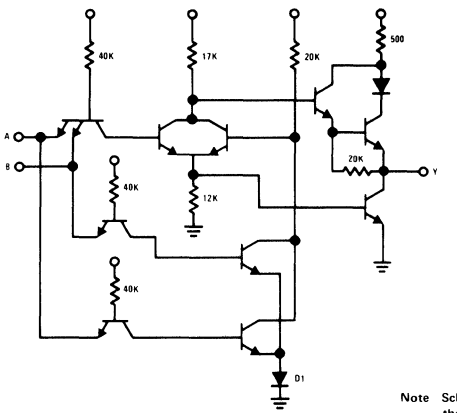


Notes 1 Clock input pulse has the following characteristics $t_{p(clock)} \geq 200$ ns and PRR = 500 kHz When testing f_{clock}, use 50% duty cycle
2 D input (pulse A and C) have the following characteristics t_{setup} = 30 ns, t_p = 100 ns and PRR is 50% of the clock PRR
D input (pulse B) has the following characteristics t_{hold} = 15 ns, t_p = 80 ns and PRR is 50% of the clock PRR
D input (pulse D) has the following characteristics t_{hold} = 10 ns, t_p = 80 ns and PRR is 50% of the clock PRR
3 C_L includes probe and jig capacitance

Figure 38

EXCLUSIVE-OR GATES (DM54L86/DM74L86)

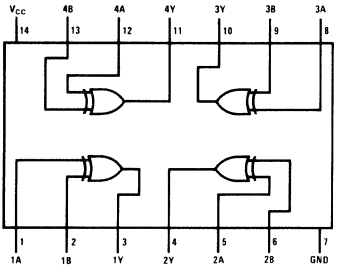
schematic diagram



Note Schematic diagram shows only one of the four exclusive OR-gates

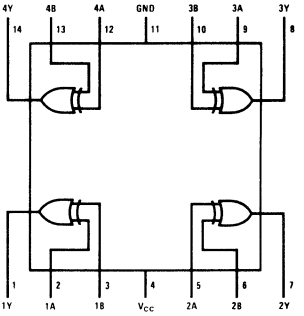
DM54L86/DM74L86

dual-in-line package connection diagram



DM54L86/DM74L86

flat package connection diagram



DM54L86/DM74L86

dc electrical characteristics

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS (Note 1)	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Input Voltage Required to Ensure Logical "1" at Any Input Terminal	39	V_{CC} = MIN	2	1 3		V
$V_{IN(0)}$	Input Voltage Required to Ensure Logical "0" at Any Input Terminal	39	V_{CC} = MIN		1 3	0 7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	39	V_{CC} = MIN, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0 7V, I_{LOAD} = −200 μA	2 4	2 8		V
$V_{OUT(0)}$	Logical "0" Output Voltage	40	V_{CC} = MIN, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0 7V, I_{OUT} = 2mA		0 15	0 3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	1	V_{CC} = MIN, I_{SINK} = 3 2 mA V_{IN} (All Inputs) = 2V		0 2	0 4	V
$I_{IN(1)}$	Logical "1" Level Input Current (Each Input)	41	V_{CC} = MAX, V_{IN} = 2.4V V_{CC} = MAX, V_{IN} = 5 5V		<2	20 200	μA μA
$I_{IN(0)}$	Logical "0" Level Input Current (Each Input)	42	V_{CC} = MAX, V_{IN} = 0 3V		−0 22	−0 36	mA
I_{OS}	Short Circuit Output Current	43	V_{CC} = MAX, $V_{IN(1)}$ = 4 5V, $V_{IN(0)}$ = 0	−3	−9	−15	mA
$I_{CC(0)}$	Supply Current (Per Gate)	44	V_{CC} = MAX			1 67	mA
$I_{CC(1)}$	Supply Current (Per Gate)	43	V_{CC} = MAX, $V_{IN(1)}$ = 4 5V, $V_{IN(0)}$ = 0			1 10	mA

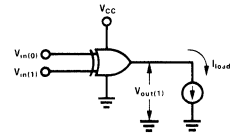
Note 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type

EXCLUSIVE-OR GATES
switching characteristics

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
t_{pd0}	Propagation Delay Time to Logical "0" Level (Other Input Low)	45	C_L = 50 pF, R_L = 4 kΩ		21	60	ns
t_{pd1}	Propagation Delay Time to Logical "1" Level (Other Input Low)	45	C_L = 50 pF, R_L = 4 kΩ		37	60	ns
t_{pd0}	Propagation Delay Time to Logical "0" Level (Other Input High)	45	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation Delay Time to Logical "1" Level (Other Input High)	45	C_L = 50 pF, R_L = 4 kΩ		25	60	ns

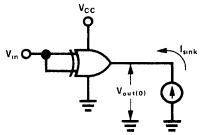
Note 1: Switching parameter limits, switching parameter typicals, and electrical parameter typicals are given for V_{CC} = 5V at T_A = 25°C only.

dc test circuits



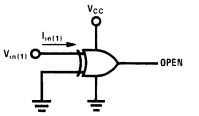
Note Each input is tested separately

Figure 39



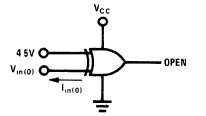
Note Logical "0" and logical "1" input conditions are tested

Figure 40



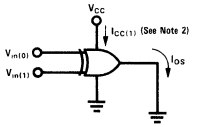
Note Each input is tested separately

Figure 41



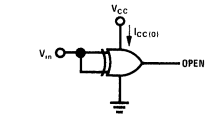
Note Each input is tested separately

Figure 42



Notes 1 Each gate is tested separately
2 When testing $I_{CC(1)}$, the output is open

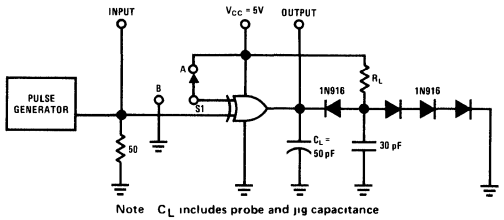
Figure 43



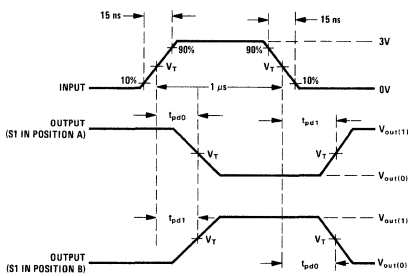
Note Logical "0" and logical "1" input conditions are tested

Figure 44

ac test circuits and waveforms



Note C_L includes probe and jig capacitance

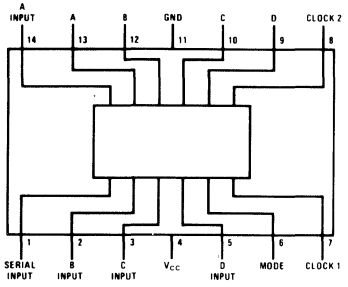


T_A	V_T
125°C	0 9V
70°C	1 1V
25°C	1 3V
0°C	1 4V
-55°C	1 6V

Figure 45

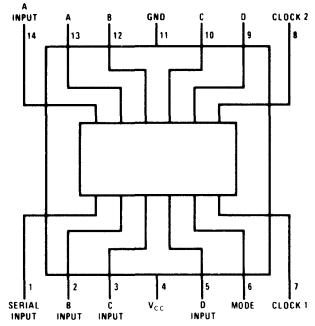
(DM54L95/DM74L95)

connection diagram dual-in-line package



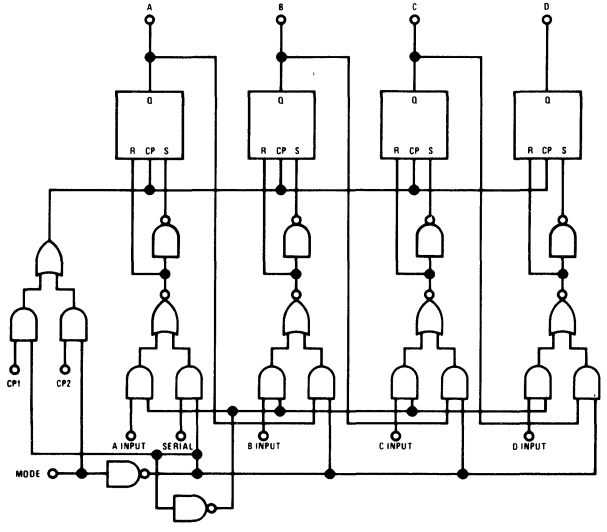
DM54L95/DM74L95

flat package connection diagram



DM54L95/DM74L95

logic diagram



TRUTH TABLE

Mode	Ser_n	Inp A_n	Inp B_n	Inp C_n	Inp D_n	A_{n+1}	B_{n+1}	C_{n+1}	D_{n+1}
1		1	1	1	1	1	1	1	1
1		0	0	0	0	0	0	0	0
0	1					1	An	Bn	Cn
0	0					0	An	Bn	Cn

DM54L95/DM74L95

SHIFT REGISTERS

electrical characteristics (DM54L95/DM74L95)

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN		46, 48	2 0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN		47, 49			0.7	
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN	I_{OUT} = -200 μA	46, 48	2 4	3.1		
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN	I_{OUT} = +2 mA	47, 49		0.13	0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN	I_{OUT} = 3 2 mA	47, 49		0 2	0.4	V
$I_{IN(0)}$	Logical "0" Input Current (Except Mode)	V_{CC} = MAX	V_{IN} = 0 3V	50		-0 1	-0.18	mA
$I_{IN(0)}$	Logical "0" Input Current (Mode Only)	V_{CC} = MAX	V_{IN} = 0 3V	50		-0 2	-0 36	mA
$I_{IN(1)}$	Logical "1" Input Current (Except Mode)	V_{CC} = MAX	V_{IN} = 2 4V V_{IN} = 5 5V	51			10 100	μA μA
$I_{IN(1)}$	Logical "1" Input Current (Mode Only)	V_{CC} = MAX	V_{IN} = 2.4V V_{IN} = 5 5V	51			20 200	μA μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX	V_{OUT} = 0V	52	-3	-9	-15	mA
I_{CC}	Supply Current	V_{CC} = MAX		53		4 8	8 0	mA

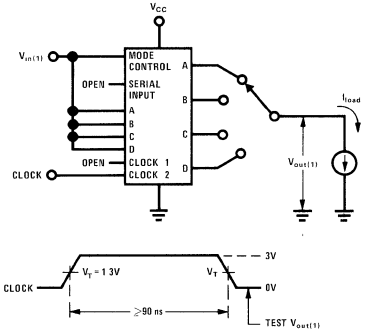
switching characteristics (DM54L95/DM74L95) (Note 1)

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Shift Frequency	V_{CC} = 5 0V C_L = 50 pF		54	6 0	14		MHz
$t_{pW(CLOCK)}$	Clock Pulse Width	V_{CC} = 5 0V C_L = 50 pF		54	90	44		ns
$t_{pd(1)}$	Propagation Delay to a Logical "1" A, B, C, or D	V_{CC} = 5 0V C_L = 50 pF		54	15	42	90	ns
$t_{pd(0)}$	Propagation Delay to a Logical "0" A, B, C, or D	V_{CC} = 5 0V C_L = 50 pF		54	15	48	90	ns
t_1	Mode Control Logical "0" Setup Time With Respect to CP1	V_{CC} = 5 0V C_L = 50 pF		55	120	55		ns
t_2	Mode Control Logical "1" Setup Time With Respect to CP2	V_{CC} = 5 0V C_L = 50 pF		56	100	45		ns
t_3	Mode Control Logical "0" Setup Time With Respect to CP2	V_{CC} = 5 0V C_L = 50 pF	(Note 2)	56	0	-43		ns
t_4	Mode Control Logical "1" Setup Time With Respect to CP1	V_{CC} = 5 0V C_L = 50 pF	(Note 2)	55	0	-50		ns
t_5	Logical "1" Setup Time at Serial, A, B, C, or D Inputs	V_{CC} = 5 0V C_L = 50 pF		54	50	20		ns
t_6	Logical "0" Setup Time at Serial, A, B, C, or D Inputs	V_{CC} = 5 0V C_L = 50 pF		54	50	13		ns
t_7	Logical "1" Hold Time at Serial, A, B, C, or D Inputs	V_{CC} = 5 0V C_L = 50 pF	(Note 2)	54	0	-14		ns
t_8	Logical "0" Hold Time at Serial, A, B, C, or D Inputs	V_{CC} = 5 0V C_L = 50 pF	(Note 2)	54	0	-20		ns

Note 1: Switching parameter limits, switching parameter typicals, and electrical parameter typicals are given for V_{CC} = 5V at T_A = 25°C only

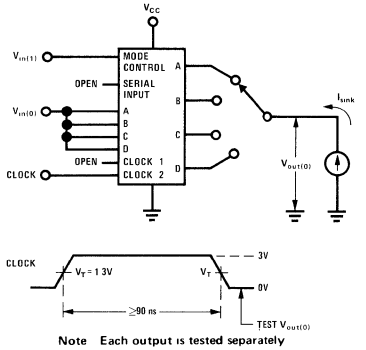
Note 2: Negative hold time values indicate that data can be released prior to the time the clock reaches its 1.3V level

dc test circuits (DM54L95/DM74L95)



Note Each output is tested separately

Figure 46



Note Each output is tested separately

Figure 47

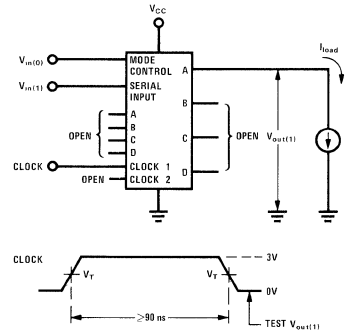


Figure 48

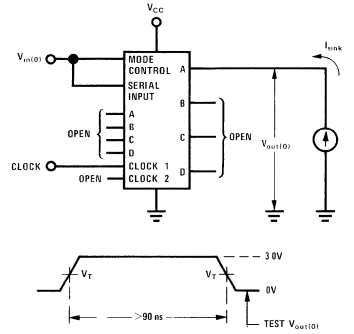
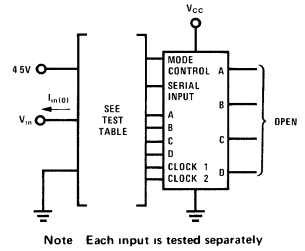


Figure 49

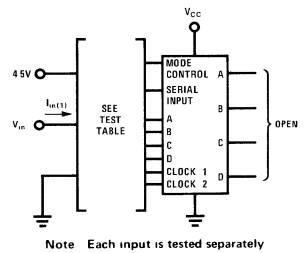


Note Each input is tested separately

TEST TABLE

TEST	APPLY 4 5V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
A INPUT	MODE CONTROL	NONE
B INPUT	MODE CONTROL	NONE
C INPUT	MODE CONTROL	NONE
D INPUT	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

Figure 50



Note Each input is tested separately

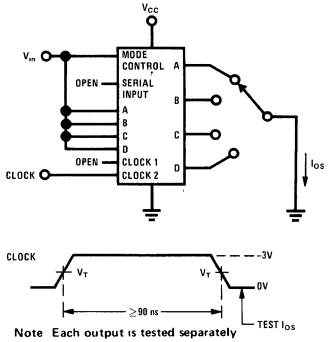
TEST TABLE

TEST	APPLY 4 5V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
A INPUT	NONE	MODE CONTROL
B INPUT	NONE	MODE CONTROL
C INPUT	NONE	MODE CONTROL
D INPUT	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

Figure 51

SHIFT REGISTERS

dc test circuits (cont.) (DM54L95/DM74L95)



Note Each output is tested separately

Figure 52

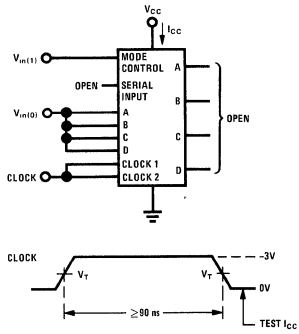
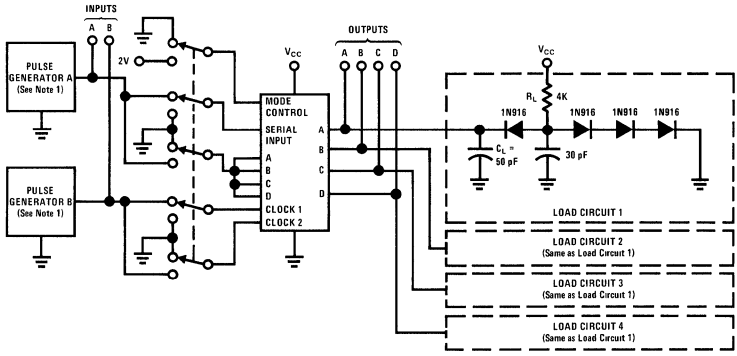
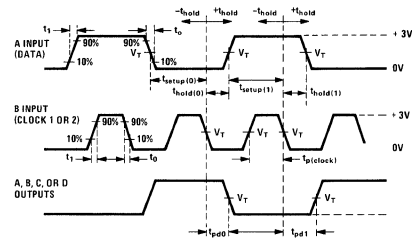


Figure 53

ac test circuits and waveforms (DM54L95/DM74L95)



Notes 1 The pulse generators have the following characteristics t_1 = 10 ns to 12 ns, t_0 = 10 ns to 12 ns, and $Z_{out} \approx 50\Omega$
For pulse generator A t_p = 150 ns and PRR = 500 kHz For pulse generator B t_p = 10 ns and PRR = 1 MHz
When testing f_{max}, vary PRR
2 Voltage values are with respect to network ground terminal
3 C_L includes probe and jig capacitance



T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
-55°C	1.6V

Figure 54

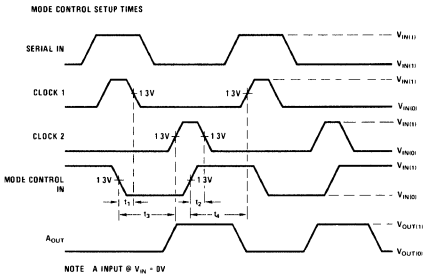
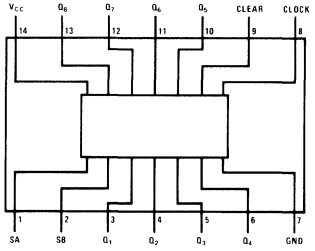


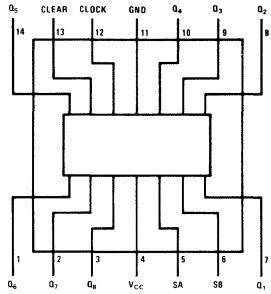
Figure 55

dual-in-line package connection diagram



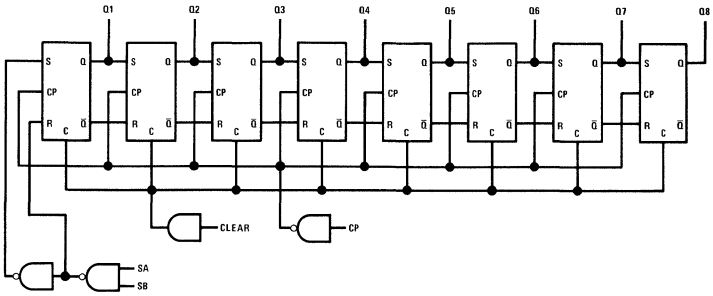
DM76L70/DM86L70

flat package connection diagram



DM76L70/DM86L70

logic diagrams



DM76L70/DM86L70

electrical characteristics (DM76L70/DM86L70) (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN	2.0	1.3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MAX		1.3	0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN, I_{OUT} = -200 μA	2.4	2.8		V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA			0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3.2 mA		<1	0.4	V
$I_{IN(1)}$	Logical "1" Input Current (Except Clear Input)	V_{CC} = MAX, V_{IN} = 2 4V		<2	10	μA
$I_{IN(1)}$	Logical "1" Input Current (Clear Input)	V_{CC} = MAX, V_{IN} = 2.4V			20	μA
$I_{IN(1)}$	Logical "1" Input Current (Except Clear Input)	V_{CC} = MAX, V_{IN} = 5.5V			100	μA
$I_{IN(1)}$	Logical "1" Input Current (Clear Input)	V_{CC} = MAX, V_{IN} = 5.5V			200	μA
$I_{IN(1)}$	Logical "0" Input Current (Except Clear Input)	V_{CC} = MAX, V_{IN} = 0.3V		-120	-180	μA
$I_{IN(0)}$	Logical "0" Input Current (Clear Input)	V_{CC} = MAX, V_{IN} = 0.3V		-240	-360	μA
I_{OS}	Output Short Circuit Current (Note 2)	V_{CC} = MAX, V_{OUT} = 0V	-3	-9	-15	mA
I_{CC}	Power Supply Current	V_{CC} = MAX		6	9	mA

Note 1: Switching parameter limits, switching parameter typicals, and electrical parameter typicals are given for V_{CC} = 5V at T_A = 25°C only

Note 2: Only one output should be shorted at a time.

SHIFT REGISTERS

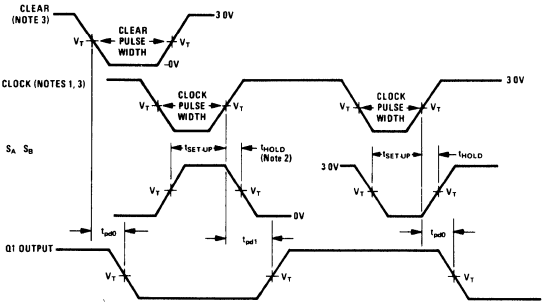
switching characteristics (DM76L70/DM86L70)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{MIN}	Minimum Clock Frequency	V_{CC} = 5 0V, 50% Duty Cycle	6	12		MHz
t_{pd0}	Propagation Delay to a Logical "0" From Clock to Output	V_{CC} = 5 0V, C_L = 50 pF		70	120	ns
t_{pd1}	Propagation Delay to a Logical "1" From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF		40	90	ns
t_{pd0}	Propagation Delay to a Logical "0" From Clear to Output	V_{CC} = 5.0V, C_L = 50 pF		90	160	ns
$t_{PW(CLOCK)}$	Minimum Clock Pulse Width	V_{CC} = 5 0V, C_L = 50 pF	40	25		ns
$t_{PW(CLEAR)}$	Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF	40	25		ns
t_{SET-UP}	Minimum Time That $S_A \cdot S_B$ Data Must be Set-up Prior to Clock Pulse, $t_{set\ up}$	V_{CC} = 5 0V, C_L = 50 pF		35	60	ns
t_{HOLD}	Minimum Time That $S_A \cdot S_B$ Data Must be Held After Clock Pulse, t_{hold}	V_{CC} = 5 0V, C_L = 50 pF	-10	-35		ns
t_{CR}	Clear Recovery Time*	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF		80	120	ns

*Time required after removal of clear signal for clocking to occur.

**Negative hold times indicate that data may be released prior to time clock reaches its 1.3V level.

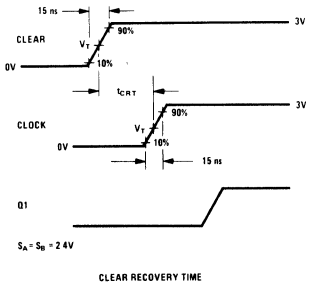
switching waveforms (DM76L70/DM86L70)



Notes. 1. Clock may be at either a Logical "1" or a Logical "0" while clearing.

2 Negative hold time values indicate S_A S_B information may be released prior to the time the clock pulse reaches its 1 3V level

3 Clear and Clock Waveforms· $t_r = t_f$ = 15 ns (10%–90%, 90%–10% transition) f = 1 MHz



CLEAR RECOVERY TIME

Figure 56

Series 54L/74L

DM54L42A/DM74L42A (SN54L42A/SN74L42A) low power BCD to decimal decoder

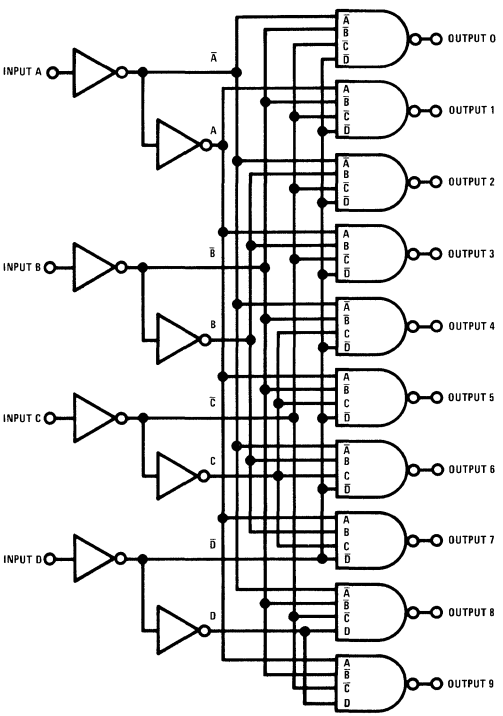
general description

The DM54L42A/DM74L42A one-of-ten decoder produces a low-power TTL logical "0" for the decimal output corresponding to a BCD input value from zero to nine, and a logical "1" for the other nine outputs. When a BCD input greater than nine is presented, all outputs are logical "1". Conventional low-power TTL output gates assure excellent low-power speeds and fan-out.

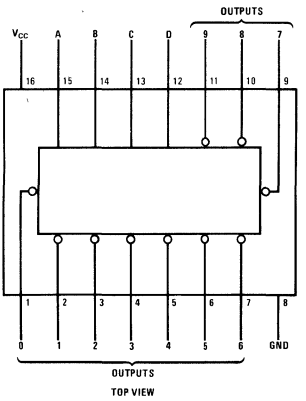
features

- Series 54L/74L compatible
- 15 mW typical power dissipation
- 50 ns typical propagation delay

logic and connection diagrams



Dual-In-Line Package & Flat Package



truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings (Note 1)

Supply Voltage		+8V
Input Voltage		+5.5V
Output Voltage		+5.5V
Operating Temperature Range	DM54L42A	−55°C to +125°C
	DM74L42A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		+300°C

electrical characteristics (Note 2)

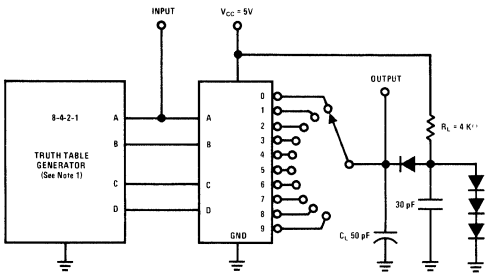
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L42A	V_{CC} = 4.5V		2.0	1.3		V
	DM74L42A	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM54L42A	V_{CC} = 4.5V			1.3	0.7	V
	DM74L42A	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM54L42A	V_{CC} = 4.5V	I_{OUT} = −200 μA	2.4	2.8		V
	DM74L42A	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM54L42A	V_{CC} = 4.5V	I_{OUT} = 2 mA		0.15	0.30	V
	DM74L42A	V_{CC} = 4.75V	I_{OUT} = 3.2 mA		0.20	0.40	V
Logical "1" Input Current	DM54L42A	V_{CC} = 5.5V	V_{IN} = 2.4V		<1	10	μA
	DM74L42A	V_{CC} = 5.25V					
	DM54L42A	V_{CC} = 5.5V	V_{IN} = 5.5V		<1	100	μA
	DM74L42A	V_{CC} = 5.25V					
Logical "0" Input Current	DM54L42A	V_{CC} = 5.5V	V_{IN} = 0.3V		−0.10	−0.18	mA
	DM74L42A	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM54L42A	V_{CC} = 5.5V	V_{OUT} = 0V	−3.0	−9.0	−15.0	mA
	DM74L42A	V_{CC} = 5.25V					
Supply Current I_{CC} max	DM54L42A	V_{CC} = 5.5V			3.0	5.3	mA
	DM74L42A	V_{CC} = 5.25V					
Propagation Delay to a Logical "0" from Any BCD Input to Any Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF	35	70	140	ns
Propagation Delay to a Logical "1" from Any BCD Input to Any Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF	15	35	70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L42A and across the 0°C to 70°C range for the DM74L42A All typicals are given for V_{CC} = 5 0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

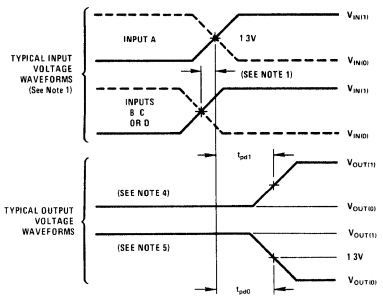
switching times



Note 1 The truth table generator has the following characteristics $V_{OUT(1)} > 2.4V$, $V_{OUT(0)} < 0.4V$, t_r and $t_f < 15$ ns, and PRR = 1 MHz Input B, C, and D transitions occur simultaneously with or prior to input A transitions

Note 2 C_L includes probe and jig capacitance

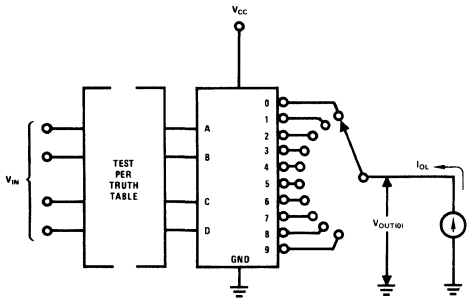
Note 3 All diodes are 1N3064 or equivalent



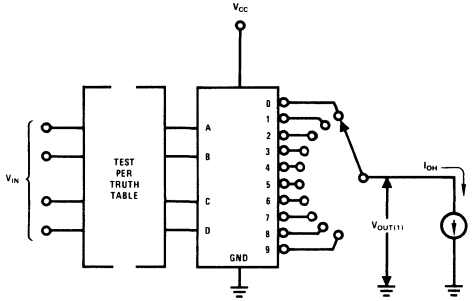
Note 4 This waveform represent the Q output when A in goes from "0" to "1" (i e) with B=C=D="0"

Note 5 This waveform represents the Q output when A goes from (i e) "1" to "0" with B=C=D="0"

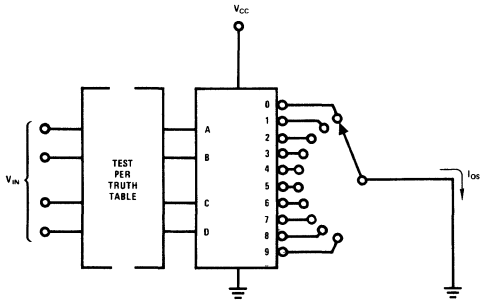
dc test circuits



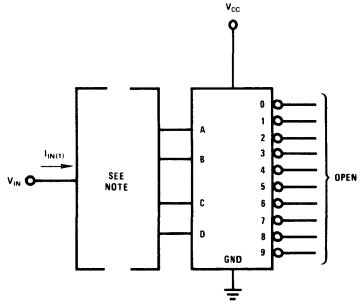
Note Each output is tested separately



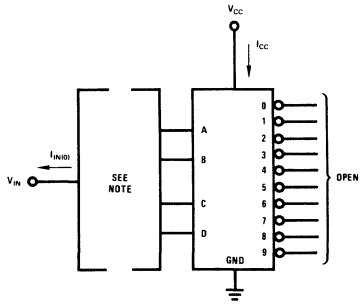
Note Each output is tested separately



Note Each output is tested separately



Note Each input is tested separately



Note 1 When testing $I_{IN(0)}$ each input is tested separately

Note 2 When testing I_{CC} all inputs are grounded and outputs are open

Series 54L/74L

DM54L85/DM74L85 (SN54L85/SN74L85)
4-bit magnitude comparator

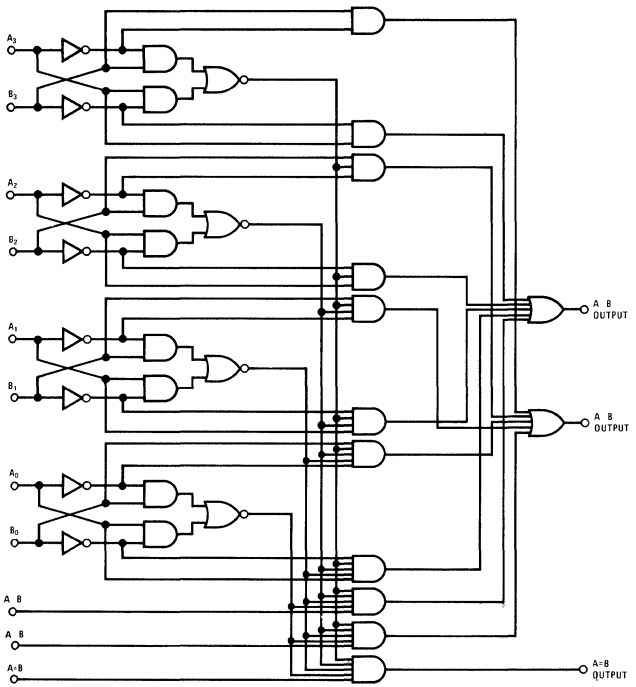
general description

The DM54L85/DM74L85 low power TTL 4-bit magnitude comparator is compatible with most TTL and DTL families. This comparator compares two 4-bit words and determines their relative magnitude with the result being indicated by a high level at the A>B, A<B, or A=B output. The DM54L85/DM74L85 may be connected in cascade to compare words of greater length. The A>B, A<B, and A=B outputs of a stage handling less significant bits are connected to the corresponding inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a low-level voltage applied to A>B and A<B inputs and a high-level voltage applied to the A=B input.

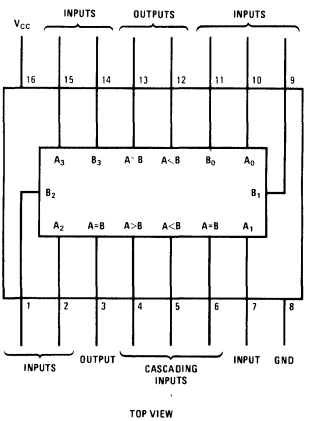
features

- Power dissipation typically 20 mW
- 55 ns typical propagation delay time
- TTL and DTL compatible
- May be cascaded to compare words of greater length

logic and connection diagrams



Dual-In-Line and Flat Package



absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range DM54L85	−55°C to 125°C
DM74L85	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

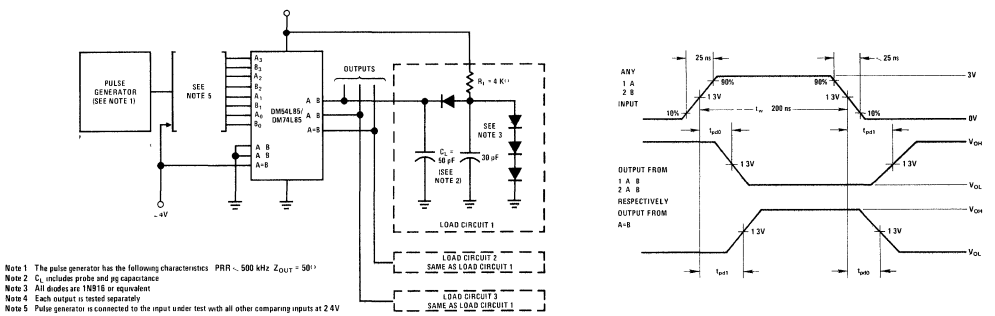
electrical characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L85	V_{CC} = 4.5V		2	1.3		V
	DM74L85	V_{CC} = 4.75V		2	1.3		V
Logical "0" Input Voltage	DM54L85	V_{CC} = 4.5V			1.3	0.7	V
	DM74L85	V_{CC} = 4.75V			1.3	0.7	V
Logical "1" Output Voltage	DM54L85	V_{CC} = 4.5V	I_{OUT} = −200 μA	2.4	2.8		V
	DM74L85	V_{CC} = 4.75V	V_{IN} = 0.7V, Other Inputs = 2V	2.4	2.8		V
Logical "0" Output Voltage	DM54L85	V_{CC} = 4.5V	I_{OUT} = 2 mA V_{IN} (All Inputs) = 0.7V		0.15	0.3	V
	DM74L85	V_{CC} = 4.75V	I_{OUT} = 3.2 mA V_{IN} (All Inputs) = 0.7V		0.2	0.4	V
Logical "1" Input Current	DM54L85	V_{CC} = 5.5V	V_{IN} = 2.4V (Comparing Inputs)		<3	30	μA
	DM74L85	V_{CC} = 5.25V	V_{IN} = 5.5V (Comparing Inputs)		<30	300	μA
	DM54L85	V_{CC} = 5.5V	V_{IN} = 2.4V (Cascading Inputs)		<1	10	μA
	DM74L85	V_{CC} = 5.25V	V_{IN} = 5.5V (Cascading Inputs)		<10	100	μA
Logical "0" Input Current	DM54L85	V_{CC} = 5.5V	V_{IN} = 0.3V (Comparing Inputs)		−360	−540	μA
	DM74L85	V_{CC} = 5.25V	Other Inputs = 0V		−360	−540	μA
	DM54L85	V_{CC} = 5.5V	V_{IN} = 0.3V (Cascading Inputs)		−120	−180	μA
	DM74L85	V_{CC} = 5.25V	Other Inputs = 4.5V		−120	−180	μA
Output Short Circuit Current	DM54L85	V_{CC} = 5.5V	V_{OUT} = 0V, V_{IN} (Comparing Inputs) = 0V	−3	−8	−15	mA
	DM74L85	V_{CC} = 5.25V	V_{IN} (Cascading Inputs) = 4.5V	−3	−8	−15	mA
Supply Current — Logical "1"	DM54L85	V_{CC} = 5.5V	V_{IN} = 4.5V			6.6	mA
	DM74L85	V_{CC} = 5.25V				6.6	mA
Logical "0"	DM54L85	V_{CC} = 5.5V	V_{IN} = 0V			7.0	mA
	DM74L85	V_{CC} = 5.25V				7.0	mA
Propagation Delay to a Logical "0" from Any Comparing Input to Output, t_{pd0}		V_{CC} = 5V, T_A = 25°C			55	90	ns
Propagation Delay to a Logical "1" from Any Comparing Input to Output, t_{pd1}		V_{CC} = 5V, T_A = 25°C			70	115	ns
Propagation Delay to a Logical "0" from Any Cascading Input to Output, t_{pd0}		V_{CC} = 5V, T_A = 25°C			40	65	ns
Propagation Delay to a Logical "1" from Any Cascading Input to Output, t_{pd1}		V_{CC} = 5V, T_A = 25°C			55	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L85 and across the 0°C to 70°C range for the DM74L85. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ac test circuit and switching waveforms



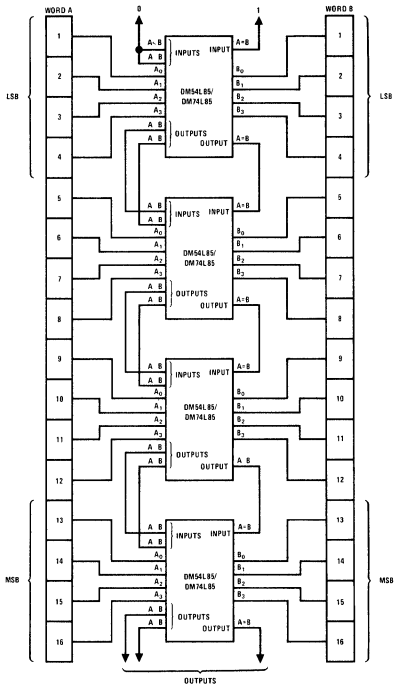
Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, Z_{OUT} = 50Ω
Note 2: C_L includes probe and jig capacitance
Note 3: All diodes are 1N916 or equivalent
Note 4: Each output is tested separately
Note 5: Pulse generator is connected to the input under test with all other comparing inputs at 2.4V

FIGURE 1 Propagation Times from Comparing Inputs

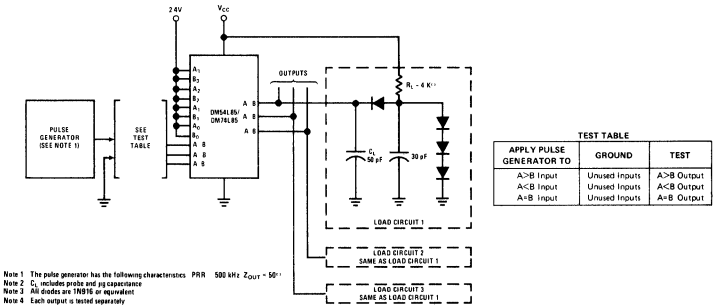
typical application

Longer Word Comparison

Comparing Two 16 Bit Words



ac test circuit and switching waveforms (con't)



TEST TABLE

APPLY PULSE GENERATOR TO	GROUND	TEST
A>B Input	Unused Inputs	A>B Output
A<B Input	Unused Inputs	A<B Output
A=B Input	Unused Inputs	A=B Output

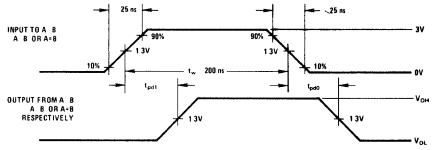


FIGURE 2. Propagation Times from Cascading Inputs

Series 54L/74L

DM54L90/DM74L90(SN54L90/SN74L90)
low power decade counter

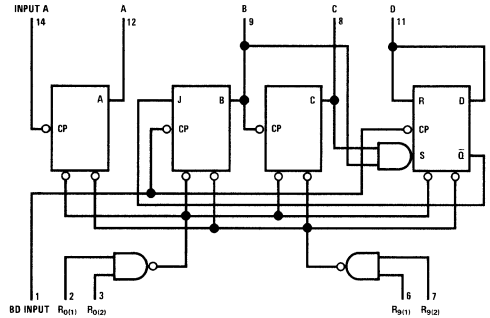
general description

The DM54L90/DM74L90 is a low power decade counter which can be reset to zero or preset to the 9 state. Internal logic has been kept to a minimum by using an R-S flip flop on the D bit and J-K flip flops on the A, B and C bits. A separate flip flop on the A bit enables the user to operate the device as a divide-by-five or divide-by-ten frequency divider In addition the A flip flop can be used for a basic divide-by-two section. All outputs are standard low power T^2L Darlington configurations capable of fanning out to 2 standard T^2L unit loads over the commercial temperature range and 10 54L/74L loads in the low state In addition these devices can fanout to 20 54L/74L loads in the high state.

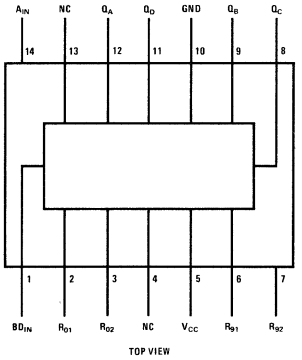
features

- 20 mW typical power dissipation
- 11 MHz typical clock frequency
- Same pin-out as standard SN5490/SN7490

logic and connection diagrams



Dual-In-Line and Flat Package



truth tables

BCD Count Sequence
(See Note 1)

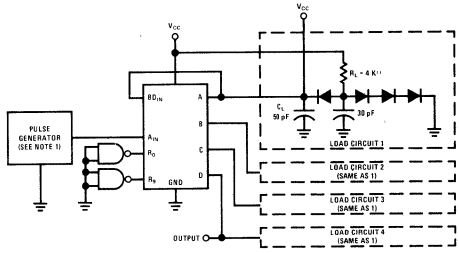
COUNT	OUTPUT			
	0	0	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Reset Count
(See Note 2)

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

Note 1 Output A connected to input BD for BCD count
Note 2 X indicates that either a logical 1 or a logical 0 may be present

ac test circuit



absolute maximum ratings (Note 1)

Supply Voltage	+8 0V
Input Voltage	+5 5V
Output Voltage	+5 5V
Operating Temperature Range DM54L90	−55°C to +125°C
DM74L90	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

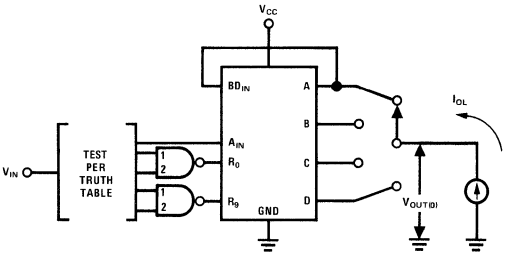
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L90	V_{CC} = 4 5V		2 0	1 3		V
	DM74L90	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM54L90	V_{CC} = 4 5V	A_{IN} & BD_{IN}		1.2	0 6	V
	DM74L90	V_{CC} = 4 75V	Other Inputs		1 3	0 7	V
Logical "1" Output Voltage	DM54L90	V_{CC} = 4 5V	I_{OUT} = −200 μA	2 4	2 8		V
	DM74L90	V_{CC} = 4 75V					
Logical "0" Output Voltage	DM54L90	V_{CC} = 4 5V	I_{OUT} = +2 mA		0 15	0 30	V
	DM74L90	V_{CC} = 4 75V	I_{OUT} = +3 2 mA		0 20	0 40	V
Logical "1" Input Current	DM54L90	V_{CC} = 5 5V	V_{IN} = 2 4V Reset Inputs			10	μA
	DM74L90	V_{CC} = 5 25V	V_{IN} = 5 5V Reset Inputs			100	μA
	DM54L90	V_{CC} = 5 5V	V_{IN} = 2 4V A_{IN}			20	μA
	DM74L90	V_{CC} = 5 25V	V_{IN} = 5 5V A_{IN}			200	μA
	DM54L90	V_{CC} = 5 5V	V_{IN} = 2 4V BD_{IN}			40	μA
	DM74L90	V_{CC} = 5 25V	V_{IN} = 5 5V BD_{IN}			400	μA
Logical "0" Input Current	DM54L90	V_{CC} = 5 5V	V_{IN} = 0 3V, Reset Inputs			−0 18	mA
	DM74L90	V_{CC} = 5 25V					
	DM54L90	V_{CC} = 5 5V	V_{IN} = 0 3V, A_{IN}			−0 36	mA
	DM74L90	V_{CC} = 5 25V					
	DM54L90	V_{CC} = 5 5V	V_{IN} = 0 3V, BD_{IN}			−0 72	mA
	DM74L90	V_{CC} = 5 25V					
Output Short Circuit Current (Note 3)	DM54L90	V_{CC} = 5 5V	V_{OUT} = 0V	−3	−9	−15	mA
	DM74L90	V_{CC} = 5 25V					
I_{CC} Max	DM54L90	V_{CC} = 5 5V				5 5	mA
	DM74L90	V_{CC} = 5 25V					
Propagation Delay to a Logical "0" from A_{IN} to D_{OUT}, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ	95	190	300	ns
Propagation Delay to a Logical "1" from A_{IN} to D_{OUT}, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ	90	175	300	ns
Maximum Clock Frequency		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ	6	11		MHz
Clock Pulse Width		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ	90			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

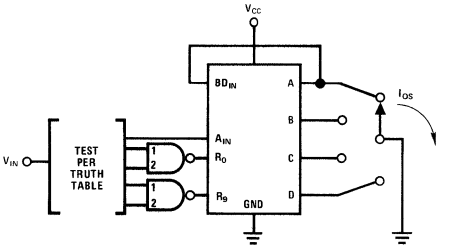
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L90, and across the 0°C to 70°C range for the DM74L90 All typicals are given for V_{CC} = 5 0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

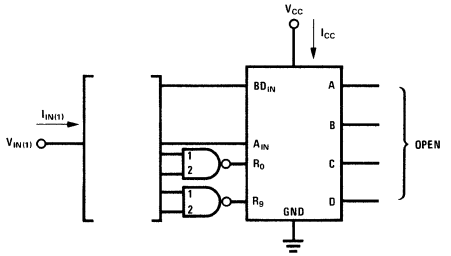
parameter measurement information



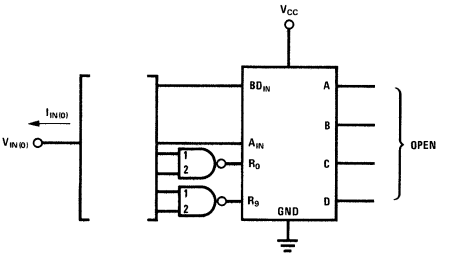
Note 1 Each output is tested in the logical "0" state



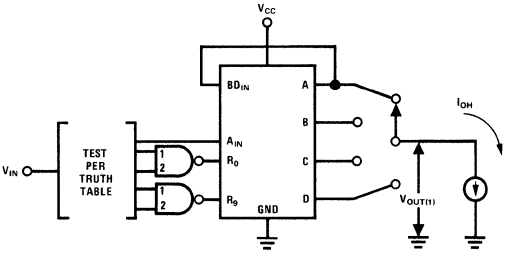
Note 1 Each output is tested in the logical "1" state



Note 1 Each input is tested separately
Note 2 When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$
Note 3 When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$
Note 4 When testing I_{CC} reset all outputs to logical "0", ground all inputs, then measure I_{CC}

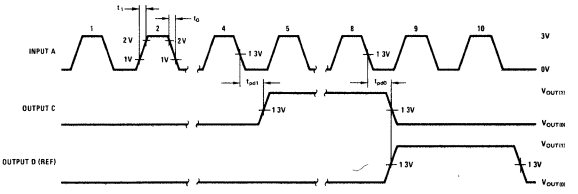


Note 1 Each input is tested separately
Note 2 When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5V to $R_{0(2)}$ or $R_{9(2)}$
Note 3 When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5V to $R_{0(1)}$ or $R_{9(1)}$



Each output is tested in the logical "1" state

switching time waveforms



Note 1 The pulse generator has the following characteristics: $V_{GEN} = 3V$, $t_0 = t_1 \leq 15$ ns, $f_0 = 0.5\ \mu s$, PRR = 1 MHz, $Z_{OUT} = 50\Omega$
Note 2 All diodes are 1N3064 or equivalent
Note 3 C_L includes probe and jig capacitance
Note 4 $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
Note 5 Voltage values are with respect to ground terminal

Series 54L/74L

DM54L91/DM74L91(SN54L91/SN74L91) 8-bit shift register

general description

The DM54L91/DM74L91 is a serial-in, serial-out, 8-bit shift register which utilizes low-power transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at typical clock rates of 8 MHz. Power dissipation is typically 17.5 milliwatts, and full fan-out of 10 is available from the outputs.

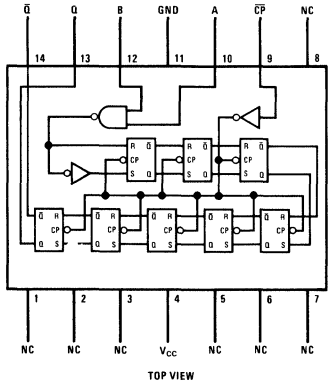
The register will shift information to the output on the positive transition of the clock.

features

- SN54L/74L Series compatible
- Fully compatible with edge-triggering flip-flops

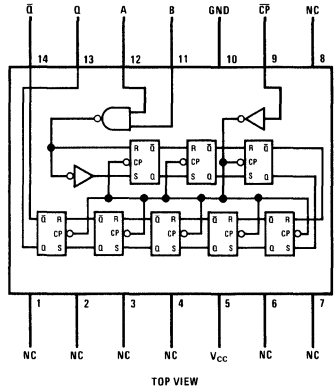
logic and connection diagrams

Flat Package



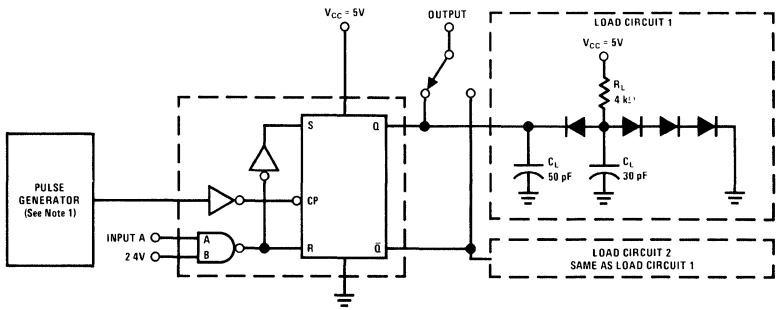
TOP VIEW

Dual-In-Line Package



TOP VIEW

dc test circuit



absolute maximum ratings (Note 1)

Supply Voltage	8 0V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54L91	4 5	5 5	V
DM74L91	4 75	5 25	V
Temperature (T_A)			
DM54L91	−55	+125	°C
DM74L91	0	70	°C

electrical characteristics (Note 2)

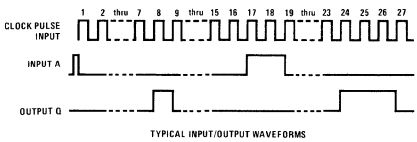
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2	1 3		V
Logical "0" Input Voltage			1 3	0 7	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200 μA	2 4	2 8		V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 2 mA (DM54L91) V_{CC} = Min, I_{OUT} = 3 2 mA (DM74L91)		0 15 0 2	0 3 0 4	V V
Logical "1" Input Current	V_{CC} = Max, Other Inputs = 0V, V_{IN} = 2 4V		<1	10	μA
	V_{IN} = 5 5V		<10	100	μA
Logical "0" Input Current	V_{CC} = Max, Other Inputs = 4 5V, V_{IN} = 0 3V		−110	−180	μA
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_{OUT} = 0V	−3	−8	−15	mA
Supply Current I_{CC} (Max)	V_{CC} = Max, V_{IN} = 5V		3 5	6 6	mA
f_{MAX} (maximum input clock frequency)	V_{CC} = 5 0V T_A = 25°C	4	8		MHz
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}	V_{CC} = 5 0V T_A = 25°C		65	130	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}	V_{CC} = 5 0V T_A = 25°C		40	80	ns
Minimum Width of Logical "0" Level Clock Pulse, $t_{p0(clock)}$	V_{CC} = 5 0V T_A = 25°C	120	60		ns
Minimum Width of Logical "1" Level Clock Pulse, $t_{p1(clock)}$	V_{CC} = 5 0V T_A = 25°C	120	60		ns
Input Setup Time, t_{setup}	V_{CC} = 5 0V T_A = 25°C	120			ns
Input Hold Time, t_{hold}	V_{CC} = 5 0V T_A = 25°C	0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

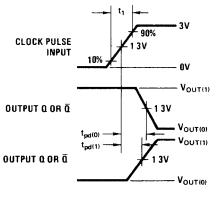
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L91, and across the 0°C to 70°C range for the DM74L91. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

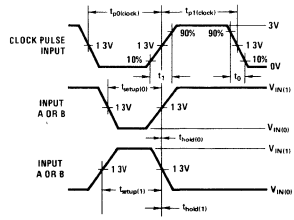
Note 3: Only one output at a time should be shorted

switching time waveforms



TYPICAL INPUT/OUTPUT WAVEFORMS





Note 1 The generator has the following characteristics $V_{IN(0)} < 0\ 3V$, $V_{IN(1)} > 2\ 4V$, $t_1 = t_0 = 15$ ns, $t_{pd(CLOCK)} = 500$ ns, $t_{pd0(CLOCK)} = 500$ ns, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$

Note 2 C_L includes probe and jig capacitance

Note 3 Each output is tested separately

Note 4 Voltage values are with respect to network ground terminal

Note 5 All diodes are 1N3064 or equivalent

Note 6 f_{MAX} use 50% duty cycle

Series 54L/74L

DM54L93/DM74L93(SN54L93/SN74L93) and DM76L93/DM86L93 ripple binary counters

general description

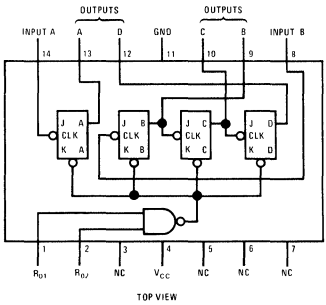
The DM54L93/DM74L93 and DM76L93/DM86L93 ripple binary counters enable a systems designer to have some flexibility in his design. The DM76L93/DM86L93 has the same pin out as the standard SN5493/SN7493, but the same power specifications as the SN54L93/SN74L93 low-power counter. Both counters can be used to divide-by-2, 8, or 16.

Two reset inputs are provided to allow for initializing the counters. Resetting occurs asynchronously when both reset inputs are high. Darlington outputs provide for a fanout capability of two standard TTL unit loads over the commercial temperature range and 10 54L/74L loads in the low state. In addition these devices can fan out to 20 54L/74L loads in the high state.

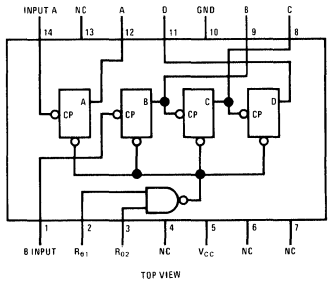
features

- Series 54L/74L compatible
- 15 MHz typical clock frequency
- 18 mW typical power dissipation

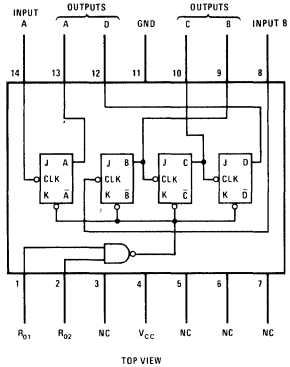
logic and connection diagrams



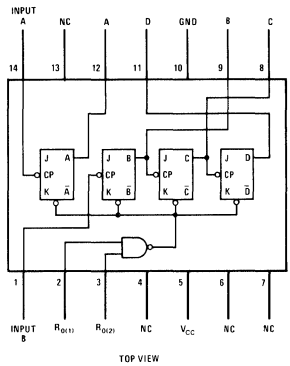
Dual-In-Line Package
DM54L93/DM74L93



Dual-In-Line Package
DM76L93/DM86L93



Flat Package
DM54L93/DM74L93



Flat Package
DM76L93/DM86L93

absolute maximum ratings (Note 1)

Supply Voltage		+8.0V
Input Voltage		+5.5V
Output Voltage		+5.5V
Operating Temperature Range	DM54L93,DM76L93	−55°C to +125°C
	DM74L93,DM86L93	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

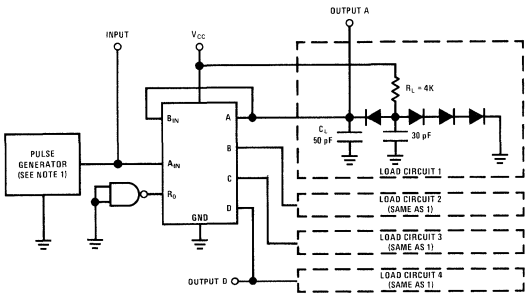
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L93, DM76L93	V_{CC} = 4 5V		2 0	1 3		V
	DM74L93, DM86L93	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM54L93, DM76L93	V_{CC} = 4 5V	A_{IN} & B_{IN}		1 2	0 6	V
	DM74L93, DM86L93	V_{CC} = 4 75V	Reset Inputs		1 3	0 7	V
Logical "1" Output Voltage	DM54L93, DM76L93	V_{CC} = 4 5V	I_{OUT} = −200 μA	2 4	2 8		V
	DM74L93, DM86L93	V_{CC} = 4 75V					
Logical "0" Output Voltage	DM54L93, DM76L93	V_{CC} = 4 5V	I_{OUT} = 2 mA		0 15	0 3	V
	DM74L93, DM86L93	V_{CC} = 4 75V	I_{OUT} = 3 2 mA		0 20	0 4	V
Logical "1" Input Current	DM54L93, DM76L93	V_{CC} = 5 5V	V_{IN} = 2 4V Reset Inputs			10	μA
	DM74L93, DM86L93	V_{CC} = 5 25V	V_{IN} = 5 5V Reset Inputs			100	μA
	DM54L93, DM76L93	V_{CC} = 5 5V	V_{IN} = 2 4V A_{IN} & B_{IN}			20	μA
	DM74L93, DM86L93	V_{CC} = 5 25V	V_{IN} = 5 5V A_{IN} & B_{IN}			200	μA
Logical "0" Input Current	DM54L93, DM76L93	V_{CC} = 5 5V	V_{IN} = 0 3V, R_{01} & R_{02}			−0 18	mA
	DM74L93, DM86L93	V_{CC} = 5 25V					
	DM54L93, DM76L93	V_{CC} = 5 5V	V_{IN} = 0 3V, A_{IN} & B_{IN}			−0 36	mA
	DM74L93, DM86L93	V_{CC} = 5 25V					
Output Short Circuit Current (Note 3)	DM54L93, DM76L93	V_{CC} = 5 5V	V_{OUT} = 0V	−3	−9	−15	mA
	DM74L93, DM86L93	V_{CC} = 5 25V					
I_{CC} max	DM54L93, DM76L93	V_{CC} = 5 5V				5 50	mA
	DM74L93, DM86L93	V_{CC} = 5 25V					
Propagation Delay to a Logical "0" from A_{IN} to D_{OUT}, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		230	400	ns
Propagation Delay to a Logical "1" from A_{IN} to D_{OUT}, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		210	400	ns
Maximum Clock Frequency		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ	6	15		MHz
Minimum Clock Pulse Width		V_{CC} = 5 0V, T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		60	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

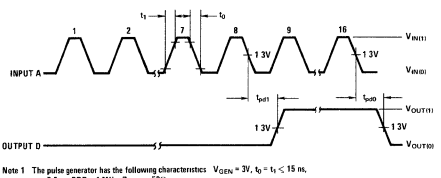
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L93, DM76L93 and across the 0°C to 70°C range for the DM74L93,DM86L93. All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

ac test circuit

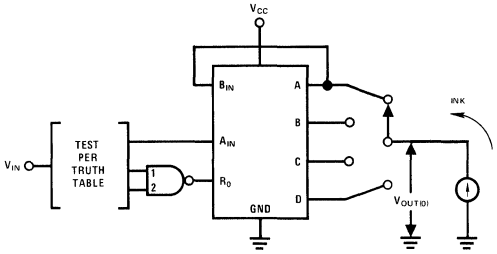


switching time waveforms

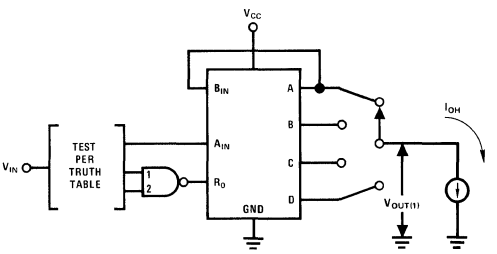


Note 1 The pulse generator has the following characteristics V_{GEN} = 3V, t_0 = t_1 ≤ 15 ns, t_0 = 0 5 t_1 PRR = 1 MHz, Z_{OUT} = 50Ω
Note 2 All diodes are 1N3064 or equivalent
Note 3 C_L includes probe and jig capacitance
Note 4 $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
Note 5 Voltage values are with respect to ground terminal

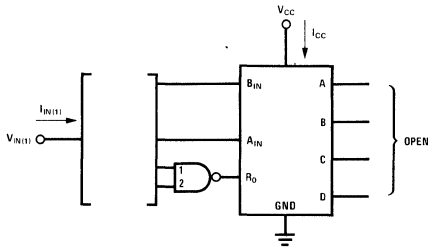
parameter measurement information



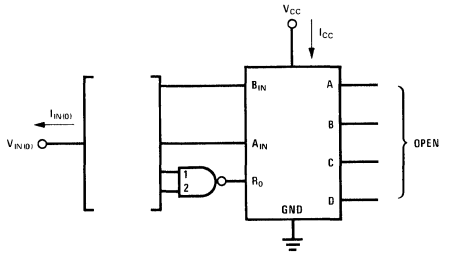
Note 1 Each output is tested in the logical "0" state



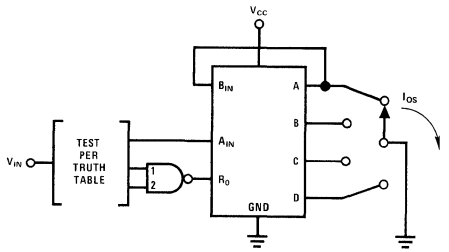
Note 1 Each output is tested in the logical "1" state



Note 1 Each input is tested separately
Note 2 When testing $R_{O(1)}$ ground $R_{O(2)}$
Note 3 When testing $R_{O(2)}$ ground $R_{O(1)}$
Note 4 When testing I_{CC} all inputs and outputs are open



Note 1 Each input is tested separately
Note 2 When testing $R_{O(1)}$ apply 4.5V to $R_{O(2)}$
Note 3 When testing $R_{O(2)}$ apply 4.5V to $R_{O(1)}$



Note 1 Each output is tested in the logical "1" state

truth table (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES 1 Output A connected to input B
2 To reset all outputs to logical "0" both $R_{O(1)}$ and $R_{O(2)}$ Inputs must be at a logical "1"
3 Either (or both) reset inputs $R_{O(1)}$ and $R_{O(2)}$ must be at a logical "0" to count

Series 54L/74L

DM54L98/DM74L98(SN54L98/SN74L98)
4-bit data selector/storage register

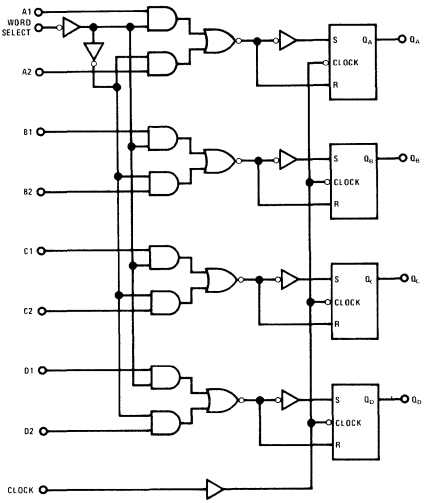
general description

The DM54L98/DM74L98 4-bit data selector/storage register is composed of four R-S flip flops with associated gating arranged to allow entry of data from one of two four-bit words. When the Word Select input is at the logical "0" level, word 1 is presented to the flip flop inputs. Conversely a logical "1" level allows word 2 to be selected. The selected word is entered into the flip flops during the negative-going transition of the clock.

features

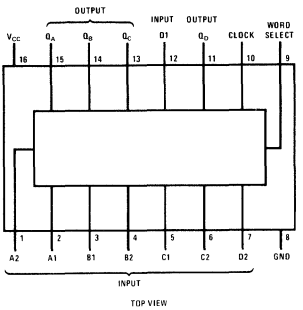
- 30 mW typical power dissipation
- 12 MHz typical clock frequency
- Fan-out to two standard 74 Series loads

block diagram

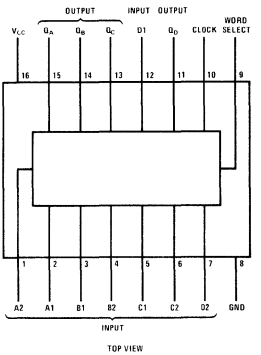


connection diagrams

Dual-In-Line Package



Flat Package



absolute maximum ratings

Supply Voltage	8.0V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range DM54L98	−55°C to +125°C
DM74L98	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L98 / DM74L98	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0	1.3		V
Logical "0" Input Voltage	DM54L98 / DM74L98	V_{CC} = 4.5V / V_{CC} = 4.75V		1.3	0.7	V
Logical "1" Output Voltage	DM54L98 / DM74L98	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = −200 μA, All Data Inputs = 2V	2.4	2.8		V
Logical "0" Output Voltage	DM54L98 / DM74L98	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = 2 mA, All Data Inputs = 0.7V I_{OUT} = 3.2 mA		0.15	0.3 0.4	V V
Logical "1" Input Current	DM54L98 / DM74L98	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V V_{IN} = 2.4V, Any Input			10	μA
	DM54L98 / DM74L98	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 5.5V V_{IN} = 5.5V, Any Input			100	μA
Logical "0" Input Current	DM54L98 / DM74L98	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 0.3V V_{IN} = 0.3V, Any Input			−0.18	mA
Output Short Circuit Current (Note 3)	DM54L98 / DM74L98	V_{CC} = 5.5V / V_{CC} = 5.25V	Data Inputs = 2V V_{OUT} = 0V	−3	−9	−15	mA
Supply Current I_{CC} Max	DM54L98 / DM74L98	V_{CC} = 5.5V / V_{CC} = 5.25V			6.0	8.0	mA
Propagation Delay to a Logical "0" from Clock to Any Out, t_{pd0}		V_{CC} = 5.0V T_A = 25°C			65	100	ns
Propagation Delay to a Logical "1" from Clock to Any Out, t_{pd1}		V_{CC} = 5.0V T_A = 25°C			40	80	ns
Maximum Clock Frequency		V_{CC} = 5.0V T_A = 25°C		6	12		MHz
Minimum Pulse Width on Clock		V_{CC} = 5.0V T_A = 25°C		100	65		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L98 and across the 0°C to 70°C range for the DM74L98. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

Series 54L/74L

DM54L154A/DM74L154A (SN54L154A/SN74L154A)
low power 4-line to 16-line decoder/demultiplexer

general description

The DM54L154A/DM74L154A is a one of sixteen decoder utilizing a true Series 54L/74L technology providing a full factor-of-ten power saving over conventional Series 54/74. The device is provided with two control inputs, both of which must be in the logical "0" state for normal operation. If either control input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

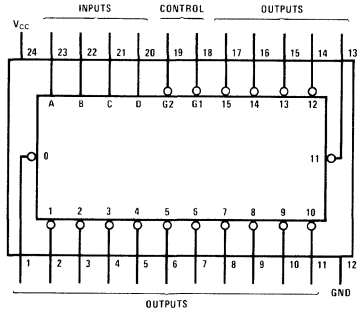
To use the product as a demultiplexer, one of the control inputs serves as the data input terminal, while the other control input must be maintained in the logical "0" state. The information will then be transmitted to the selected output, as determined by the 4-line input address.

features

- 20 mW typical power dissipation
- 55 ns typical propagation delay
- Pin compatible with SN54154/SN74154

connection diagram

Dual-In-Line Package



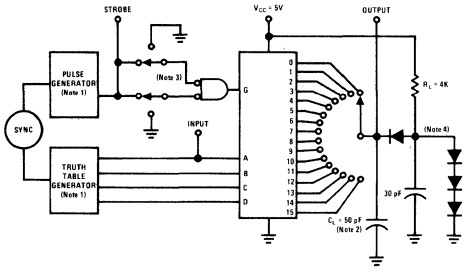
TOP VIEW

truth table

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high, L = low, X = don't care

ac test circuit



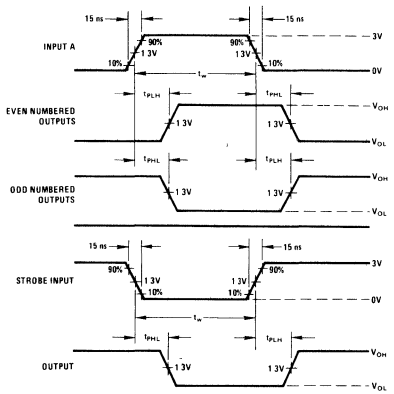
NOTE 1 The truth table generator and the pulse generator have the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$, t_w = 100 ns

NOTE 2 C_L includes probe and jig capacitance

NOTE 3 When measuring select input to output times the strobe inputs are grounded. When measuring strobe input to output times, the untested strobe input is grounded. Select inputs determine output under test through truth table generator.

NOTE 4 All diodes are 1N3064 or equivalent

switching time waveforms



absolute maximum ratings (Note 1)

Supply Voltage	+8V
Input Voltage	+5.5V
Output Voltage	+5.5V
Operating Temperature Range DM54L154A	−55°C to +125°C
DM74L154A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L154	V_{CC} = 4 5V		2 0			V
	DM74L154	V_{CC} = 4 75V					
Logical "0" Input Voltage	DM54L154	V_{CC} = 4 5V				0 7	V
	DM74L154	V_{CC} = 4 75V					
Logical "1" Output Voltage	DM54L154	V_{CC} = 4 5V	I_{OUT} = −200 μA	2 4	2 8		V
	DM74L154	V_{CC} = 4 75V					
Logical "0" Output Voltage	DM54L154	V_{CC} = 4 5V	I_{OUT} = 2 mA		0 15	0 30	V
	DM74L154	V_{CC} = 4 75V	I_{OUT} = 3 2 mA		0 20	0 40	V
Logical "1" Input Current	DM54L154	V_{CC} = 5 5V	V_{IN} = 2 4V			10	μA
	DM74L154	V_{CC} = 5 25V					
	DM54L154	V_{CC} = 5 5V	V_{IN} = 5 5V			100	μA
	DM74L154	V_{CC} = 5 25V					
Logical "0" Input Current	DM54L154	V_{CC} = 5 5V	V_{IN} = 0 3V		−0.11	−0.18	mA
	DM74L154	V_{CC} = 5 25V					
Output Short Circuit Current (Note 3)	DM54L154	V_{CC} = 5 5V	V_{OUT} = 0V	−3	−9	−15	mA
	DM74L154	V_{CC} = 5 25V					
I_{CC}	DM54L154	V_{CC} = 5.5V			4.8	6 0	mA
	DM74L154	V_{CC} = 5 25V					
Propagation Delay to a Logical "0" from any Input to any Output, t_{pd0}		V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		75	150	ns
Propagation Delay to a Logical "0" from G1 or G2 to any Output, t_{pd0}		V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		55	110	ns
Propagation Delay to a Logical "1" from any Input to any Output, t_{pd1}		V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		35	70	ns
Propagation Delay to a Logical "1" from G1 or G2 to any Output, t_{pd1}		V_{CC} = 5 0V T_A = 25°C	C_L = 50 pF, R_L = 4 kΩ		35	70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L154 and across the 0°C to 70°C range for the DM74L154 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

Series 54L/74L

DM54L165A/DM74L165A low power parallel-in serial-out 8-bit shift register

general description

The DM54L165A/DM74L165A utilizes Series 54L/74L compatible low-power TTL circuitry to provide an 8 bit parallel-in serial-out shift register. The device features internal gating for clock inhibit, parallel load control, and both Q & $\overline{Q}$ outputs are available from the last flip flop for added flexibility.

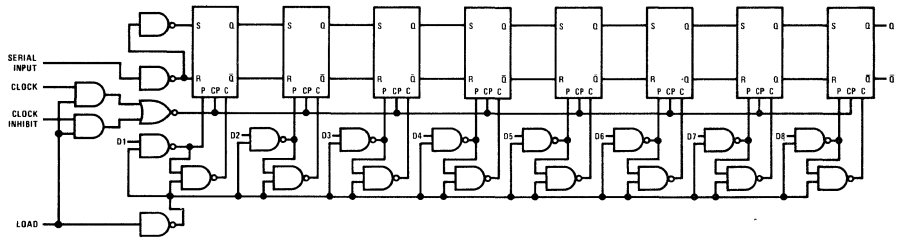
The clock inhibit must be a logical "0" for clocking to occur. A "1" on the clock inhibit line disables the clock. The function of these two inputs is completely interchangeable and they may be switched to facilitate die layout.

Clocking occurs on the positive-going transition of the clock. Data D_1 thru D_8 will be entered on the negative-going transition of the load input.

features

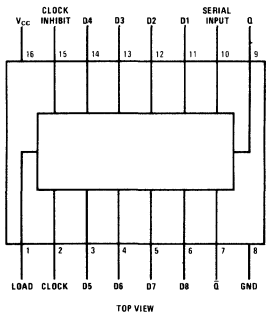
- Series 54L/74L compatible — true 1/10 -power technology
- Pin compatible with DM7590/DM8590 and SN54165/SN74165
- Typical power dissipation 30 mW
- Typical shift frequency 14 MHz

logic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

SERIAL IN	DATA IN	CLK	CLK INH	LOAD	FUNCTION
X	X	X	1	1	Do Nothing
X	X	1	X	1	Do Nothing
1	X	CP	0	1	Shift "1"s
0	X	CP	0	1	Shift "0"s
1	X	0	CP	1	Shift "1"s
0	X	0	CP	1	Shift "0"s
X	1	X	X	0	Load "1" Asynchronously
X	0	X	X	0	Load "0" Asynchronously

absolute maximum ratings (Note 1)

Supply Voltage		+8 0V
Input Voltage		+5 5V
Output Voltage		+5.5V
Operating Temperature Range	DM54L165A	−55°C to +125°C
	DM74L165A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54L165A	V_{CC} = 4 5V		2 0	1 3		V
	DM74L165A	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM54L165A	V_{CC} = 4.5V			1 3	0 7	V
	DM74L165A	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM54L165A	V_{CC} = 4.5V	I_{OUT} = −200 μA	2.4	2 8		V
	DM74L165A	V_{CC} = 4 75V					
Logical "0" Output Voltage	DM54L165A	V_{CC} = 4 5V	I_{OUT} = 2 mA		0 15	0 3	V
	DM74L165A	V_{CC} = 4 75V	I_{OUT} = 3 2 mA		0 20	0 4	V
Logical "1" Input Current	DM54L165A	V_{CC} = 5 5V	V_{IN} = 2 4V			10	μA
	DM74L165A	V_{CC} = 5 25V	V_{IN} = 5 5V			100	μA
Logical "0" Input Current	DM54L165A	V_{CC} = 5.5V	V_{IN} = 0 3V			−0 18	mA
	DM74L165A	V_{CC} = 5 25V					
Output Short Circuit Current (Note 3)	DM54L165A	V_{CC} = 5 5V	V_{OUT} = 0V	−3	−9	−15	mA
	DM74L165A	V_{CC} = 5.25V					
Supply Current I_{CC} max	DM54L165A	V_{CC} = 5 5V				9.5	mA
	DM74L165A	V_{CC} = 5.25V					
Propagation Delay to a Logical "0" from Clock or Clock Inhibit to Q or $\overline{Q}$, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		50	100	ns
Propagation Delay to a Logical "0" from Load to Q or $\overline{Q}$, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		62	124	ns
Propagation Delay to a Logical "1" from Clock or Clock Inhibit to Q or $\overline{Q}$, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		35	70	ns
Propagation Delay to a Logical "1" from Load to Q or $\overline{Q}$, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		44	88	ns
Maximum Clock Frequency		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF	6	14		MHz
Minimum Clock Pulse Width		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF			100	ns
Minimum Load Pulse Width						100	ns
t_{SETUP} Minimum Setup Time for Input Data (Load)		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		22	44	ns
t_{HOLD} Minimum Hold Time for Parallel Input Data (Load)		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		0	0	ns
t_{SETUP} (Clock) Minimum Setup Time for Serial Data		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		22	44	ns
t_{HOLD} (Clock) Minimum Hold Time for Serial Data		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		0	0	ns
Propagation Delay to Logical "1" from Data in to Q or $\overline{Q}$, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		56	112	ns
Propagation Delay to Logical "0" from Data in to Q or $\overline{Q}$, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		33	66	ns

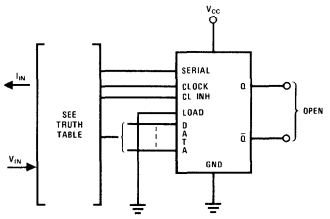
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L165A and across the 0°C to 70°C range for the DM74L165A All typicals are given for V_{CC} = 5 0V and T_A = 25°C

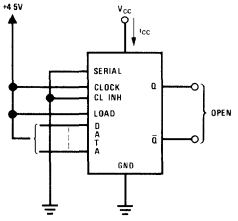
Note 3: Only one output at a time should be shorted.

parameter measurement information

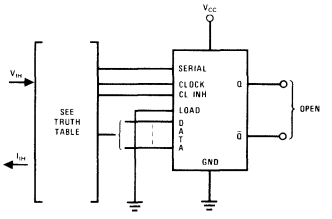
$V_{IN}(0)$, $I_{IN}(0)$



I_{CC}

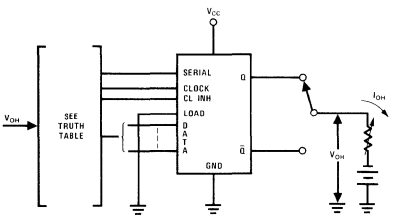


I_{IH}, I_{IL}

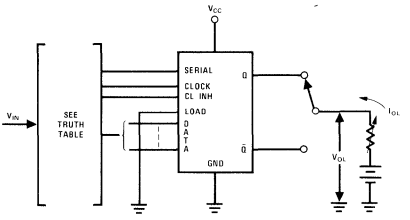


Note 1 Each input tested separately V_{IH}, I_{IH}

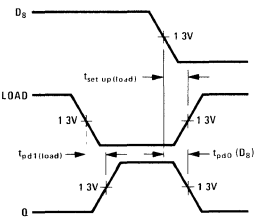
V_{OH}

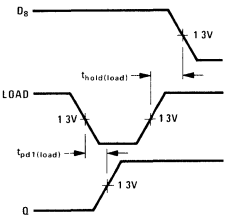


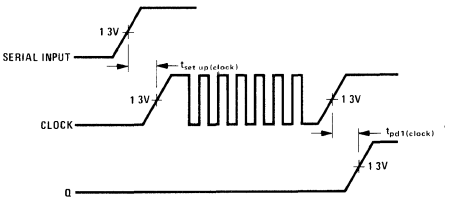
V_{OL}

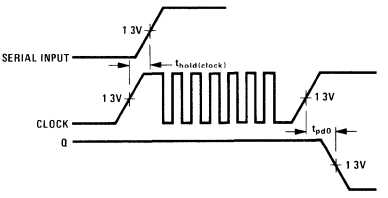


switching time waveforms









3

Series 54L/74L

DM54L192/DM74L192(SN54L192/SN74L192) up-down decade counter

DM54L193/DM74L193(SN54L193/SN74L193) up-down binary counter

general description

The DM54L192/DM74L192 and DM54L193/DM74L193 are up-down decade and up-down binary counters respectively. Separate clock inputs determine up or down counting. The unused clock input must be tied high when not in use.

Asynchronous clear and load inputs with clear override provide for parallel data entry. Clear overrides the load as far as asynchronous data entry is concerned. Carry and borrow outputs are controlled synchronously. Normal synchronous operation requires clear = "0" and load = 1.

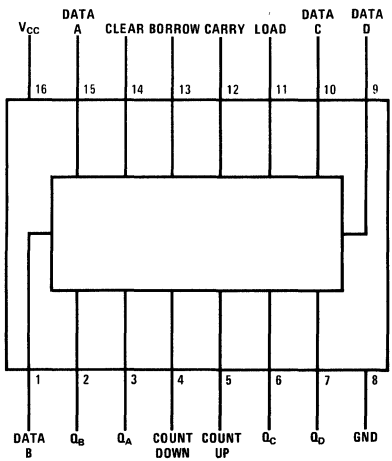
The counters can drive two standard TTL loads over the commercial temperature range and 10 and 20 low power TTL loads in the "0" and "1" states respectively over the military temperature range.

features

- Series 54L/74L compatible
- 40 mW typical power dissipation
- 50 ns typical propagation delay

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54L192, DM54L193	4.5	5 5	V
DM74L192, DM74L193	4.75	5.25	V
Temperature (T_A)			
DM54L192, DM54L193	−55	+125	°C
DM74L192, DM74L193	0	70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		V_{CC} = Min		2 0	1 3		V
Logical "0" Input Voltage		V_{CC} = Min			1 3	0 7	V
Logical "1" Output Voltage		V_{CC} = Min	I_{OUT} = −200 μA	2 4	2 8		V
Logical "0" Output Voltage	DM54L192,DM54L193	V_{CC} = 4 5V	I_{OUT} = 2 mA		0 15	0 3	V
	DM74L192,DM74L193	V_{CC} = 4 75V	I_{OUT} = 3 2 mA		0 20	0 4	V
Logical "1" Input Current		V_{CC} = Max, V_{IN} = 2 4V			<1	10	μA
		V_{CC} = Max, V_{IN} = 5 5V			<1	100	μA
Logical "0" Input Current		V_{CC} = Max, V_{IN} = 0 3V			−0 10	−0 18	mA
Output Short Circuit Current (Note 3)		V_{CC} = Max, V_{OUT} = 0V		−3	−9	−15	mA
Supply Current I_{CC} Max	DM54L192/DM74L192	V_{CC} = Max			8 0	13	mA
	DM54L193/DM74L193	V_{CC} = Max			7 5	12 5	mA
Propagation Delay to a Logical "0" from Either Count Input to Output, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		75	150	ns
Propagation Delay to a Logical "0" from Count Up to Carry, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		60	120	ns
Propagation Delay to a Logical "1" from Either Count Input to Output, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		45	90	ns
Propagation Delay to a Logical "1" from Count Up to Carry, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		30	60	ns
Maximum Clock Frequency		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF	6	12		MHz
Propagation Delay to Logical "1" from Count Down to Borrow, t_{pd1}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		30	60	ns
Propagation Delay to Logical "0" from Count Down to Borrow, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		50	100	ns
t_{SETUP} — Minimum Input Setup		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		5	30	ns
Minimum Clock Pulse Width		V_{CC} = 5 0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		35	70	ns

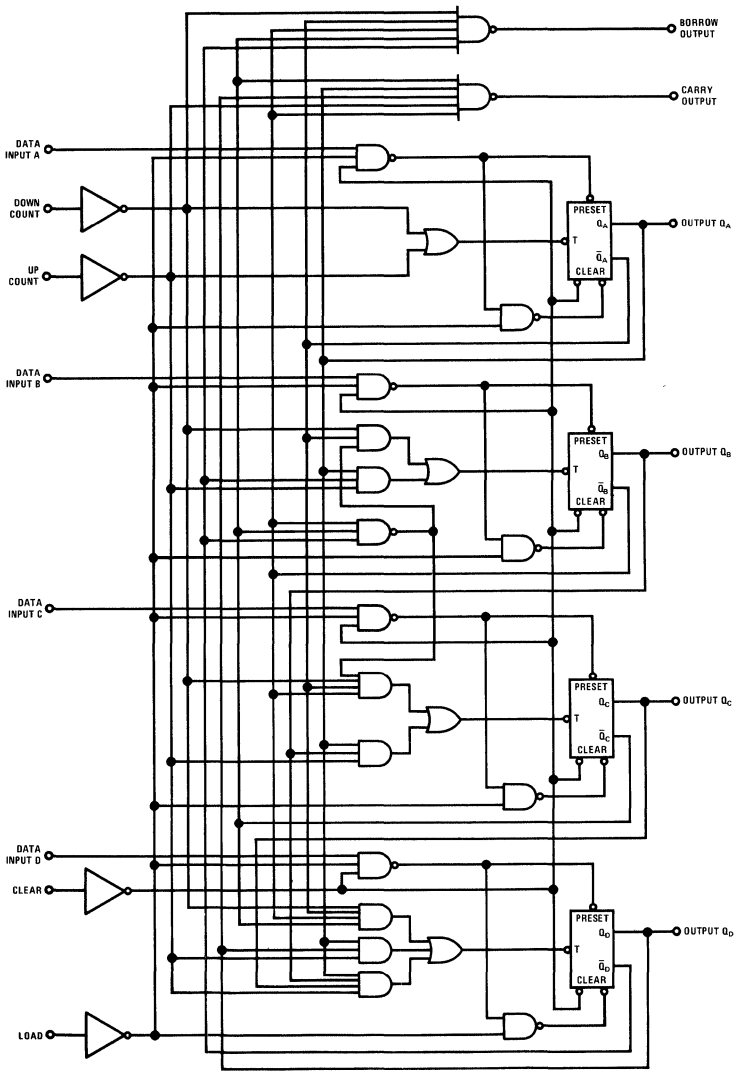
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L192, DM54L193 and across the 0°C to 70°C range for the DM74L192, DM74L193 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

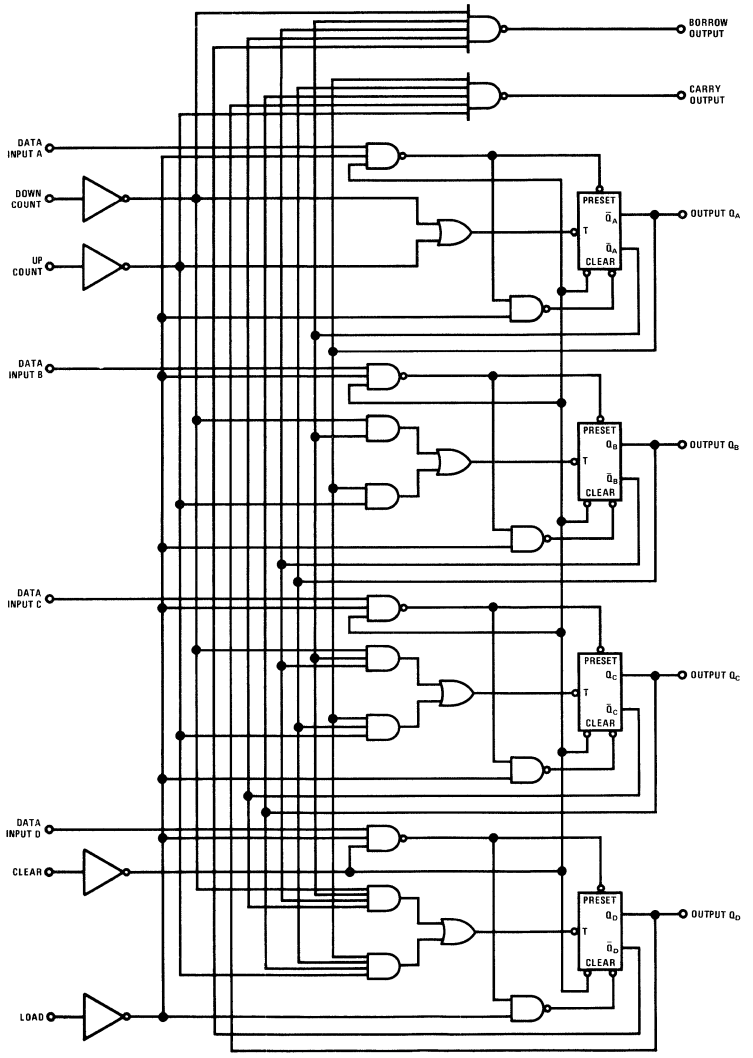
logic diagrams

DM54L192/DM74L192

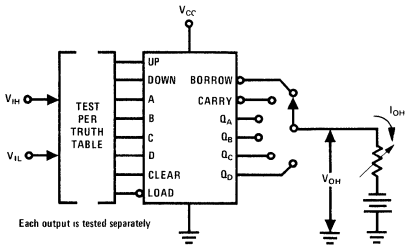


logic diagrams (cont.)

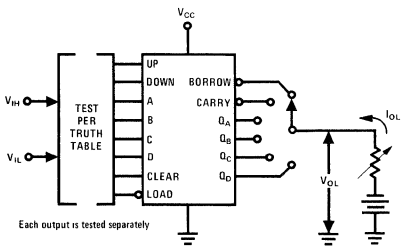
DM54L193/DM74L193



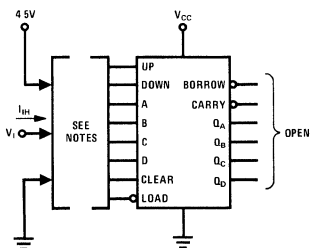
dc test circuits



V_{IH}, V_{IL}, V_{OH}

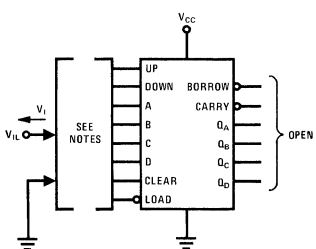


V_{IH}, V_{IL}, V_{OL}



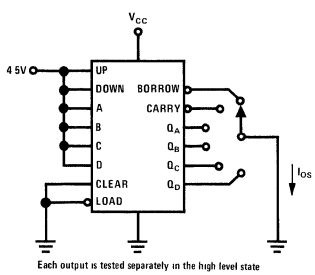
Note 1 Each input is tested separately
Note 2 Apply V_I to input under test and ground other inputs except when testing data inputs, apply 4.5V to clear and load inputs

I_{IH}

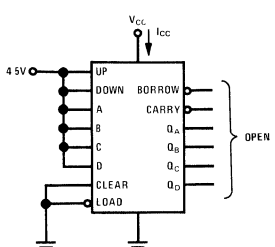


Note 1 Each input is tested separately
Note 2 Apply V_I to input under test and ground other inputs

I_{IL}



I_{OS}

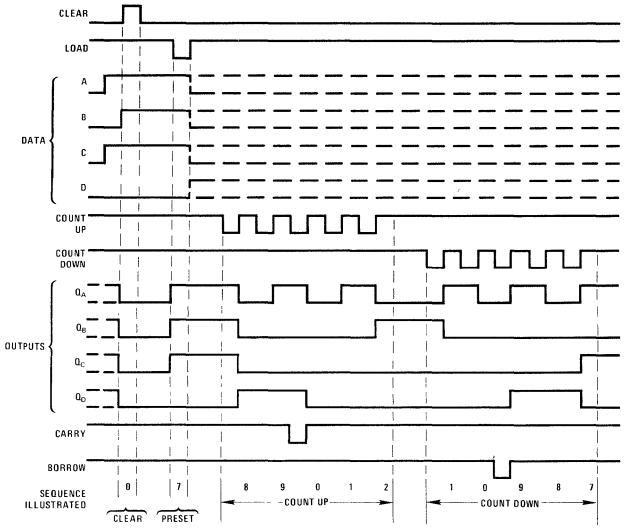


I_{CC}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

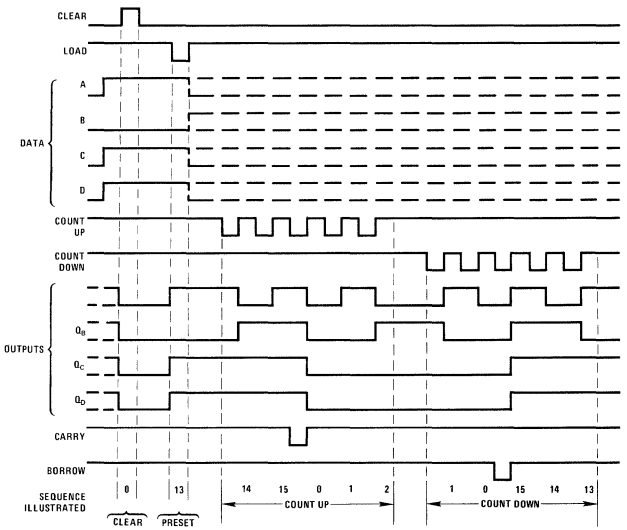
switching time waveforms

1 Clear outputs to zero
2 Load (preset to BCD seven
3 Count up to eight, nine, carry, zero, one and two
4 Count down to one, zero, borrow, nine, eight, and seven



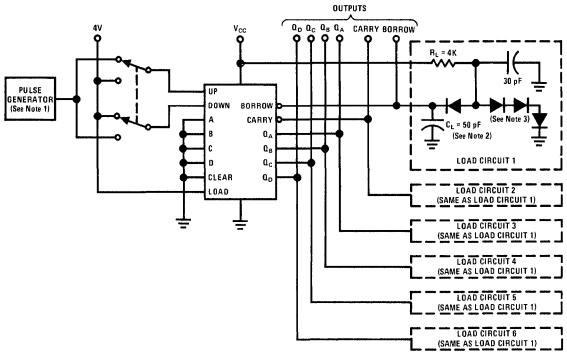
DM54L192/DM74L192

Illustrated below is the following sequence
1 Clear outputs to zero
2 Load (preset) to BCD thirteen
3 Count up to fourteen, fifteen, carry, zero, one, and two
4 Count down to one, zero, borrow, fifteen, fourteen, and thirteen



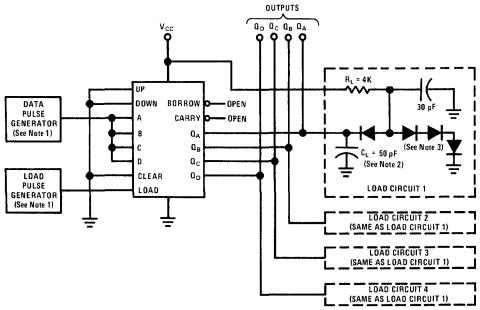
DM54L193/DM74L193

switching characteristics



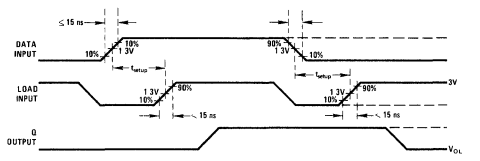
Note 1 The pulse generators have the following characteristics $Z_{OUT} \approx 50\Omega$, for the data pulse generator, PRR = 500 kHz, duty cycle = 50%, for the load pulse generator, PRR = 1 MHz, duty cycle = 50%
Note 2 C_L includes probe and jig capacitance
Note 3 All diodes are 1N3064, or equivalent

Test Circuit 1

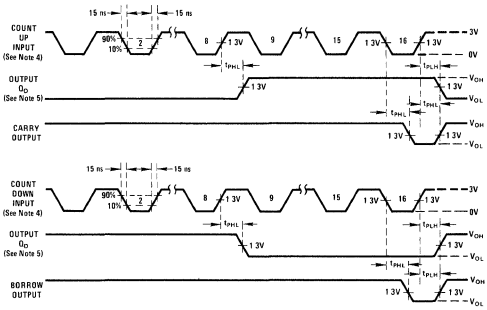


Note 1 The pulse generator has the following characteristics PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$, duty cycle = 50%
Note 2 C_L includes probe and jig capacitance
Note 3 All diodes are 1N3064
Note 4 Count up and count down pulses shown are for the SN54193/SN74193 binary counters Count cycle for SN54192 decade counter is 1 through 10
Note 5 Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing

Test Circuit 2



Voltage Waveforms 1



Voltage Waveforms 2

Series 54L/74L

DM71L22/DM81L22, DM71L23/DM81L23 quad 2-input multiplexers

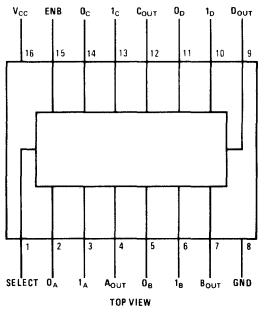
general description

The DM71L22/DM81L22 and DM71L23/DM81L23 are quad 2-input multiplexers which select one of two word inputs, and outputs the data when enabled. The enable input can be used to synchronize data transfer and forces the output to the "0" state (DM71L22/DM81L22) or high impedance state (DM71L23/DM81L23) when enable = "1". The advantage of the DM71L23/DM81L23 is that it makes "wire-oring" of the outputs possible.

Each buffered output can fanout to two standard TTL unit loads over the commercial temperature range, and 10 54L/74L unit loads in the low state over the Mil temperature range. In addition these devices can fanout to 20 54L/74L unit loads with the output in the high state ("1").

connection diagram

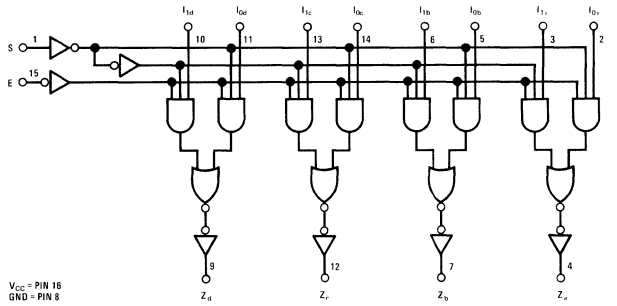
Dual-In-Line and Flat Packages



TOP VIEW

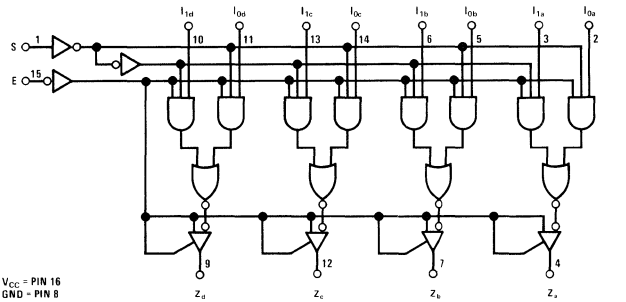
truth tables and logic diagrams

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\bar{E}$	S	ϕ_X	1_X	Z_X
1	X	X	X	ϕ
ϕ	1	X	ϕ	ϕ
ϕ	1	X	1	1
ϕ	ϕ	ϕ	X	ϕ
ϕ	ϕ	1	X	1



DM71L22/DM81L22

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\bar{E}$	S	ϕ_X	1_X	Z_X
1	X	X	X	HI Z
ϕ	1	X	ϕ	ϕ
ϕ	1	X	1	1
ϕ	ϕ	ϕ	X	ϕ
ϕ	ϕ	1	X	1



DM71L23/DM81L23

absolute maximum ratings (Note 1)

Supply Voltage	+8 0V
Input Voltage	+5 5V
Output Voltage	+5 5V
Operating Temperature Range	
DM71L22, DM71L23	−55°C to +125°C
DM81L22, DM81L23	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM71L22, DM71L23	4 5	5 5	V
DM81L22, DM81L23	4 75	5 25	V
Temperature (T_A)			
DM71L22, DM71L23	−55	+125	°C
DM81L22, DM81L23	0	70	°C

electrical characteristics (Note 2)

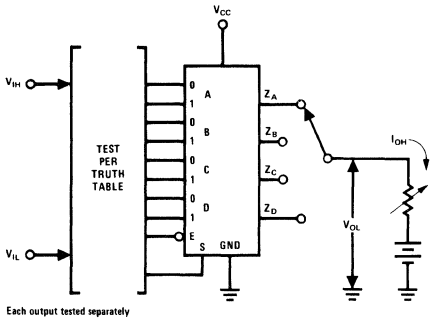
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0	1 3		V
Logical "0" Input Voltage	V_{CC} = Min		1 3	0 7	V
Logical "1" Output Voltage	I_{OH} = −200 μA, V_{CC} = Min	2 4	2 8		V
Logical "0" Output Voltage	Mil I_{OUT} = 2 mA, V_{CC} = Min Comm I_{OUT} = 3 2 mA		0 15 0 20	0 30 0 40	V V
Third State Output Current	DM71L23/DM81L23 Only, V_{CC} = Max	−40		+20	μA
Logical "1" Input Current	V_{IN} = 2 4V, V_{CC} = Max			10	μA
	V_{IN} = 5 5V, V_{CC} = Max			100	μA
Logical "0" Input Current	V_{IN} = 0 3V, V_{CC} = Max			−0 18	mA
Output Short Circuit Current (Note 3)	V_{OUT} = 0V, V_{CC} = Max	−3	−9	−15	mA
$I_{CC\ MAX}$ DM71L22/DM81L22	See DC Test Ckts, V_{CC} = Max			4	mA
$I_{CC\ MAX}$ DM71L23/DM81L23	See DC Test Ckts, V_{CC} = Max			5 3	mA
Input Clamp Voltage					
Output V_{CC} Clamp Voltage					
Output Ground Clamp Voltage					
Propagation Delay to a Logical "0" from ϕ or 1 to Z_{OUT}, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF	20	40	80	ns
Propagation Delay to a Logical "0" from Select to Z_{OUT}, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF	25	50	100	ns
Propagation Delay to a Logical "1" from ϕ or 1 to Z_{OUT}, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF	20	40	80	ns
Propagation Delay to a Logical "1" from Select to Z_{OUT}, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF	35	70	140	ns
Delay from Enable to Output from Logical "1" to High Impedance State	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF DM71L23/DM81L23 Only	15	30	60	ns
Delay from Enable to Output from Logical "0" to High Impedance State	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF DM71L23/DM81L23 Only	35	75	150	ns
Delay from Enable to Output from High Impedance State to Logical "1"	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF DM71L23/DM81L23 Only	15	30	60	ns
Delay from Enable to Output from High Impedance State to Logical "0"	V_{CC} = 5 0V, T_A = 25°C, R_L = 4 kΩ, C_L = 50 pF DM71L23/DM81L23 Only	20	35	70	ns
Propagation Delay to a Logical "1" from Enable to Z_{OUT}, t_{pd1}	DM71L22/DM81L22 Only	30	60	120	ns
Propagation Delay to a Logical "0" from Enable to Z_{OUT}, t_{pd0}	DM71L22/DM81L22 Only	30	60	120	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM71L22, DM71L23 and across the 0°C to 70°C range for the DM81L22, DM81L23 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

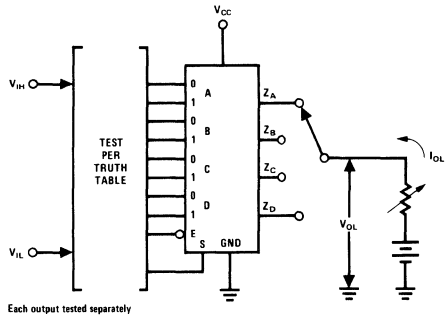
Note 3: Only one output at a time should be shorted

DM71L22, DM71L23 dc test circuits



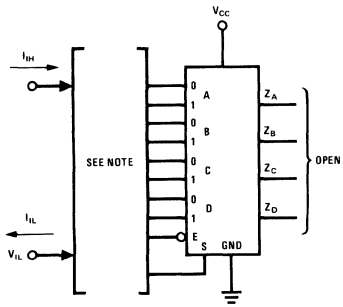
Each output tested separately

V_{IH}, V_{IL}, V_{OH}



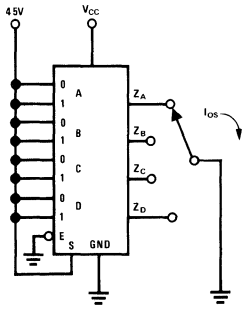
Each output tested separately

V_{IH}, V_{IL}, V_{OL}



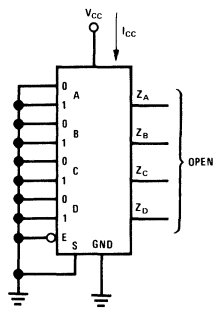
NOTE For I_{IH} on 0/1, take enable input to 4 5V and 1/0 to 0 volts
For I_{IL} on 0/1, ground enable and take select input to 0V/4 5V
Test I_{IH} & I_{IL} on select & enable inputs separately with no special conditions on other inputs

I_{IH}, I_{IL}



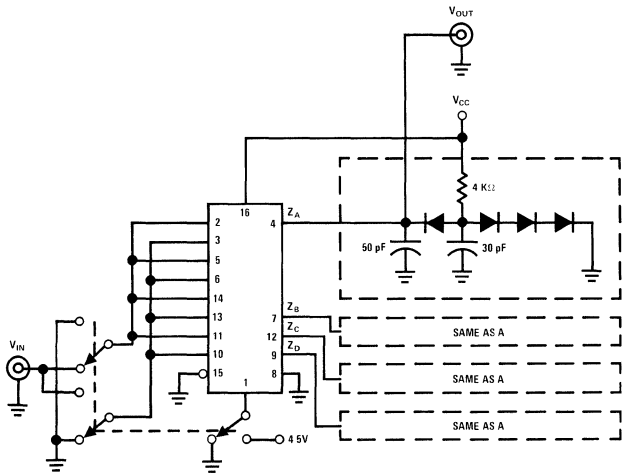
Each output tested separately

I_{OS}

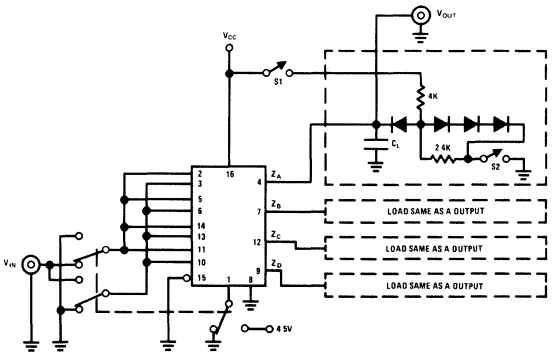


I_{CC}

DM71L22 ac test setup

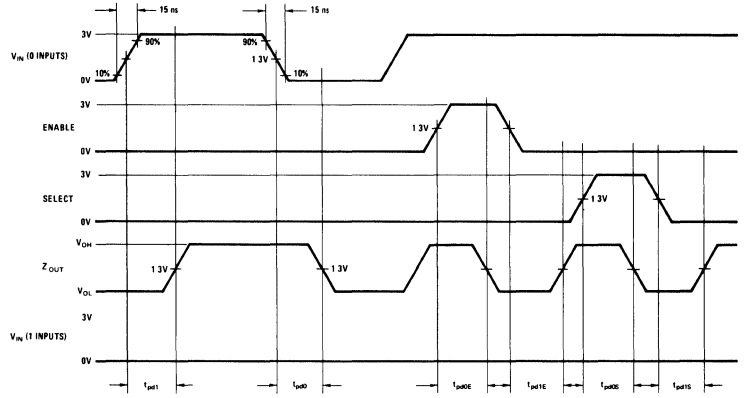


DM71L23 ac test setup



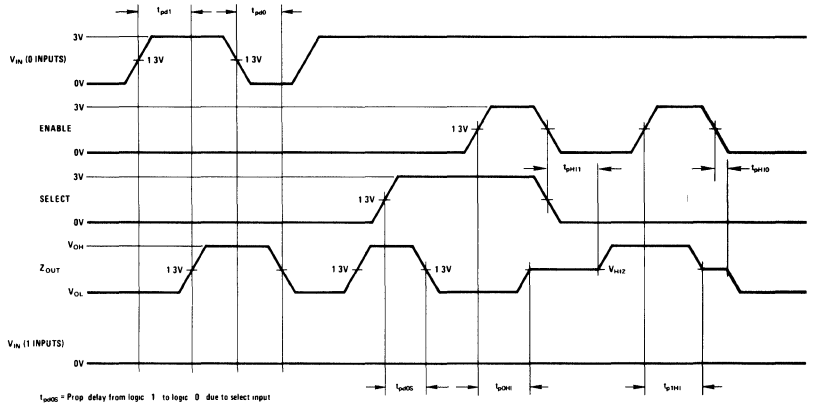
MEASURE FROM	MEASURE TO	S1	S1	C_L	MEASURE TO
'1	0''	Closed	Closed	50 pF	1.3V Level
0 '	1 '	Closed	Closed	50 pF	1.3V Level
0 '	OFF	Closed	Closed	5 pF	0.5V Change
'1	OFF	Closed	Closed	5 pF	0.5V Change
OFF	'0	Closed	Open	50 pF	1.3V Level
OFF	1	Open	Closed	50 pF	1.3V Level

DM71L22 ac switching characteristics



t_{pd0E} = Prop delay from logic '1' to logic "0" due to enable input
t_{pd1E} = Prop delay from logic '0' to logic '1' due to enable input
t_{pd0S} = Prop delay from logic '1' to logic '0' due to select input
t_{pd1S} = Prop delay from logic '0' to logic '1' due to select input

DM71L23 ac switching characteristics



t_{pd0S} = Prop delay from logic 1 to logic 0 due to select input
t_{pDHI} = Prop delay (from logic '0') to Hi z state due to enable input
t_{pTHI} = Prop delay (from logic '1') to Hi z state due to enable input
t_{pHH1} = Prop delay from Hi z state to a logic 1 due to enable input
t_{pHH0} = Prop delay from Hi z state to a logic 0 due to enable input

Series 54L/74L

DM75L11/DM85L11 TTL dual gated D flip flop

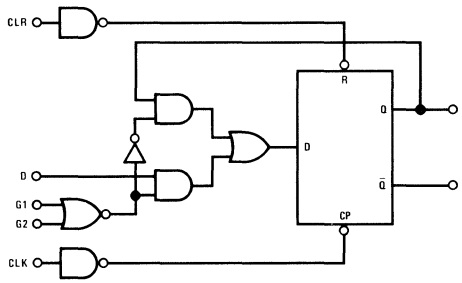
general description

The DM75L11/DM85L11 is a low power TTL dual gated D flip flop utilizing two gate inputs Both gate inputs must be low to enable data transfer to the Q and $\overline{Q}$ outputs If either gate input is high the data on the Q and $\overline{Q}$ outputs is constant

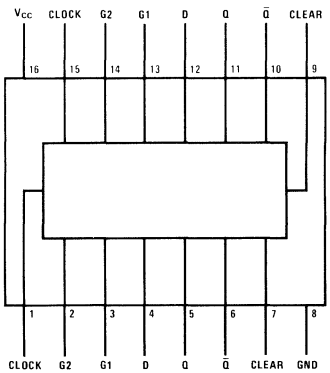
features

- Positive edge triggered, buffered clock
- 18 mW typical power dissipation
- 70 ns typical propagation delay
- Pin compatible with STD TTL DM7511/ DM8511

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

truth table

D	G_1	G_2	CLR	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	0	0	0	1
1	0	0	0	1	0
X	1	X	0	Q_n	$\overline{Q}_n$
X	X	1	0	Q_n	$\overline{Q}_n$
X	X	X	1	0	1*

*Asynchronous Transition

X = Irrelevant (Don't Care)

absolute maximum ratings (Note 1)

Supply Voltage	+8 0 V_{DC}
Input Voltage	+5 5 V_{DC}
Output Voltage	+5 5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75L11	4 5	5 5	V
DM85L11	4 75	5 25	V
Temperature (T_A)			
DM75L11	−55	+125	°C
DM85L11	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0	1 3		V
Logical "0" Input Voltage	V_{CC} = Min		1 3	0 7	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = -200μA	2 4	2 8		V
Logical "0" Output Voltage DM75L11	V_{CC} = Min, I_{OUT} = 2 0 mA		0 15	0 30	V
Logical "0" Output Voltage DM85L11	V_{CC} = Min, I_{OUT} = 3 2 mA		0 20	0 40	V
Logical "1" Input Current DM75L11 All Inputs	V_{CC} = Min, V_{IN} = 2 4V			10	μA
Logical "1" Input Current DM85L11 All Inputs	V_{CC} = Min, V_{IN} = V_{CC}			100	μA
Logical "0" Input Current All Inputs	V_{CC} = Max, V_{IN} = 0 3V		−100	−180	μA
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_{OUT} = 0V	−3	−9	−15	mA
Supply Current (Per Package)	V_{CC} = Max		3 5	4 9	mA
Propagation Delay to a Logical "0" from t_{PHL} Clock to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C Figure 1 Waveforms A		75	125	ns
Propagation Delay to a Logical "1" from t_{PLH} Clock to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C Figure 1 Waveforms A		55	95	ns
Propagation Delay to a Logical "0" from t_{PHL} Clear to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C Figure 2 Waveforms B		75	125	ns
Propagation Delay to a Logical "1" from t_{PLH} Clear to Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C Figure 2 Waveforms B		55	95	ns
Maximum Clock Frequency	V_{CC} = 5 0V, T_A = 25°C Figure 1 Waveforms A	6	9		MHz
Minimum Clear Pulse Width, $t_{W(CLEAR)}$	V_{CC} = 5 0V, T_A = 25°C Figure 2 Waveforms B		30	100	ns
Minimum Clock Pulse Width, $t_{W(CLOCK)}$	V_{CC} = 5 0V, T_A = 25°C Figure 1 Waveforms A		30	100	ns
Minimum Set-Up Time for Data Input, $t_{S(DATA)}$	V_{CC} = 5 0V, T_A = 25°C Figure 3 Waveforms C		40	80	ns
Minimum Hold Time $t_{H(DATA)}$ for Data Input	V_{CC} = 5 0V, T_A = 25°C Figure 3 Waveforms C		30	60	ns
Minimum Set-Up Time $t_{S(G)}$ for G_1 or G_2 Input	V_{CC} = 5 0V, T_A = 25°C Figure 4 Waveforms D		40	80	ns
Minimum Hold Time $t_{H(G)}$ for G_1 or G_2 Input	V_{CC} = 5.0V, T_A = 25°C Figure 4 Waveforms D		30	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

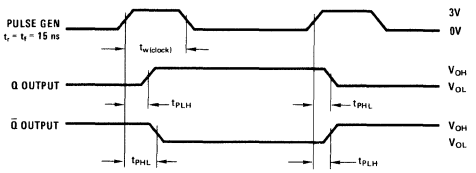
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75L11 and across the 0°C to 70°C range for the DM85L11 All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

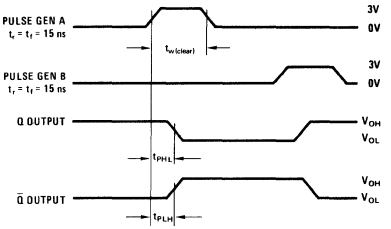
Note 4: Switching parameters guaranteed to change less than 50% over the full operating temperature range

switching time waveforms

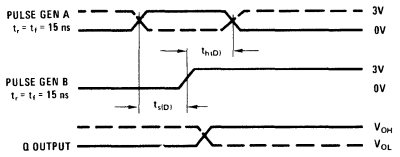
All times measured from 1.3V level



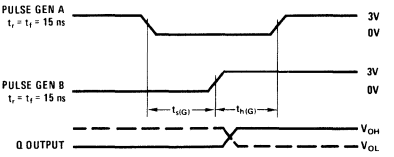
(a)



(b)



(c)



(d)

ac test circuits

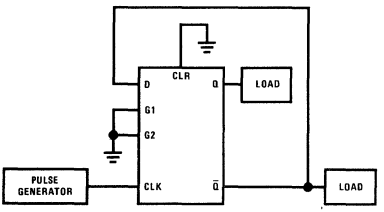


FIGURE 1. Use Waveforms A

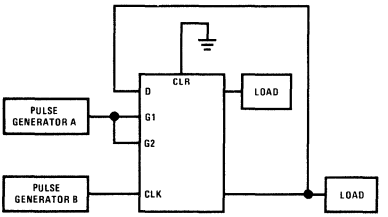


FIGURE 2. Use Waveforms B

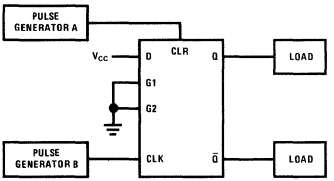


FIGURE 3. Use Waveforms C

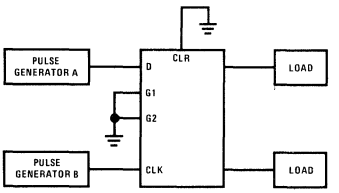


FIGURE 4. Use Waveforms D

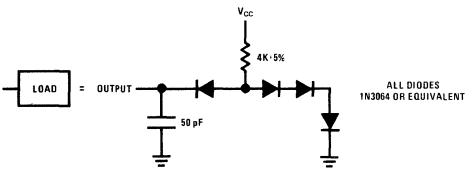


FIGURE 5.

Series 54L/74L

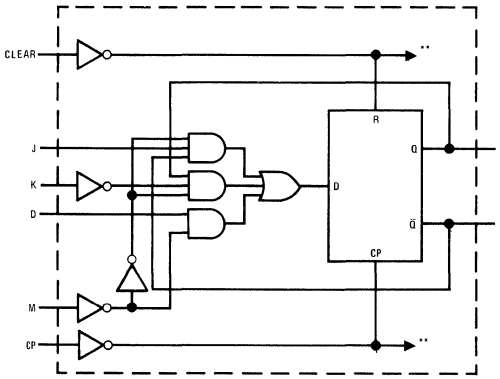
DM75L12/DM85L12 dual JK, D flip flop

general description

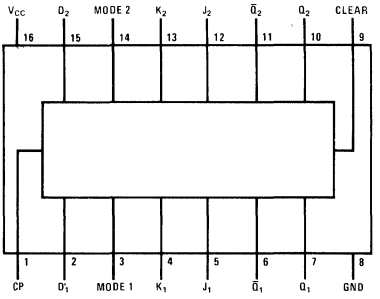
The DM75L12/DM85L12 is a dual JK, D flip flop with a common clock and common clear A mode control input on each flip flop determines the type of flip flop operation (Mode = "1" enables the JK mode, and mode = "0" enables the D mode.) The clear input is an asynchronous input which overrides all other inputs

Q and $\overline{Q}$ outputs are both provided on each flip flop. Typical propagation delays from clock to outputs are approximately equal to three low power TTL gate delays.

logic and connection diagrams



*ONLY LOGIC FOR ONE OF THE TWO FLIP FLOPS IS SHOWN
**CLOCK AND CLEAR ARE COMMON TO BOTH FLIP FLOPS



TOP VIEW

truth table

J	K	M	CLEAR	Q_{n+1}
0	0	1	0	Q_n
1	0	1	0	1
0	1	1	0	0
1	1	1	0	$\overline{Q}_n$
X	X	0	0	D
X	X	X	1	0*

*Asynchronous Transition

absolute maximum ratings (Note 1)

Supply Voltage	+8 0 V_{DC}
Input Voltage	+5.5 V_{DC}
Output Voltage	+5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75L12	4 5	5 5	V
DM85L12	4.75	5 25	V
Temperature (T_A)			
DM75L12	−55	+125	°C
DM85L12	0	70	°C

electrical characteristics (Note 2)

V_{CC} = 5.0V, T_A = 25°C, R_L = 4kΩ, C_L = 50 pF

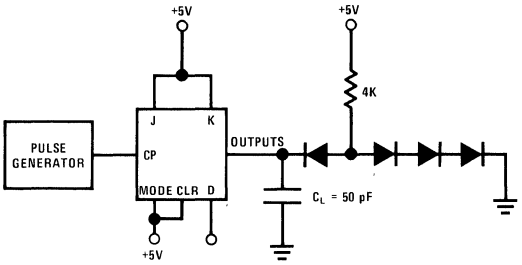
PARAMETER	CONDITIONS	WAVEFORM REF tΔ	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Max		2	1 3		V
Logical "0" Input Voltage	V_{CC} = Max			1 3	0 7	V
Logical "1" Output Voltage	I_{OUT} = -200μA, V_{CC} = Min		2 4	2 8		V
Logical "0" Output Voltage	Mil I_{OUT} = 2 mA, Com I_{OUT} = 3 2 mA, V_{CC} = Min			0 15 0 20	0 3 0 4	V V
Logical "1" Input Current	V_{IN} = 2 4V D, J, K, M, Inputs, CP, CLEAR V_{IN} = 5 5V V_{CC} = Max				10 100	μA μA
Logical "0" Input Current	V_{IN} = 0 3V, All Inputs V_{CC} = Max				−180	μA
Output Short Circuit Current (Note 3)	V_{OUT} = 0V, V_{CC} = Max		−3	−9	−15	mA
Supply Current − I_{CC} Max	M_1 = M_2 = CP = "0", All Other Inputs = "1" V_{CC} = Max				4 5	mA
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}		t_1		60	120	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}		t_2		35	70	ns
Propagation Delay to a Logical "0" from Clear to Output, t_{pd0}		t_{11}		57	114	ns
Maximum Clock Frequency			6	10		MHz
t_{SETUP} Minimum	JK Mode Data	t_3, t_4 t_7, t_{10} t_{12}, t_{13}		77 81 45	140 150 90	ns ns ns
t_{HOLD} Minimum	JK Mode Data	t_5, t_6 t_8, t_9 t_{14}, t_{15}		77 81 45	140 150 90	ns ns ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75L12 and across the 0°C to 70°C range for the DM85L12. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

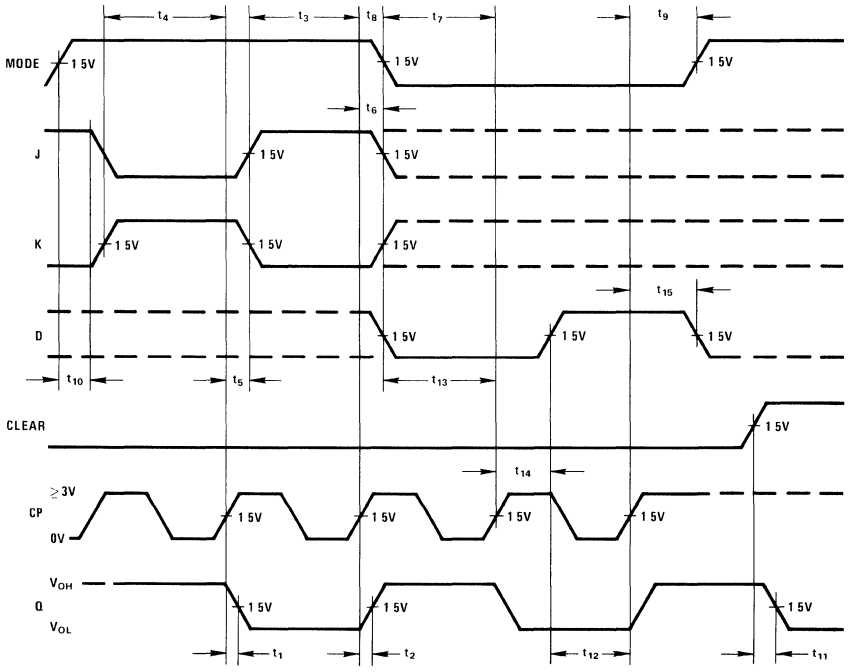
Note 3: Only one output at a time should be shorted

ac test circuit



ALL DIODES 1N916
C_L = INCLUDES PROBE AND JIG CAPACITANCE

switching time waveforms



Series 54L/74L

DM75L51/DM85L51 low power TRI-STATE® quad-D flip flop

general description

The DM75L51/DM85L51 is a TRI-STATE ® logic device which provides four D-type flip flops in one package which operate synchronously from a common clock

A unique three-state output allows the device to be used in bus-organized systems. The outputs can be directly wired to outputs of other DM75L51/DM85L51s without encountering the problems normally met with "collector-ORing" LP TTL circuits. This is accomplished by gating the normally low impedance logical "1" or logical "0" output into a high impedance state

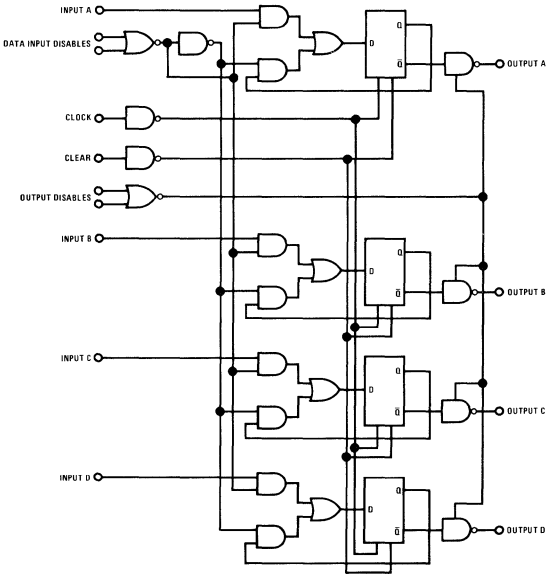
The DM75L51/DM85L51 is completely compatible with other Series 54L/74L devices

features

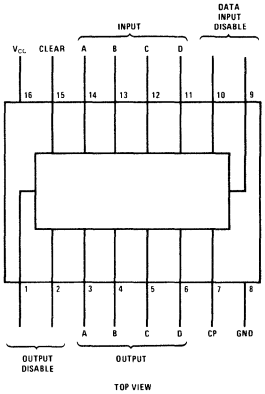
- Series 54L/74L compatible
- 50 ns typical propagation delay
- 30 mW typical power dissipation
- Outputs directly connectable for bus-line operation
- A "do-nothing" state accomplished without gating the clock
- Simple disable encoding

3

logic and connection diagrams



Dual-In-Line and Flat Package



truth table

(Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLES	D	OUTPUT
Logical 1 on 1 or both inputs	X	O_n
Logical 0 on both inputs	1	1
Logical "0" on both inputs	0	0

X = Don t Care

absolute maximum ratings (Note 1)

Supply Voltage	8 0V	Storage Temperature Range	−65°C to 150°C
Input Voltage	5 5V	Lead Temperature (Soldering, 10 sec)	300°C
Output Voltage	5 5V		
Operating Temperature Range DM75L51	−55°C to 125°C		
DM85L51	0°C to 70°C		

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM75L51	V_{CC} = 4 5V		2	1 3		V
	DM85L51	V_{CC} = 4 75V		2	1 3		V
Logical "0" Input Voltage	DM75L51	V_{CC} = 4 5V			1 3	0 7	V
	DM85L51	V_{CC} = 4 75V			1 3	0 7	V
Logical "1" Output Voltage	DM75L51	V_{CC} = 4 5V	I_{OUT} = −1 mA	2 4	2 7		V
	DM85L51	V_{CC} = 4 75V	I_{OUT} = −1 mA	2 4	2 7		V
Logical "0" Output Voltage	DM75L51	V_{CC} = 4 5V	I_{OUT} = 2 mA		0 15	0 3	V
	DM85L51	V_{CC} = 4 75V	I_{OUT} = 3 2 mA		0 2	0 4	V
Third State Output Current	DM75L51	V_{CC} = 5 5V	V_{OUT} = 2 4V			20	μA
	DM85L51	V_{CC} = 5 25V	V_{OUT} = 0.3V			−40	μA
Logical "1" Input Current	DM75L51	V_{CC} = 5 5V	V_{IN} = 2 4V		<1	10	μA
	DM85L51	V_{CC} = 5 25V	V_{IN} = 5 5V		<10	100	μA
Logical "0" Input Current	DM75L51	V_{CC} = 5 5V	V_{IN} = 0.3V		−120	−180	μA
	DM85L51	V_{CC} = 5 25V			−120	−180	μA
Output Short Circuit Current (Note 3)	DM75L51	V_{CC} = 5 5V	V_{OUT} = 0V	−3	−8	−15	mA
	DM85L51	V_{CC} = 5 25V		−3	−8	−15	mA
Supply Current - (each device) $I_{CC\,(max)}$	DM75L51	V_{CC} = 5 5V			5 5	9	mA
	DM85L51	V_{CC} = 5.25V					
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}		V_{CC} = 5 0V T_A = 25°C			77	120	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}		V_{CC} = 5 0V T_A = 25°C			39	70	ns
Propagation Delay from Clear to Output, t_{pdR}		V_{CC} = 5 0V T_A = 25°C			72	110	ns
Delay from Output Disable to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0V T_A = 25°C			18	50	ns
Delay from Output Disable to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V T_A = 25°C			32	75	ns
Delay from Output Disable to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5 0V T_A = 25°C			28	55	ns
Delay from Output Disable to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5 0V T_A = 25°C			35	60	ns
Maximum Clock Frequency		V_{CC} = 5 0V T_A = 25°C		6	15		MHz
Input Data Setup Time, t_{SDATA}		V_{CC} = 5 0V T_A = 25°C			+5 7	+10	ns
Input Data Hold Time, t_{HDATA}		V_{CC} = 5 0V T_A = 25°C		10	+2		ns
Input Disable Setup Time, $t_{S\,DIS}$		V_{CC} = 5 0V T_A = 25°C			33	45	ns
Input Disable Hold Time, $t_{H\,DIS}$		V_{CC} = 5 0V T_A = 25°C			19	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75L51 and across the 0°C to 70°C range for the DM85L51 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted

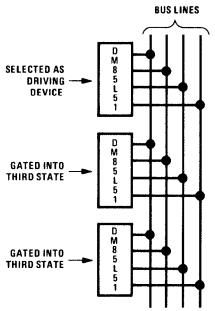


FIGURE 1

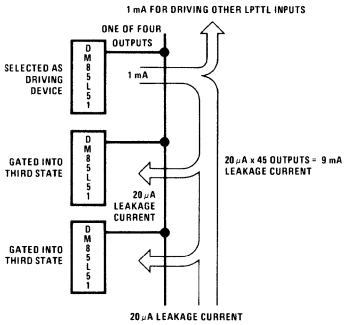


FIGURE 2

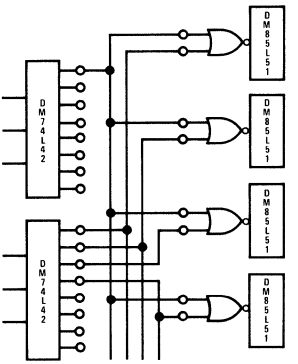


FIGURE 3

mode of operation

The high impedance state occurs on all outputs of all devices except the four outputs of the one device selected (Figure 1). The result is that the selected device has a normal LPTTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from a logical "0" to a logical "1". The other outputs are all in the "third-state" and take only a small amount of leakage current from the driving outputs. Since the logical "1" output current of the selected device is 5 times that of a normal Series 54L/74L output (1.0 mA vs 200 μA), the output is easily able to supply that leakage current to as many as 45 connected devices and still retain enough drive for a full Series 54L/74L fanout of 10 at the end of the bus line (Figure 2).

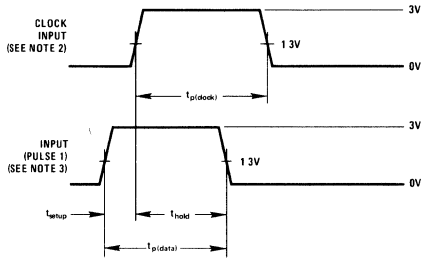
A two-input NOR gate facilitates selection of the driving device through the use of only two 1 out of 5 decoders for as many as 64 DM75L51/DM85L51s (Figure 3)

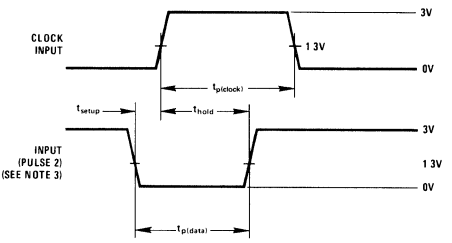
A problem inherent in conventional D-type flip flops is that it is impossible to code the data input in such a way as to cause the flip flop to remain in its present state when clocked. Because flexibility is not as great as with a J-K flip flop (and its J=0, K=0 state), to keep a D-type flip flop in its present state it is usually necessary to gate the clock, which increases the danger of false-clocking. The DM75L51/DM85L51 contains a gated input disable which does not disrupt clocking, but rather recirculates information from the Q output to the D input. In this manner the flip flop does not change state and the possibility of false-clocking is eliminated.

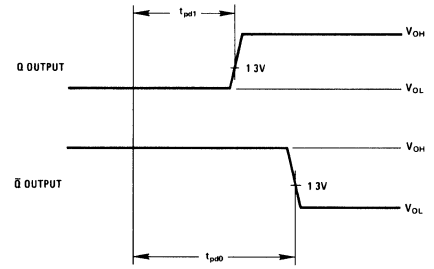
The following logic levels control the device:

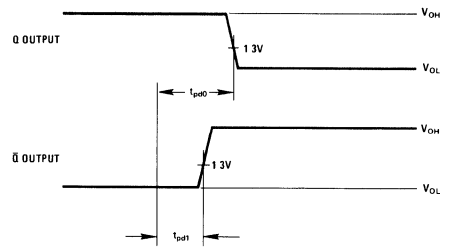
- Clocking occurs on the positive-going transition.
- Clearing is enabled by taking the input to a logical "1" level.
- Outputs are placed in the "third-state" if either of the two Output Disable inputs is taken to a logical "1" level.
- The flip flops will remain in their previous state when clocked so long as either of the two Data Input Disable inputs is taken to a logical "1" level.

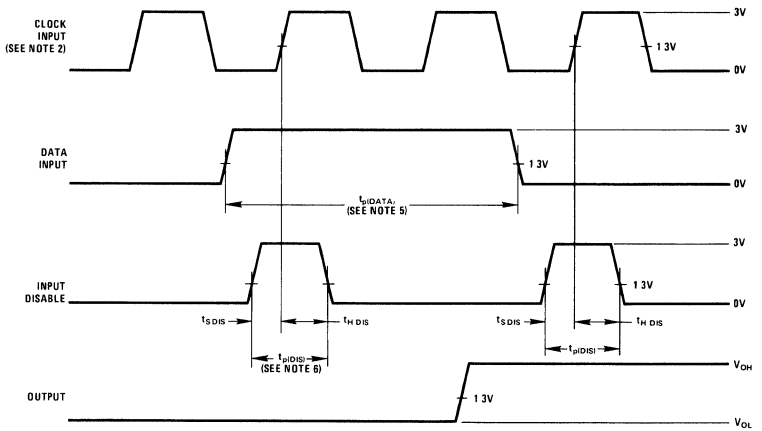
switching time waveforms

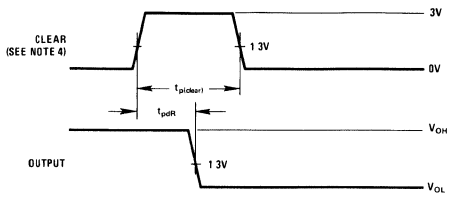






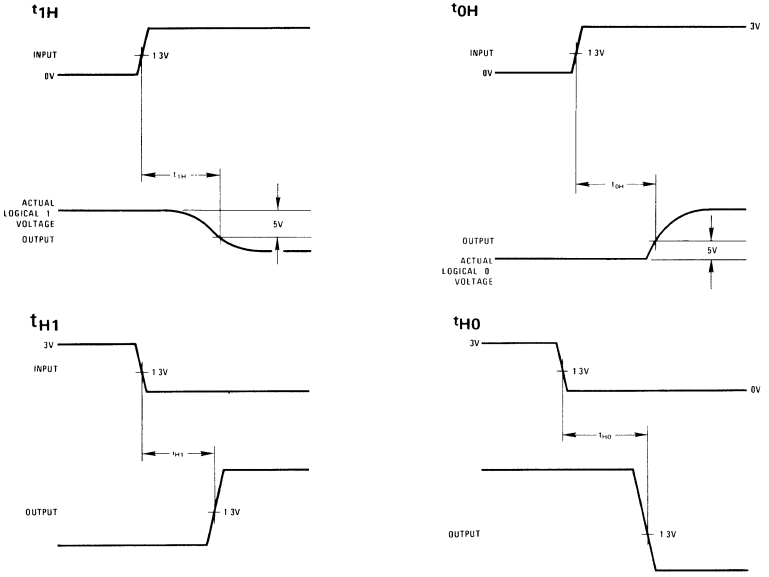




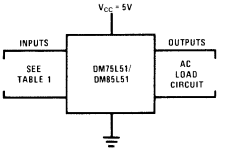


Note 1 All input pulses have $t_r = t_f = 15$ ns
Note 2 Clock input $t_{p(clock)} > 200$ ns and PRR = 500 kHz When testing f_{clock}, use 50% duty cycle
Note 3 Pulse 1 and pulse 2 $t_n = 100$ ns, PRR is 50% of the clock PRR
Note 4 $t_{p(clear)} = > 100$ ns, PRR = 500 kHz
Note 5 $t_{p(DATA)} = 4\ t_{p(clock)}$ and PRR = 125 kHz
Note 6 $t_{p(DIS)} = t_{p(clock)}$ and PRR = 250 kHz

switching time waveforms (con't)

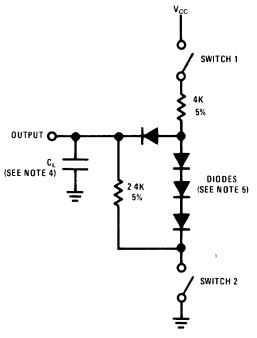


ac test circuits



AC TEST	INPUT CONDITIONS									
	OUTPUT DISABLE 1	OUTPUT DISABLE 2	CLOCK	DATA INPUT DISABLE	DATA INPUT DISABLE	INPUT D	INPUT C	INPUT B	INPUT A	CLEAR
t_{pd0}	GND	GND	See Note 1	GND	GND	See Note 2	See Note 2	See Note 2	See Note 2	GND
t_{pd1}	GND	GND	See Note 1	GND	GND	See Note 2	See Note 2	See Note 2	See Note 2	GND
t_{pdR}	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}	See Note 2
t_{1H}	See Note 3	See Note 3	See Note 2	GND	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}	GND
t_{0H}	See Note 3	See Note 3	GND	GND	GND	GND	GND	GND	GND	V_{CC}
t_{H1}	See Note 3	See Note 3	See Note 2	GND	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}	GND
t_{H0}	See Note 3	See Note 3	GND	GND	GND	GND	GND	GND	GND	V_{CC}
$t_{S\,DATA}$	GND	GND	See Note 1	GND	GND	See Note 2	See Note 2	See Note 2	See Note 2	GND
$t_{H\,DATA}$	GND	GND	See Note 1	GND	GND	See Note 2	See Note 2	See Note 2	See Note 2	GND
$t_{S\,DIS}$	GND	GND	See Note 1	See Note 3	See Note 3	See Note 2	See Note 2	See Note 2	See Note 2	GND
$t_{H\,DIS}$	GND	GND	See Note 1	See Note 3	See Note 3	See Note 2	See Note 2	See Note 2	See Note 2	GND
f_{clock}	GND	GND	See Note 7	GND	GND	See Note 2	See Note 2	See Note 2	See Note 2	GND

ac load circuit



TEST	SWITCH S_1	SWITCH S_2	C_L	
t_{pd0}	Closed	Closed	50 pF	
t_{pd1}	Closed	Closed	50 pF	
t_{pdR}	Closed	Closed	50 pF	
t_{1H}	Closed	Closed	5 pF	(See Note 6)
t_{0H}	Closed	Closed	5 pF	
t_{H1}	Open	Closed	50 pF	
t_{H0}	Closed	Open	50 pF	
$t_{S\,DATA}$	Closed	Closed	50 pF	
$t_{H\,DATA}$	Closed	Closed	50 pF	
$t_{S\,DIS}$	Closed	Closed	50 pF	
$t_{H\,DIS}$	Closed	Closed	50 pF	
f_{clock}	Closed	Closed	50 pF	

Note 1 Pulse gen PRR = 500 kHz, $t_{p(clock)} \geq 200$ ns, $t_r = t_f = 15$ ns
Note 2 See ac switching time waveforms
Note 3 Tie these inputs together, see ac switching time waveforms
Note 4 Includes jig and probe capacitance
Note 5 All diodes are 1N3064 or equivalent
Note 6 Jig capacitance
Note 7 Use 50% duty cycle

3

Series 54L/74L

DM75L52/DM85L52 TRI-STATE® decade counter/latch
DM75L54/DM85L54 TRI-STATE binary counter/latch

general description

The DM75L52/DM85L52 and DM75L54/DM85L54 are LPTTL TRI-STATE synchronous decade and binary counter/latch circuits respectively. The circuit consists of a counter made up of four edge-triggered J-K flip-flops.

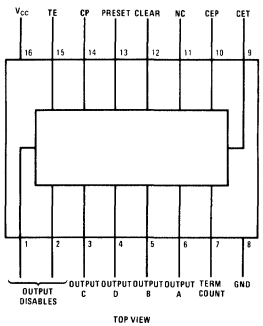
The circuits logically combine the function of counters for frequency division, latches to hold the counter's information, and output buffer gates which allow active LPTTL outputs as well as the high impedance (3rd) state for output multiplexing of data.

features

- Series 54L/74L compatible
- 38 mW typical power dissipation
- TRI-STATE outputs directly connectable for bus-line operation
- TRI-STATE outputs information may be latched
- 50 ns typical propagation delay
- Count mode and terminal count output are operable when the outputs are in the high impedance state or latch mode.
- Blanking capability with the DM75L52/DM85L52
- Positive true logic

logic and connection diagram

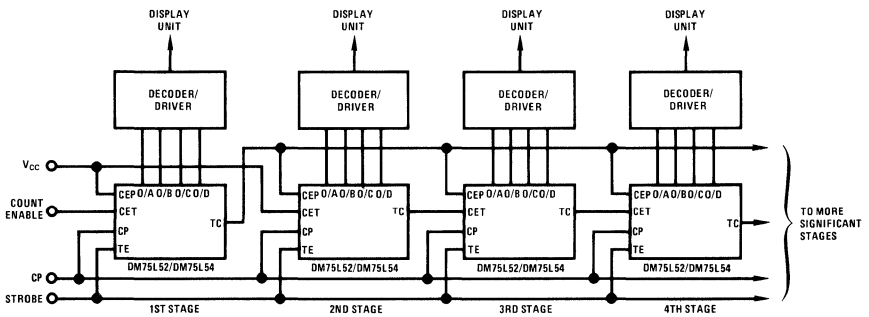
Dual-In-Line and Flat Package



TOP VIEW

typical application

Multi-Stage Synchronous Counter with Visual Display



absolute maximum ratings (Note 1)

Supply Voltage	8 0V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75L52/75L54	4.5	5 5	V
DM85L52/85L54	4.75	5.25	V
Temperature (T_A)			
DM75L52,DM75L54	−55	+125	°C
DM85L52,DM85L54	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2 4	1 3		V
Logical "0" Input Voltage			1 3	0 7	V
Logical "1" Output Voltage	I_{OUT} = −1 mA	2 4	2 7		V
Logical "1" Output Voltage — Terminal Count	I_{OUT} = −200 μA	2 4	2 8		V
Logical "0" Output Voltage	DM75L52/DM75L54, I_{OUT} = 2 mA		0 15	0 3	V
	DM85L52/DM85L54, I_{OUT} = 3 2 mA		0 2	0 4	V
Third State Output Current	V_{OUT} = 2 4V			20	μA
	V_{OUT} = 0 3V			−40	μA
Logical "1" Input Current	V_{IN} = 2 4V		<2	20	μA
"CET"	V_{IN} = 5 5V		<20	200	μA
"Other Inputs"	V_{IN} = 2 4V		<1	10	μA
	V_{IN} = 5 5V		<10	100	μA
Logical "0" Input Current					
"CET"	V_{IN} = 0 3V		−240	−360	μA
"Other Inputs"	V_{IN} = 0 3V		−120	−180	μA
Output Short Circuit Current (Note 3)	V_{OUT} = 0V	−3	−8	−15	mA
Supply Current — (Each Device) I_{CC} (Max)			7 6	13 0	mA
Propagation Delay to a Logical "0" from Clock to any Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		75	150	ns
Propagation Delay to a Logical "1" from Clock to any Output, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		115	220	ns
Propagation Delay from TE to Output, $t_{pd(TE)}$	V_{CC} = 5 0V, T_A = 25°C		90	160	ns
Delay from Output Disable to High Impedance State (from Logical "1" Level), t_{1H}	V_{CC} = 5 0V, T_A = 25°C		8	15	ns
Delay from Output Disable to High Impedance State (from Logical "0" Level), t_{0H}	V_{CC} = 5 0V, T_A = 25°C		57	105	ns
Delay from Output Disable to Logical "1" Level (from High Impedance State), t_{H1}	V_{CC} = 5 0V, T_A = 25°C		75	150	ns
Delay from Output Disable to Logical "0" Level (from High Impedance State), t_{H0}	V_{CC} = 5 0V, T_A = 25°C		90	150	ns
Maximum Clock Frequency	V_{CC} = 5 0V, T_A = 25°C	6	11		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75L52, DM75L54 and across the 0°C to 70°C range for the DM85L52,DM85L54 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

mode of operation

When the Transfer Enable (TE) is at a logical "1" level the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear (CL) resets the counter to 0000.

Asynchronous Preset (PRE) sets the counter to 1111. The 1111 state may be used in the DM75L52/DM85L52 for blanking out leading zeroes in visual displays. The next clock pulse will advance the DM75L52/DM85L52 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the DM75L54/DM85L54 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

DM75L52/DM85L52 $TC = CET \cdot A \cdot \overline{B} \cdot \overline{C} \cdot D$

DM75L54/DM85L54 $TC = CET \cdot A \cdot B \cdot C \cdot D$

The following logic levels control the device:

- The counters changes state on the positive-going transition of the clock.
- Clearing or presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "third-state" either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique (see application).

Counter stages can be cascaded as shown above to provide multiple stage BCD or Binary synchronous counting by using the DM75L52/DM85L52 or the DM75L54/DM85L54 respectively. With a Terminal Count (TC) fan out of ten the above scheme allows eleven stages to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the strobe line while the counters can continue counting. The display can be updated by applying a positive pulse to the strobe line.

logic tables

FUNCTION TABLE

INPUTS							OUTPUTS				
OD1	OD2	CEP	CET	CLEAR	PRESET	TE	A	B	C	D	TC
1	X	X	X	X	X	X	"High Impedance State"				*
X	1	X	X	X	X	X	"High Impedance State"				*
0	0	X	X	1	X	1	0	0	0	0	0
0	0	X	X	0	1	1	1	1	1	1	*
0	0	X	X	X	X	0	LATCH				*
0	0	1	1	0	0	1	COUNT				*

*Function of the count sequence

DM75L52/DM85L52
DECADE COUNT SEQUENCE

	OUTPUTS				
COUNT	A	B	C	D	TC
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
3	1	1	0	0	0
4	0	0	1	0	0
5	1	0	1	0	0
6	0	1	1	0	0
7	1	1	1	0	0
8	0	0	0	1	0
9	1	0	0	1	1
**If Preset Applied Next Count	1	1	1	1	0
	1	0	0	0	0

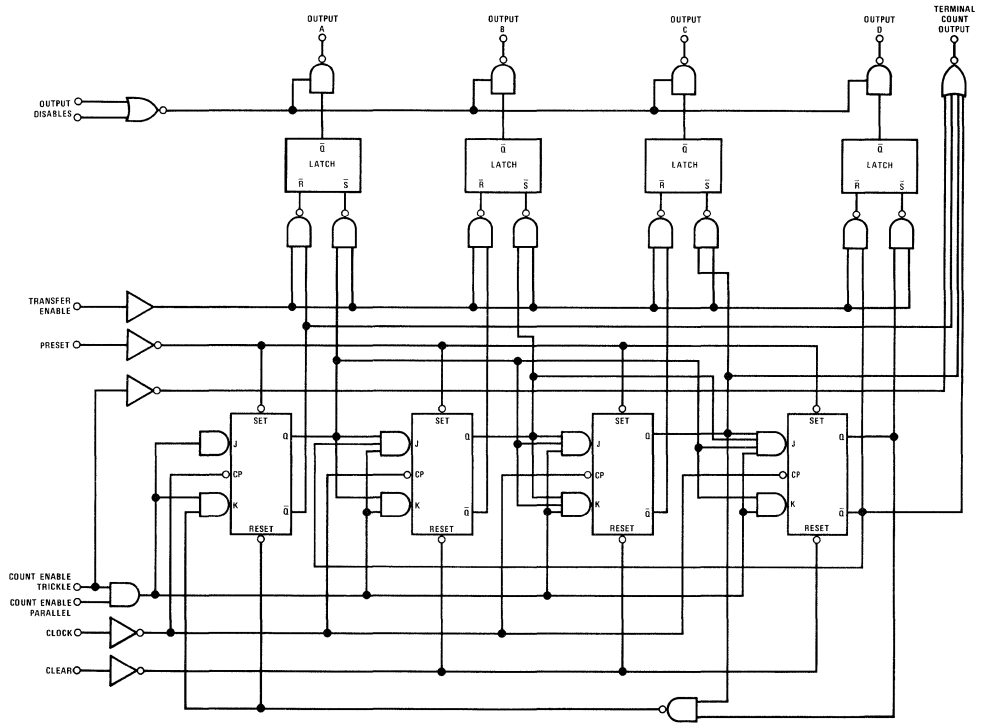
**The 1111 state may be used in conjunction with certain decoder/drivers i e , DM5446, DM5447 and DM5448 for blanking leading zeroes

DM75L54/DM85L54
BINARY COUNT SEQUENCE

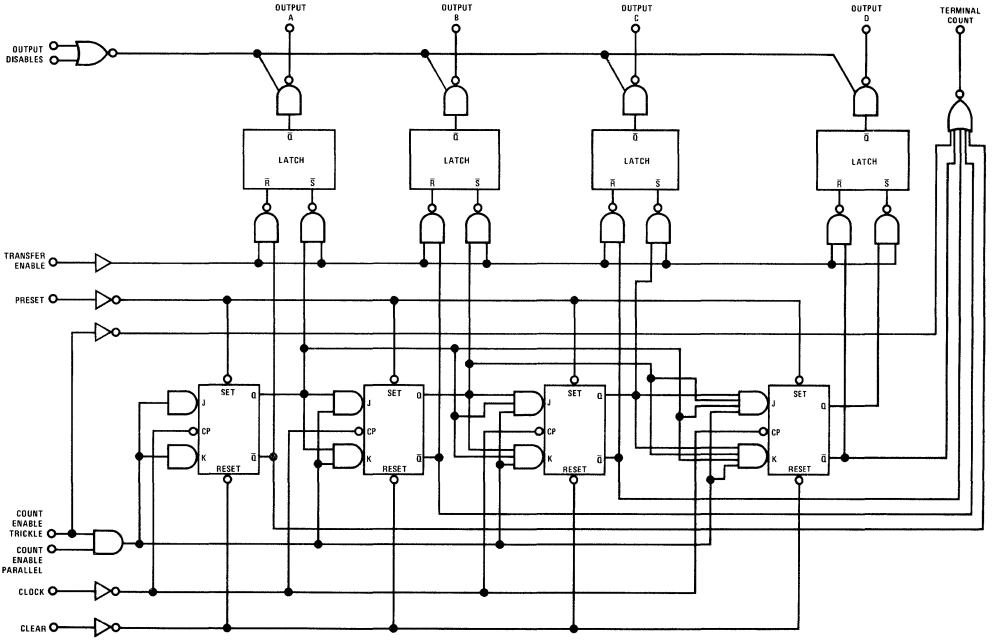
	OUTPUTS				
COUNT	A	B	C	D	TC
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
3	1	1	0	0	0
4	0	0	1	0	0
5	1	0	1	0	0
6	0	1	1	0	0
7	1	1	1	0	0
8	0	0	0	1	0
9	1	0	0	1	0
10	0	1	0	1	0
11	1	1	0	1	0
12	0	0	1	1	0
13	1	0	1	1	0
14	0	1	1	1	0
15	1	1	1	1	1

logic diagrams

DM75L52/DM85L52



DM75L54/DM85L54



ac test circuit

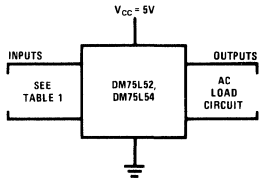
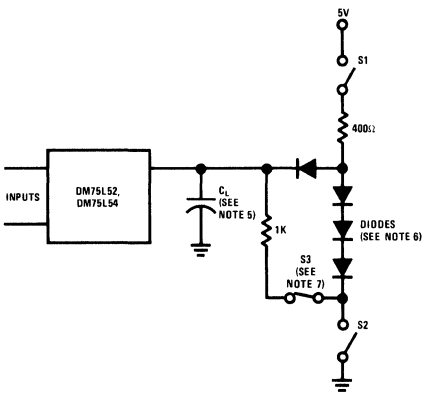


FIGURE 1

TEST	INPUT CONDITIONS							
	OD1	OD2	CET	CEP	CLEAR	PRESET	CP	TRANSFER ENABLE
t_{pd0}	GND	GND	V_{CC}	V_{CC}	GND	GND	See Note 1	V_{CC}
t_{pd1}	GND	GND	V_{CC}	V_{CC}	GND	GND	See Note 1	V_{CC}
$t_{pd(TE)}$	GND	GND	V_{CC}	V_{CC}	GND	GND	See Note 1	See Note 2
t_{1H}	See Note 4	See Note 4	GND	GND	GND	V_{CC}	GND	V_{CC}
t_{0H}	See Note 4	See Note 4	GND	GND	V_{CC}	GND	GND	V_{CC}
t_{H1}	See Note 4	See Note 4	GND	GND	GND	V_{CC}	GND	V_{CC}
t_{H0}	See Note 4	See Note 4	GND	GND	V_{CC}	GND	GND	V_{CC}
f_{CLOCK}	GND	GND	V_{CC}	V_{CC}	GND	GND	See Note 9	V_{CC}

TABLE 1

ac load circuit

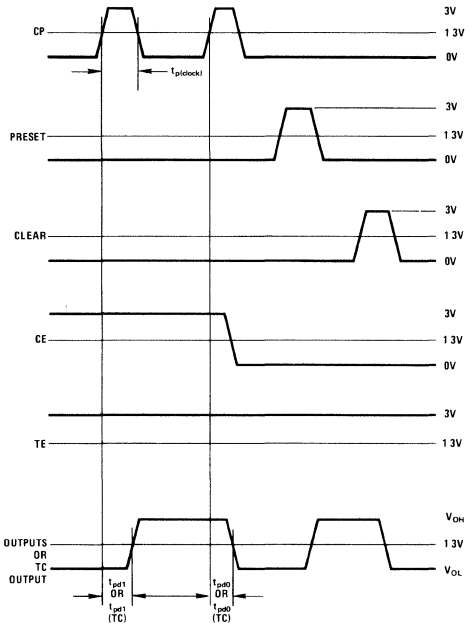


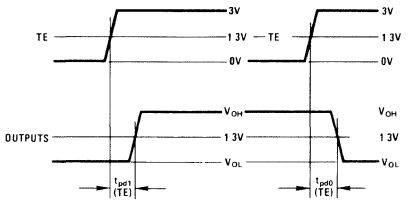
TEST	SWITCH S1	SWITCH S2	C_L
t_{pd0}	Closed	Closed	50 pF
t_{pd1}	Closed	Closed	50 pF
$t_{pd(TE)}$	Closed	Closed	50 pF
t_{1H}	Closed	Closed	50 pF (See Note 8)
t_{0H}	Closed	Closed	50 pF (See Note 8)
t_{H1}	Open	Closed	50 pF
t_{H0}	Closed	Open	50 pF
f_{clock}	Closed	Closed	50 pF

FIGURE 2

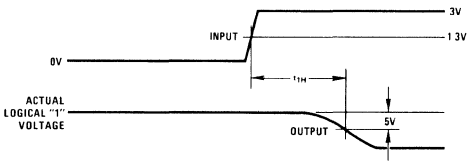
Note 1 Pulse gen PRR $\leq$ 1 MHz, $t_r \leq$ 15 ns, $t_f \leq$ 5 ns, $t_{p(clock)} \geq$ 200 ns
Note 2 See switching time waveforms
Note 3 Apply V_{CC} momentarily to clear input then ground, enter 9 clock pulses for DM75L52/DM85L52 or 15 clock pulses for DM75L54/DM85L54, leaving the clock high on the last clock pulse
Note 4 Tie these inputs together, see switching time waveforms
Note 5 Includes jig capacitance
Note 6 All diodes are FD100 or equivalent
Note 7 Open switch S3 for $t_{pd0(TC)}$, $t_{pd1(TC)}$,
Note 8 Jig capacitance
Note 9 f_{clock} use 50% duty cycle

switching time waveforms

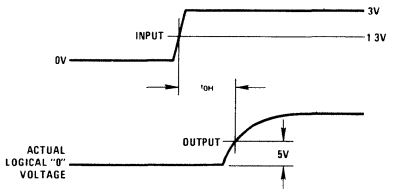




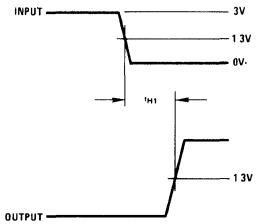
t_{1H}



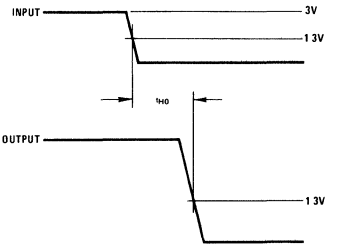
t_{OH}



t_{H1}



t_{HO}



Series 54L/74L

DM76L75/DM86L75 low power presettable decade counter
DM76L76/DM86L76 low power presettable binary counter

general description

The DM76L75/DM86L75 and DM76L76/DM86L76 are synchronous up decade and binary counters respectively. They have synchronous parallel load capability, overriding asynchronous master reset, terminal count and carry look-ahead logic for high speed multi-decade operation.

The counters are synchronous, with the counter outputs changing state after the logical "0" to logical "1" transition of the clock. When the parallel enable input is low, the parallel inputs determine the next state of the counter synchronously with the clock.

Mode selection is accomplished as shown in the table below. However the transition of C_{EP} or C_{ET} from logical "1" to logical "0" or of $\overline{PE}$ from logical "0" to logical "1" may only be done with CP in the logical "1" state.

A logical "0" level on $\overline{MR}$ will reset all outputs to logical "0".

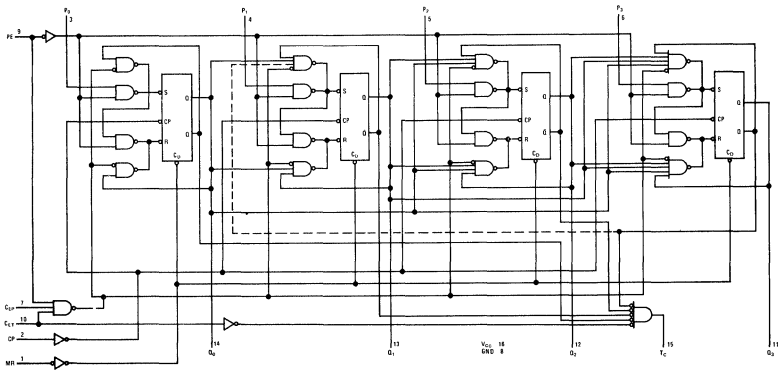
The purpose of the C_{EP} and C_{ET} inputs and the T_C output is to provide for a fast propagation delay when cascading several decades (shown below).

Operation can best be understood by realizing that in order for counting to occur both C_{EP} and C_{ET} must be at logical "1" levels. In addition the T_C output is a logical "1" only when a counter is at its maximum count (9 for the DM76L75/DM86L75 ; and 15 for the DM76L76/DM86L76) and when the C_{ET} input is at a logical "1" level. Therefore if counters are connected as shown, a more significant counter stage cannot be clocked until all previous counters are at their maximum count. The reason for the feedforward connection from the least significant counter to all C_{EP} inputs is that no counter needs to wait for a ripple from the previous counter when the least significant counter changes from a maximum count to zero.

features

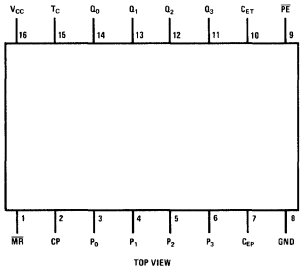
- 32 mW typical power
- 13 MHz typical count frequency
- Series 54L/74L compatible
- Pin compatible with 93L10, 93L16

logic and connection diagrams



Note Dotted line portions applicable to DM76L75/DM86L75 only

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM76L75, DM76L76	−55°C to +125°C
DM86L75, DM86L76	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM76L75/76 DM86L75/76	V_{CC} = 4 5V V_{CC} = 4 75V		2 0	1 3		V
Logical "0" Input Voltage	DM76L75/76 DM86L75/76	V_{CC} = 4 5V V_{CC} = 4 75V			1 3	0 7	V
Logical "1" Output Voltage	DM76L75/76 DM86L75/76	V_{CC} = 4 5V V_{CC} = 4 75V	I_{OUT} = −200 μA	2.4	3 1		V
Logical "0" Output Voltage	DM76L75/76 DM86L75/76	V_{CC} = 4 5V V_{CC} = 4 75V	I_{OUT} = 2 0 mA I_{OUT} = 3 2 mA		0 2 0 2	0 3 0 4	V V
Logical "1" Input Current All Inputs Except C_{ET}	DM76L75/76 DM86L75/76	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 2 4V V_{IN} = 5 5V			10 100	μA μA
C_{ET}	DM76L75/76 DM86L75/76	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 2 4V V_{IN} = 5 5V			20 200	μA μA
Logical "0" Input Current All Inputs Except C_{ET}	DM76L75/76 DM86L75/76	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 0 3V V_{IN} = 0 4V		−100	−180	μA
C_{ET}	DM76L75/76 DM86L75/76	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 0 3V V_{IN} = 0 4V		−200	−360	μA
Output Short Circuit Current (Note 3)	DM76L75/76 DM86L75/76	V_{CC} = 5 5V V_{CC} = 5 25V		−3	−9	−15	mA
Supply Current	DM76L75/76 DM86L75/76	V_{CC} = 5 5V V_{CC} = 5 25V			6 5	9	mA
Propagation Delays Clock to Any Q Output							
	t_{pd0}				65	110	ns
	t_{pd1}				45	75	ns
Clock to T_C Output							
	t_{pd0}				85	140	ns
	t_{pd1}				70	115	ns
C_{ET} to T_C Output							
	t_{pd0}				35	60	ns
	t_{pd1}				35	60	ns
t_s (CE)		Setup Time CE			40	65	ns
t_r (CE)		Release Time CE			50	80	ns
t_s		Setup Time P Inputs			15	30	ns
t_r		Release Time P Inputs			15	30	ns
t_s ($\overline{PE}$)		Setup Time Parallel Entry			40	65	ns
t_r ($\overline{PE}$)		Release Time Parallel Entry			40	65	ns
Count Frequency				6	13		MHz
Clock Pulse Width				60	25		ns
Reset Pulse Width				80	30		ns

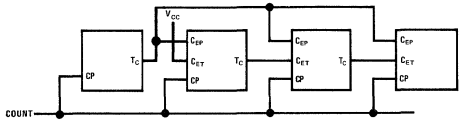
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM76L75 and DM76L76 and across the 0°C to 70°C range for the DM86L75 and DM86L76. All typicals are given for V_{CC} = 5 0V and T_A = 25°C.

mode selection

$\overline{PE}$	CE	MODE
1	1	Count
1	0	No Change
0	X	Preset

cascading counters



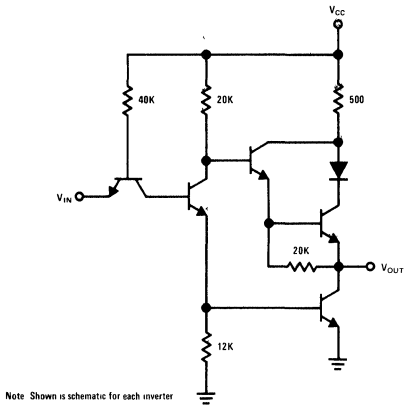
Series 54L/74L

DM88L12 TTL-MOS hex inverter/ interface gate

general description

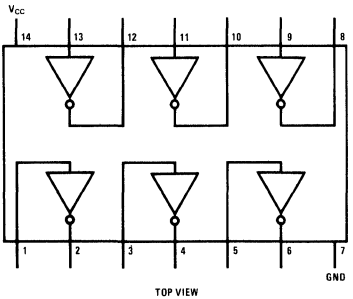
The DM88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} – 2.2V with an output current of –200 μA.

schematic and connection diagrams



Note Shown is schematic for each inverter

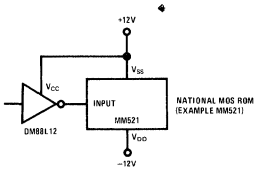
Dual-In-Line and Flat Package



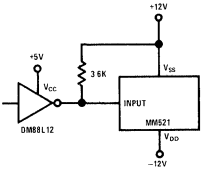
TOP VIEW

typical applications

TTL Interface to MOS ROM
Without Resistive Pull-Up



TTL Interface to MOS ROM
With Resistive Pull-Up



ac test circuits

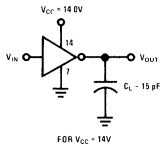


Figure 1

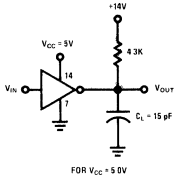
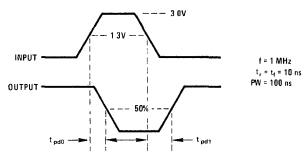


Figure 2

switching time waveforms



absolute maximum ratings (Note 1)

Supply Voltage	15V
Input Voltage	5 5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM78L12	4.5	5.5	V
DM88L12	4 75	5.25	V
Temperature			
DM78L12	−55	125	°C
DM88L12	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 14 0V			2 0	1.3		V
	V_{CC} = Min			2 0	1 3		V
Logical "0" Input Voltage	V_{CC} = 14 0V				1 3	0 7	V
	V_{CC} = Min				1 3	0 7	V
Logical "1" Output Voltage	V_{CC} = 14 0V	V_{IN} = 0 7V	I_{OUT} = −200 μA	11 8	12 0		V
	V_{CC} = Min	V_{IN} = 0 7V	I_{OUT} = +200 μA	14 5	15 0		V
Logical "0" Output Voltage	V_{CC} = 14 0V	V_{IN} = 2.0V	I_{OUT} = 12 mA		0 5	1 0	V
	V_{CC} = Min	V_{IN} = 2 0V	I_{OUT} = 3 2 mA		0 2	0 4	V
Logical "1" Input Current	V_{CC} = 14 0V	V_{IN} = 2 4V			<1	20	μA
	V_{CC} = Max	V_{IN} = 2 4V			<1	10	μA
	V_{CC} = 14 0V	V_{IN} = 5 5V			<1	100	μA
	V_{CC} = Max	V_{IN} = 5 5V			<1	100	μA
Logical "0" Input Current	V_{CC} = 14 0V	V_{IN} = 0 4V			-320	-500	μA
	V_{CC} = Max	V_{IN} = 0 4V			-100	-180	μA
Output Short Circuit Current (Note 3)	V_{CC} = 14 0V	V_{OUT} = 0V		-10	-25	-50	mA
	V_{CC} = Max	V_{OUT} = 0V		-3	-8	-15	mA
Supply Current — Logical "1" (Each Inverter)	V_{CC} = 14 0V	V_{IN} = 0V			0 32	0 50	mA
	V_{CC} = Max	V_{IN} = 0V			0 11	0 16	mA
Logical "0"	V_{CC} = 14 0V	V_{IN} = 5 25V			1 0	1 5	mA
	V_{CC} = Max	V_{IN} = 5.25V			0 3	0 5	mA
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C	See Figure 2			27	45	ns
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 14 0V, T_A = 25°C	See Figure 1			11	20	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1} (Note 4)	V_{CC} = 5 0V, T_A = 25°C	See Figure 2			79	100	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1}	V_{CC} = 14 0V, T_A = 25°C	See Figure 1			34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78L12 and across the 0°C to +70°C range for the DM88L12. All typicals are given for V_{CC} = 5.0V and T_A = 25°C, or for V_{CC} = 14.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Note 4: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

Series 74S

REFERENCE

The following table references all Physical Dimension Drawings for the devices in this section. For Order Numbers, see below * Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES										WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)					
		Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Fig.	Pg.
DM74S00	4-1	3	II													
DM74S03	4-1	3	II													
DM74S04	4-1	3	II													
DM74S05	4-1	3	II													
DM74S10	4-1	3	II													
DM74S11	4-1	3	II													
DM74S15	4-1	3	II													
DM74S20	4-1	3	II													
DM74S22	4-1	3	II													
DM74S40	4-1	3	II													
DM74S64	4-1	3	II													
DM74S65	4-1	3	II													
DM74S74	4-1	3	II													
DM74S86	4-5	3	II													
DM74S112	4-1	5	II													
DM74S113	4-1	3	II													
DM74S114	4-1	3	II													
DM74S135	4-5	5	II													
DM74S140	4-1	3	II													
DM74S151	4-7	5	II													
DM74S251	4-7	5	II													
DM74S153	4-7	5	II													
DM74S253	4-7	5	II													
DM74S157	4-7	5	II													
DM74S257	4-7	5	II													
DM74S158	4-7	5	II													
DM74S258	4-7	5	II													

*Order Numbers use Device No suffixed with package letter, i.e. DM74S00N

Series 74S

series DM74S schottky-clamped transistor-transistor logic

general description

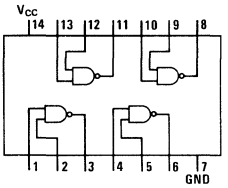
The gates, inverters, buffers and flip flops in the DM74S series are ultra-high speed versions of the similarly numbered devices in National's standard series 54/74 family. They can be used in combination with series 54/74 circuits whenever the absolute minimum propagation delays are required.

features

- Typical gate delay of 3 ns
- Higher source and sink currents than standard TTL
- Fanout of 10 series DM74S loads or 12 standard series 54/74 loads
- Compatible with all series 54/74 families
- Pin identical to lower speed devices
- 19 mW typical power dissipation

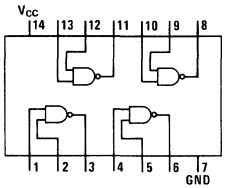
connection diagrams (Dual-In-Line Package, Top Views)

DM74S00



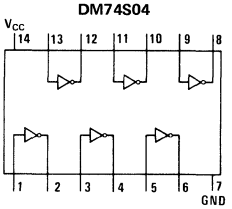
t_{pd} = 3 ns typ
P_D = 19 mW typ/Gate

DM74S03



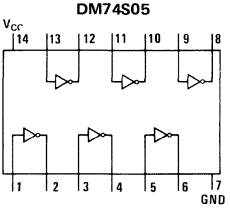
t_{pd} = 5 ns typ
P_D = 17 mW typ/Gate

DM74S04



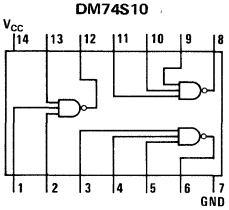
t_{pd} = 3 ns typ
P_D = 19 mW typ/Gate

DM74S05



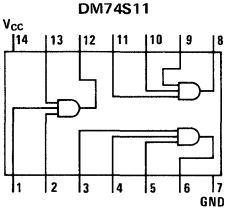
t_{pd} = 5 ns typ
P_D = 17 mW typ/Gate

DM74S10



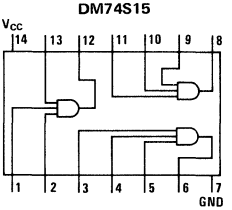
t_{pd} = 3 ns typ
P_D = 19 mW typ/Gate

DM74S11



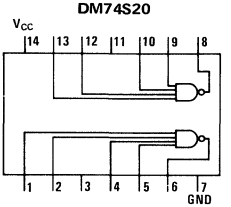
t_{pd} = 5 ns typ
P_D = 32 mW typ/Gate

DM74S15



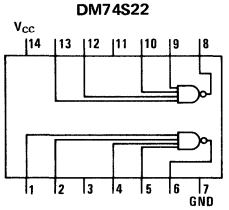
t_{pd} = 6 ns typ
P_D = 29 mW typ/Gate

DM74S20



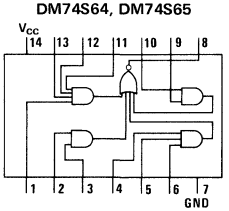
t_{pd} = 3 ns typ
P_D = 19 mW typ/Gate

DM74S22



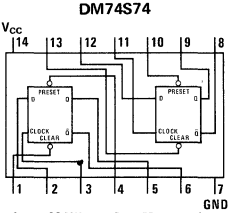
t_{pd} = 5 ns typ
P_D = 17 mW typ/Gate

DM74S64, DM74S65



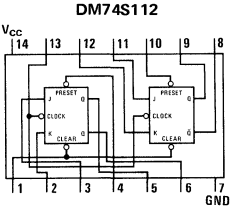
DM74S64 t_{pd} = 3.5 ns typ, P_D = 39 mW typ
DM74S65 t_{pd} = 5 ns typ, P_D = 36 mW typ

DM74S74



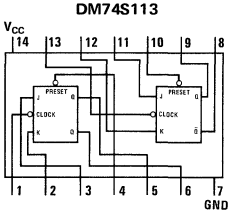
f_{max} = 90 MHz typ P_D = 75 mW typ/FF
CLOCK = Low to High Transition

DM74S112



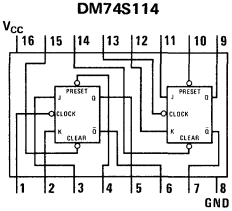
f_{max} = 125 MHz typ P_D = 75 mW typ/FF
CLOCK = High to Low Transition

DM74S113



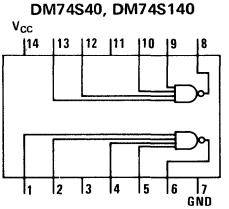
f_{max} = 125 MHz typ P_D = 75 mW typ/FF
CLOCK = High to Low Transition

DM74S114



f_{max} = 125 MHz typ P_D = 75 mW typ/FF
CLOCK = High to Low Transition

DM74S40, DM74S140



t_{pd} = 4 ns typ
P_D = 41 mW typ/Gate

absolute maximum ratings

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Interemitter Voltage	5.5V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

operating conditions (Note 1)

	MIN	NOM	MAX
Supply Voltage, V_{CC}	4.75	5.0	5.25
Operating Free-Air Temperature Range	0°C	25°C	70°C

high speed gates, buffers and line drivers

dc electrical characteristics (V_{CC} = +5V, T_A = 25°C)

over operating free-air temperature range (unless otherwise noted)

SYMBOLS	PARAMETER	CONDITIONS (Note 1)	MIN	TYP (Note 2)	MAX	UNIT
DM74S00, DM74S04, DM74S10, DM74S20						
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1 2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0 8V, I_{OH} = −1mA	2 7	3 4		V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 20 mA			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} Max, V_I = 5 5V			1	mA
I_{IH}	High-Level Input Current (Each Input)	V_{CC} = Max, V_I = 2 7V			50	μA
I_{IL}	Low-Level Input Current (Each Input)	V_{CC} = Max, V_I = 0 5V			−2	mA
I_{OS}	Short-Circuit Output Current (Note 3)	V_{CC} = Max	−40		−100	mA
I_{CCH}	Supply Current, High-Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 0V		2 5	4	mA
I_{CCL}	Supply Current, Low-Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 5V		5	9	mA
DM74S03, DM74S05, DM74S22						
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1 2	V
V_{OH}	High Level Output Current	V_{CC} = Min, V_{IL} = 0 8V, V_{OH} = 5 5V			250	μA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 20 mA			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V			1	mA
I_{IH}	High-Level Input Current (Each Input)	V_{CC} = Max, V_I = 2 7V			50	μA
I_{IL}	Low Level Input Current (Each Input)	V_{CC} = Max, V_I = 0 5V			−2	mA
I_{CCH}	Supply Current, High Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 0V		1 5	3 3	mA
I_{CCL}	Supply Current, Low Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 5V		5	9	mA
DM74S40, DM74S140						
V_{IH}	High Level Input Voltage			2		V
V_{IL}	Low-Level Input Voltage				0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1 2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0 8V, I_{OH} = −3 mA	2 7	3 4		V
		V_{CC} = Min, V_I = 0 5V, (R_O = 50 Ω to GND, DM74S140)	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 60 mA			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V			1	mA
I_{IH}	High-Level Input Current (Each Input)	V_{CC} = Max, V_I = 2 7V			100	μA
I_{IL}	Low-Level Input Current (Each Input)	V_{CC} = Max, V_I = 0 5V			−4	mA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max	−50		−225	mA
I_{CCH}	Supply Current, High-Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 0V		5	9	mA
I_{CCL}	Supply Current, Low-Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 5V		12 5	22	mA

ac switching characteristics (V_{CC} = +5V, T_A = 25°C)

SYMBOLS	PARAMETER	CONDITIONS (Note 1)	MIN	TYP (Note 2)	MAX	UNIT
DM74S00, DM74S04, DM74S10, DM74S20						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2	3 4 5	4 5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2	3 5	5	ns
DM74S03, DM74S05, DM74S22						
t_{PHL}	Propagation Delay Time, Low to High Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2	5 7 5	7 5	ns
t_{PHL}	Propagation Delay Time, High-to Low Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2	4 5 7	7	ns
DM74S40, DM74S140						
t_{PHL}	Propagation Delay Time, Low to High Level Output	C_L = 50 pF, R_L = 93 Ω C_L = 150 pF, R_L = 93 Ω	2	4 6	6 5	ns ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	C_L = 50 pF, R_L = 93 Ω C_L = 150 pF, R_L = 93 Ω	2	4 6	6 5	ns ns

Note 1: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.
Note 3: Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

ultra high speed schottky TTL flip-flops

dc electrical characteristics (V_{CC} = +5V, T_A = 25°C)

SYMBOLS	PARAMETER	CONDITIONS (Note 1)		MIN	TYP (Note 2)	MAX	UNIT
DM74S74							
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1 2	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8, I_{OH} = −1 mA		2 7	3 4		V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8, I_{OL} = 20 mA				0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2 7V	D Input Clock or Preset Clear			50 100 150	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0 5V	D Input Clock or Preset Clear			−2 −4 −6	mA
I_{OS}	Short-Circuit Output Current (Note 3)	V_{CC} = Max		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			30	50	mA
DM74S112							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1 2	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OH} = −1 mA		2 7	3 4		V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OL} = 20 mA				0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2 7V	J or K input Clock, Preset, or Clear			50 100	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0 5V	J or K Input Clock Preset or Clear			−1 6 −4 −7	mA
I_{OS}	Short Circuit Output Current (Note 3)	V_{CC} = Max,		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			30	50	mA

SYMBOLS	PARAMETER	CONDITIONS		DM74S113			DM74S114			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0 8			0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1 2			−1 2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OH} = −1 mA		2 7	3 4		2 7	3 4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OL} = 20 mA				0 5			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V				1			1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2 7V	J or K input Clock Preset Clear			50 100 100			50 200 100 200	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0 5V	J or K Input Clock Preset Clear			−1 6 −4 −7			−1 6 −8 −7 −14	mA
I_{OS}	Short Circuit Output Current (Note 3)	V_{CC} = Max		−40		−100	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			30	50		30	50	mA

Note 1 For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions
Note 2 All typical values are at V_{CC} = 5V, T_A = 25°C
Note 3 Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second
Note 4 I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4 5V

ac switching characteristics (V_{CC} = +5V, T_A = 25°C)

SYMBOLS	PARAMETER	CONDITIONS (Note 1)	MIN	TYP (Note 2)	MAX	UNIT
DM74S74						
f_{max}	Maximum Clock Frequency	C_L = 15 pF, R_L = 280 Ω	75	110		MHz
t_{PLH}	Propagation Delay Time, Low to High Level Output, From Clear or Preset			4	6	ns
t_{PHL}	Propagation Delay Time, High to Low-Level Output, From Clear or Preset (Clock Low)			5	8	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output, From Clock			6	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output, From Clock			6	9	ns
DM74S112, DM74S113, DM74S114						
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation Delay Time, Low-to High-Level Output From Clear or Preset		2	4	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output, From Clear or Preset		2	5	7	ns
t_{PLH}	Propagation Delay Time, Low-to High-Level Output, From Clock		2	4	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output, From Clock		2	5	7	ns

ultra high speed AND/AND-OR-INVERT gates

dc electrical characteristics (V_{CC} = +5V, T_A = 25°C)

SYMBOLS	PARAMETER	CONDITION	DM74S11			DM74S15			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0 8			0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1 2			−1 2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OH} = −1 mA	2 7	3 4					V
I_{OH}	High-Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{OH} = 5 5V						250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0 8V, I_{OL} = 20 mA			0 5			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V			1			1	mA
I_{IH}	High Level Input Current (Each Input)	V_{CC} = Max, V_I = 2 7V			50			50	µA
I_{IL}	Low Level Input Current (Each Input)	V_{CC} = Max, V_I = 0 5V			−2			−2	mA
I_{OS}	Short Circuit Output Current (Note 3)	V_{CC} = Max	−40		−100				mA
I_{CCH}	Supply Current High Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 5V		4 5	8		3 5	6 5	mA
I_{CCL}	Supply Current, Low-Level Output (Average Per Gate)	V_{CC} = Max, All Inputs at 0V		8	14		8	14	mA

SYMBOLS	PARAMETER	CONDITIONS	DM74S64			DM74S65			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0 8			0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1 2			−1 2	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 0 8V, I_{OH} = −1 mA	2 7	3 4					V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 0 8V, V_{OH} = 5 5V						250	µA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IL} = 2V, I_{OL} = 20 mA			0 5			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V			1			1	mA
I_{IH}	High-Level Input Current (Each Input)	V_{CC} = Max, V_I = 2 7V			50			50	µA
I_{IL}	Low Level Input Current (Each Input)	V_{CC} = Max, V_I = 0 5V			−2			−2	mA
I_{OS}	Short Circuit Output Current (Note 3)	V_{CC} = Max	−40		−100				mA
I_{CCH}	Supply Current, High-Level Output	V_{CC} = Max, (Note 5)		7	12 5		6	11	mA
I_{CCL}	Supply Current, Low-Level Output	V_{CC} = Max, (Note 6)		8 5	16		8 5	16	mA

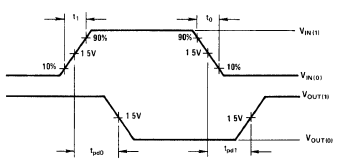
ac switching characteristics (V_{CC} = +5V, T_A = 25°C)

SYMBOLS	PARAMETER	CONDITION	DM74S11			DM74S15			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2 5	4 5 6	7	2 5	5 5 8 5	8 5	ns ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2 5	5 7 5	7 5	2 5	6 8	9	ns ns

SYMBOLS	PARAMETER	CONDITIONS	DM74S64			DM74S65			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2	3 5 5	5 5	2	5 8	7 5	ns ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	C_L = 15 pF, R_L = 280 Ω C_L = 50 pF, R_L = 280 Ω	2	3 5 5 5	5 5	2	5 5 6 5	8 5	ns ns

Note 1 For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions
Note 2 All typical values are at V_{CC} = 5V, T_A = 25°C
Note 3 Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second
Note 4 I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4 5V
Note 5 I_{CCH} is measured with all inputs grounded, and the outputs open
Note 6 I_{CCL} is measured with all inputs of one gate at 5V, the remaining inputs grounded, and the outputs open

switching time waveforms



Note 1 The pulse generator has the following characteristics $V_{IN}(1)$ = 3V $V_{IN}(0)$ = 0V t_1 = t_0 = 2 5 ns PRR = 1 MHz Duty Cycle = 50% Z_{OUT} = 50Ω
Note 2 C_L includes probe and jig capacitance

Series 74S

DM74S86(SN74S86) Schottky quad EXCLUSIVE-OR gate
DM74S135(SN74S135) Schottky quad EXCLUSIVE-OR/NOR gate

general description

The DM74S86 and DM74S135 are quad-two input EXCLUSIVE-OR gates designed for ultra high speed, high performance systems. Both devices are completely compatible with series 74, series 74H, series 74L, other series 74S devices and most DTL.

The DM74S86 is functionally identical to the DM7486 and can be used to upgrade existing designs with a minimum of logic changes.

The DM74S135 can operate as an EXCLUSIVE-OR gate (with C input LOW) or as an EXCLUSIVE NOR gate (C input HIGH).

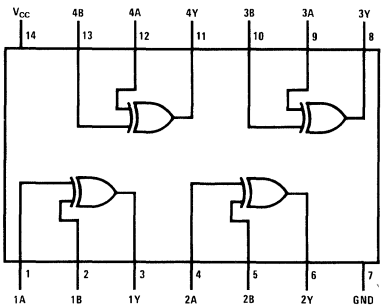
features

- Fully Compatible with Most TTL and TTL MSI Circuits
- Fully Schottky Clamping Reduces Delay Times·

DM74S86	7 ns typ.
DM74S135	8 ns typ.

logic and connection diagrams

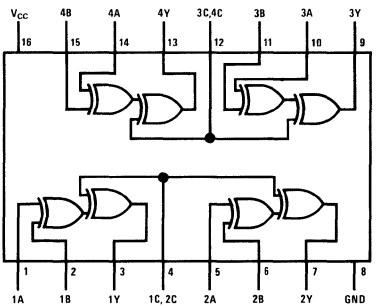
DM74S86
Dual-In-Line Package



TOP VIEW

POSITIVE LOGIC $Y = A \overline{B} + \overline{A} B$

DM74S135
Dual-In-Line Package



TOP VIEW

POSITIVE LOGIC WITH C LOW, $Y = A \oplus B = \overline{A}B + A\overline{B}$
WITH C HIGH, $Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$

function tables

DM74S86

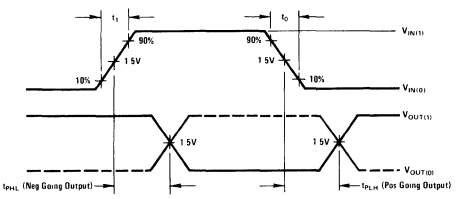
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

DM74S135

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = High Level, L = Low Level

switching time waveforms



Note 1 The pulse generator has the following characteristics $V_{IN}(1) = 3V$ $V_{IN}(0) = 0V$ $t_1 = t_0 = 2.5$ ns PRR = 1 MHz Duty Cycle = 50% $Z_{OUT} = 50\Omega$

Note 2 C_L includes probe and jig capacitance

4

absolute maximum ratings

Supply Voltage (Note 1)	7V
Input Voltage	5.5V
Operating Free-Air Temperature Range	
DM74S86, DM74S135 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

operating conditions

	MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}	4 75	5	5.25	V
Normalized Fan-Out From Each Output, N				
High Logic Level			20	
Low Logic Level			10	
Temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS (NOTE 2)	MIN	TYP (NOTE 3)	MAX	UNITS
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0 8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1 2	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OH} = −1 mA	2 7	3 4		V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OL} = 20 mA			0 5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5 5V			1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2 7V			50	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0 5V			−2	mA
I_{OS}	Short-Circuit Output Current (Note 4)	V_{CC} = Max	−40		−100	mA
I_{CC}	Supply Current DM74S86	V_{CC} = Max (Note 5)		50	75	mA
	Supply Current DM74S135			65	99	mA

Note 1: All voltage values are with respect to network ground terminal.
Note 2: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Note 3: All typical values are at V_{CC} = 5V, T_A = 25°C.
Note 4: Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.
Note 5: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics

PARAMETER*	FROM (INPUT)	CONDITIONS	DM74S86 MIN	DM74S86 TYP	DM74S86 MAX	DM74S135 MIN	DM74S135 TYP	DM74S135 MAX	UNITS
t_{PLH}	A or B	B or A = L, C = L **		7	10 5		8 5	13	ns
t_{PHL}				6 5	10		11	15	
t_{PLH}	A or B	B or A = H, C = L **		7	10 5		8	12	ns
t_{PHL}				6 5	10		9	13 5	
t_{PLH}	A or B	B or A = L, C = H					10	15	ns
t_{PHL}		C_L = 15 pF, R_L = 280Ω					6 5	10	
t_{PLH}	A or B	B or A = H, C = H					8 5	12	ns
t_{PHL}							7	11	
t_{PLH}	C	A = B					8	12	ns
t_{PHL}							9.5	14 5	
t_{PLH}	C	A ≠ B					7 5	11 5	ns
t_{PHL}							8	12	

* t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
** References to C input are applicable to DM74S135 only

Series 74S

series DM74S schottky-clamped multiplexers

general description

These devices in the DM74S series are Schottky-clamped, high performance, data selectors/multiplexers designed for use in very-high-speed data routing applications. These multiplexers select one of the "N" data sources when so directed by the binary address inputs. Each multiplexer is available with standard two-state outputs or National's TRI-STATE® outputs.

The DM74S151, DM74S153, DM74S157 and DM74S158 have Schottky TTL totem-pole outputs. The strobe inputs force all outputs low (complement outputs high) to permit further logic expansion.

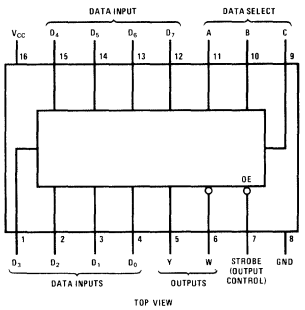
The DM74S251, DM74S253, DM74S257 and DM74S258 have Schottky TTL TRI-STATE outputs. The strobe inputs force the outputs to a high impedance state permitting N-bit (paralleled) data selectors with up to 129 sources connected to a data bus line. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed so that the output disable time is faster than the output enables.

features

- Schottky clamped for significant reduction in delay times
- High speed selection for one of eight, four or two data sources
- High fan-out, low impedance totem-pole outputs
- Strobe/output control. Line provided for expansion to N lines
- TRI-STATE outputs. Interface directly with System Bus
- Fully compatible with most TTL and DTL circuits

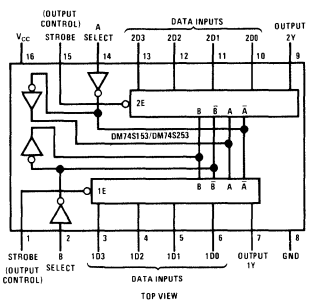
connection diagrams

DM74S151/DM74S251



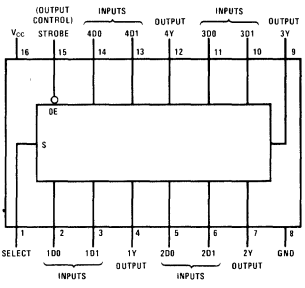
TOP VIEW

DM74S153/DM74S253



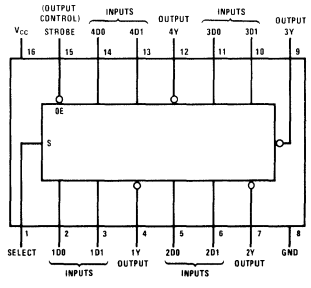
TOP VIEW

DM74S157/DM74S257



TOP VIEW

DM74S158/DM74S258



TOP VIEW

ordering information

All DM74S Series multiplexers are available in the 16-lead Molded Dual-In-Line (N) package.
Order all DM74S Series devices by their specific number, and add the package designation letter (N).

absolute maximum ratings

over operating free-air temperature range
(unless otherwise noted)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Operating Free-air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

operating conditions

	MIN	NOM	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5	5.25	V
High-Level Output Current, I_{OH}			−1.0	mA
Low-Level Output Current, I_{OL}			20	mA
Operating Free-Air Temperature, T_A			70	°C

dc electrical characteristics (V_{CC} = +5V, T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		MIN	TYP (Note 2)	MAX	UNITS
V_{IH}	High level Input Voltage			2			V
V_{IL}	Low level Input Voltage					8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1 2	V
V_{OH}	High level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OH} = Max	DM74S151/153/157/158	2 7	3 4		V
			DM74S251/253/257/258	2 4	3 2		V
V_{OL}	Low level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0 8V, I_{OL} = 20 mA				5	V
I_O	Off-state (High impedance-state) Output Current	V_{CC} = Max, V_O = 2 7V to V_O = 0 4V		−50		50	μA
I_I	Input Current at Max Input Voltage	V_{CC} = Max V_I = 5 5V				1	mA
I_{IH}	High level Input Current	V_{CC} = Max, V_I = 2 7V				50	μA
I_{IL}	Low level Input Current	V_{CC} = Max, V_I = 0 5V				−2	mA
I_{OS}	Short-circuit Output Current	V_{CC} = Max		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, All Inputs at +4 5V	DM74S151		45	70	mA
		V_{CC} = Max, All Inputs at +4 5V	DM74S251		55	85	mA
		V_{CC} = Max, All Inputs GND	DM74S153		45	70	mA
		V_{CC} = Max, All Inputs GND	DM74S253		55	70	mA
		V_{CC} = Max, All Inputs Open	DM74S157		50	78	mA
		V_{CC} = Max, All Inputs Open	DM74S257		64	99	mA
		V_{CC} = Max, All Inputs Open	DM74S158		39	61	mA
		V_{CC} = Max, All Inputs Open	DM74S258		56	87	mA

Note 1 For conditions shown as min or max, use the appropriate value specified under recommended operating conditions for the applicable device type

Note 2 All typical values are at V_{CC} = 5V, T_A = 25°C

Note 3 Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second

ac switching characteristics (V_{CC} = +5V, T_A = 25°C)

DM74S151/DM74S251

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DM74S151			DM75S251			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	A, B, or C (4 levels)	Y			12	18		12	18	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	A, B, or C (4 levels)	Y			12	18		13	19 5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	A, B, or C (3 levels)	W			10	15		10	15	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	A, B, or C (3 levels)	W			9	13 5		9	13 5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Y			8	12		8	12	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Data	Y	C_L = 15 pF, R_L = 280Ω, (Note 1)		8	12		8	12	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	W			4 5	7		4 5	7	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Data	W			4 5	7		4 5	7	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Strobe	Y			11	16 5				ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Strobe	Y			12	18				ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Strobe	W			9	13				ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Strobe	W			8 5	12				ns
t_{ZH}	Output Enable Time to High Level	Output Control	Y						13	19 5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	Y	C_L = 50 pF, R_L = 280Ω, (Note 1)					14	21	ns
t_{ZH}	Output Enable Time to High Level	Output Control	W						13	19 5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	W						14	21	ns

Note 1 See load circuits and waveforms on page 4 of this data sheet

ac switching characteristics (con't)

DM74S151/DM74S251

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DM74S151			DM75S251			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{HZ}	Output Disable Time From High Level	Output Control	Y						5 5	8 5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	Y	C_L = 5 pF, R_L = 280Ω, (Note 1)					9	14	ns
t_{HZ}	Output Disable Time From High Level	Output Control	W						5 5	8 5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	W						9	14	ns

DM74S153/DM74S253

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DM74S153			DM74S253			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Y			6	9		6	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data	Y			6	9		6	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select	Y	C_L = 15 pF R_L = 280Ω, (Note 1)		11 5	18		11 5	18	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Select	Y			12	18		12	18	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Strobe	Y			10	15				ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe	Y			9	13 5				ns
t_{ZH}	Output Enable Time to High Level	Output Control	Y						13	19 5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	Y	C_L = 50 pF R_L = 280Ω (Note 1)					14	21	ns
t_{HZ}	Output Disable Time From High Level	Output Control	Y	C_L = 5 pF, R_L = 280Ω, (Note 1)					5 5	8 5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	Y						9	14	ns

DM74S157/DM74S257

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DM74S157			DM74S257			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Y			5	7 5		5	7 5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Data	Y			4 5	6 5		4 5	6 5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Y	C_L = 15 pF, R_L = 280Ω, (Note 1)		9 5	15		8 5	15	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Select	Y			9 5	15				ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe	Y			8 5	12 5				ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Strobe	Y			7 5	12				ns
t_{ZH}	Output Enable Time to High Level	Output Control	Y	C_L = 50 pF, R_L = 280Ω (Note 1)					13	19 5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	Y						14	21	ns
t_{HZ}	Output Disable Time From High Level	Output Control	Y	C_L = 5 pF, R_L = 280Ω, (Note 1)					5 5	8 5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	Y						9	14	ns

DM74S158/DM74S258

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DM74S158			DM74S258			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data	Any			4	6		4	6	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Data	Any			4	6		4	6	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select	Any	C_L = 15 pF R_L = 280Ω (Note 1)		8	12		8	12	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Select	Any			8	12		7 5	12	ns

Note 1 See load circuits and waveforms on page 4 of this data sheet

ac switching characteristics (con't)

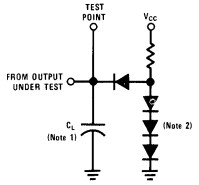
DM74S158/DM74S258

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DM74S158 MIN	DM74S158 TYP	DM74S158 MAX	DM74S258 MIN	DM74S258 TYP	DM74S258 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to High-Level Output	Strobe	Any	C_L = 15 pF, R_L = 280Ω, (Note 1)		6 5	12				ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Strobe	Any			7	12				ns
t_{ZH}	Output Enable Time to High Level	Output Control	Any	C_L = 50 pF, R_L = 280Ω (Note 1)					13	19 5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	Any						14	21	ns
t_{HZ}	Output Disable Time From High Level	Output Control	Any	C_L = 5 pF R_L = 280Ω, (Note 1)					5 5	8 5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	Any						9	14	ns

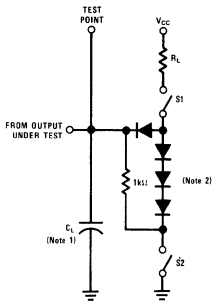
Note 1 See load circuits and waveforms on page 4 of this data sheet

ac load circuits

Bi-state Totem-pole Outputs

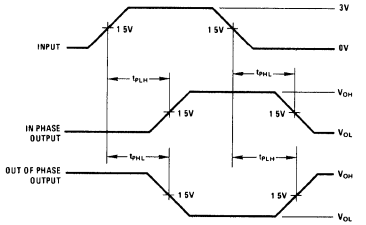


TRI-STATE Outputs

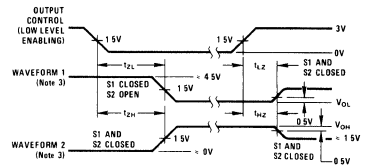


voltage waveforms

Propagation Delay Times

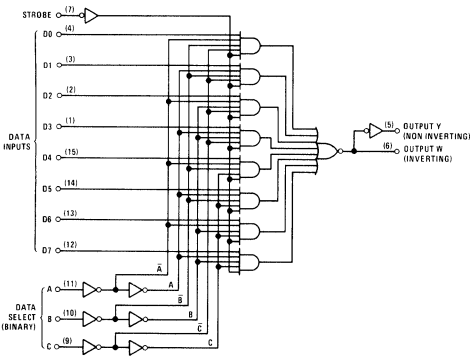


Enable and Disable Times, TRI-STATE Outputs

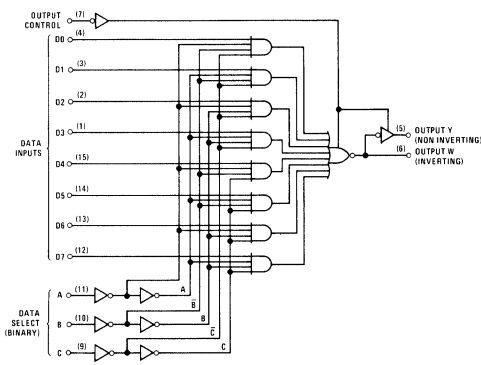


logic diagrams

DM74S151

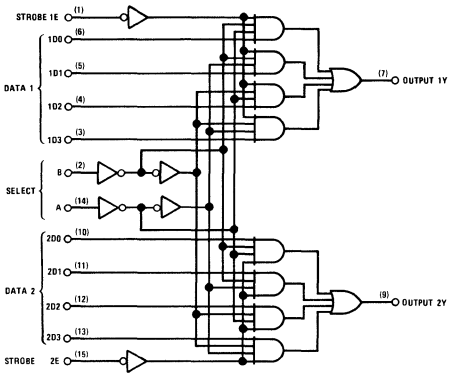


DM74S251

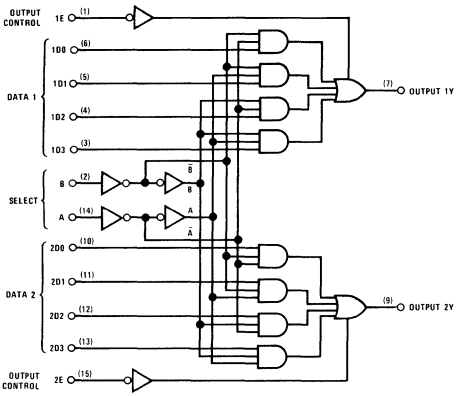


logic diagrams (con't)

DM74S153



DM74S253



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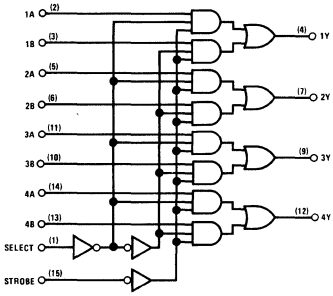

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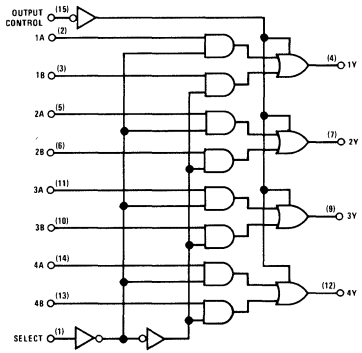

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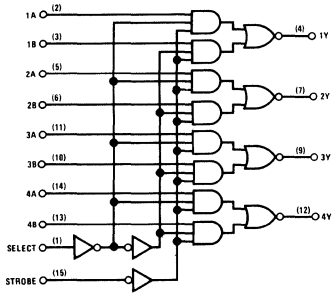

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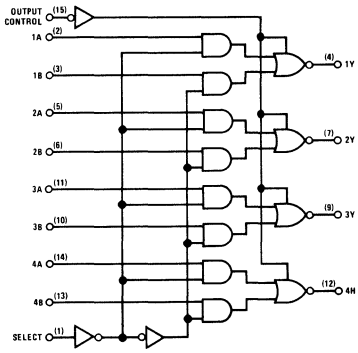


truth tables

DM74S151/DM74S251

INPUTS											OUTPUTS			
SELECT			STROBE OUTPUT CONTROL	DATA								DM74S151		DM74S251	
C	B	A		D0	D1	D2	D3	D4	D5	D6	D7	Y	W	Y	W
X	X	X	H	X	X	X	X	X	X	X	X	L	H	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	L	H	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L	H	L

DM74S153/DM74S253

SELECT INPUTS		STROBE OUTPUT CONTROL	DATA INPUTS				OUTPUTS	
							DM74S153	DM74S253
B	A	G	C0	C1	C2	C3	Y	Y
X	X	H	X	X	X	X	L	Z
L	L	L	L	X	X	X	L	L
L	L	L	H	X	X	X	H	H
L	H	L	X	L	X	X	L	L
L	H	L	X	H	X	X	H	H
H	L	L	X	X	L	X	L	L
H	L	L	X	X	H	X	H	H
H	H	L	X	X	X	L	L	L
H	H	L	X	X	X	H	H	H

DM74S157/DM74S257, DM74S158/DM74S258

SELECT INPUT	STROBE OUTPUT CONTROL	DATA		OUTPUT Y			
		A	B	DM74S157	DM74S158	DM74S257	DM74S258
X	H	X	X	L	H	Z	Z
L	L	L	X	L	H	L	H
L	L	H	X	H	L	H	L
H	L	X	L	L	H	L	H
H	L	X	H	H	L	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Series 930

REFERENCE

The following table references all Physical Dimension Drawings, Waveforms, and Test Circuits for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES										WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)					
		Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Fig.	Pg.
DM930	5-3	3	II										5-4		5-4	
DM932	5-5	3	II										5-6		5-6	
DM933	5-5	3	II										5-6		5-6	
DM935	5-3	3	II										5-4		5-4	
DM936	5-3	3	II										5-4		5-4	
DM937	5-3	3	II										5-4		5-4	
DM944	5-5	3	II										5-6		5-6	
DM945	5-7	3	II										5-9		5-9	
DM946	5-3	3	II										5-4		5-4	
DM948	5-7	3	II										5-9		5-9	
DM949	5-3	3	II										5-4		5-4	
DM957	5-5	3	II										5-6		5-6	
DM958	5-5	3	II										5-6		5-6	
DM961	5-3	3	II										5-4		5-4	
DM962	5-3	3	II										5-4		5-4	
DM963	5-3	3	II										5-4		5-4	
DM1800	5-3	3	II										5-4		5-4	
DM1801	5-3	3	II										5-4		5-4	
DM9093	5-7	3	II										5-9		5-9	
DM9094	5-7	3	II										5-9		5-9	
DM9097	5-7	3	II										5-9		5-9	
DM9099	5-7	3	II										5-9		5-9	

*Order Numbers: use Device No. suffixed with package letter, i.e. DM930N.

5

Series 930

DTL series 930 integrated circuits

general description

The National Semiconductor family of DTL (Diode-Transistor-Logic) is a complete line of compatible monolithic integrated circuits designed to operate at medium speed with medium power dissipation and high fan-out. The DTL family is available in 14-pin, silicone, dual-in-line packages for operation over the 0°C to 75°C temperature range.

The DTL line is composed of a variety of NAND gates that allow complete design flexibility. The gates are available with either 6K pull-up resistors for low power dissipation, or 2K pull-up resistors for increased speed. The gate outputs can be wired together to achieve the wired-OR function.

The NAND gates are complemented with the DM932 and DM957 buffers which provide higher fan-out, the DM944 and DM958 power gates which have an open collector, and the DM933 extender which allows increased fan-in for both buffers and the DM930 and DM961 gates.

The binaries in this family are of the direct coupled master-slave type with direct clear and direct set lines. The dual flip flops include ones with either common or separate clocks.

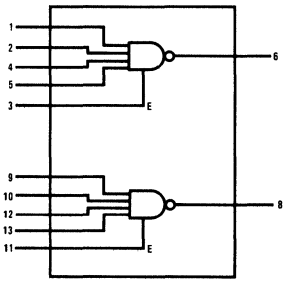
The DM930 series is directly compatible with the TTL devices manufactured by National and can be used in conjunction with them in those portions of a system where speed is not the main consideration.

table of contents

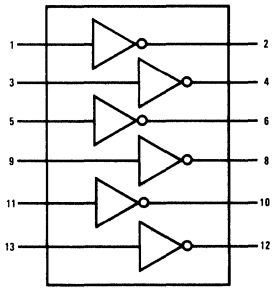
absolute maximum ratings

Power Supply Voltage	
Continuous	8.0V
Pulsed < 1 sec.	12.0V
Input Forward Current	10 mA
Input Reverse Current	1.0 mA
Output Current	
Gates and Binaries	30 mA
Buffers	100 mA
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to 75°C

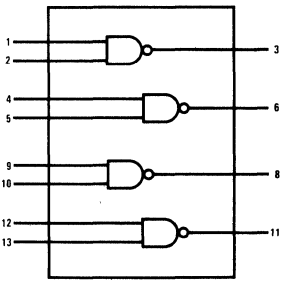
connection/logic diagrams



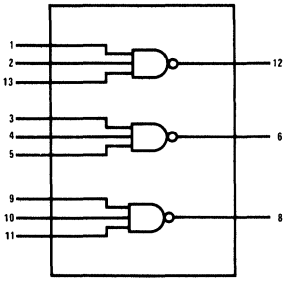
DM930/DM961
DM932/DM944
DM1800/DM1801



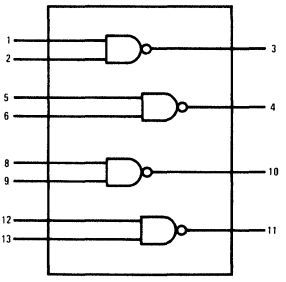
DM935/DM936/DM937



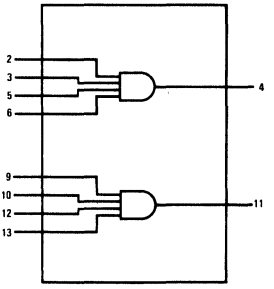
DM946/DM949



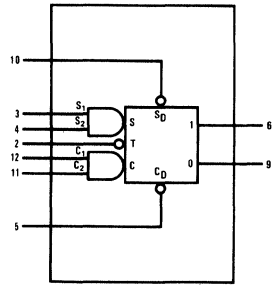
DM962/DM963



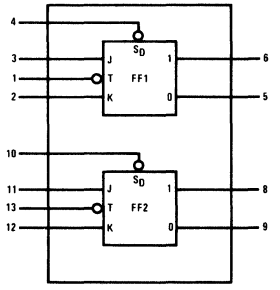
DM957/DM958



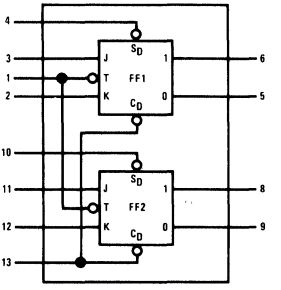
DM933



DM945/DM948



DM9093/DM9094



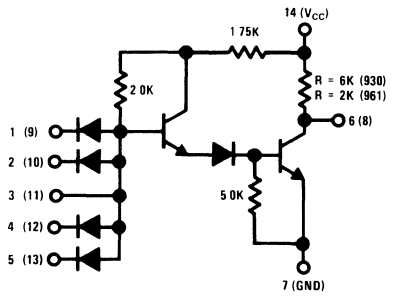
DM9097/DM9099

NAND gates

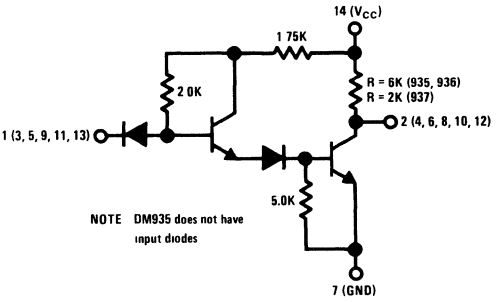
The DM930, DM936, DM946 and DM962 are a variety of NAND gates with a 6K pull-up resistor. The DM961, DM937, DM949 and DM963 are the 2K pull-up versions of the respective gates. The DM935 is a hex inverter similar to the DM936 with the exception that it has no input diodes.

The DM1800 and DM1801 dual 5-input NAND gates are new DTL gates completely compatible with DM930 series gates.

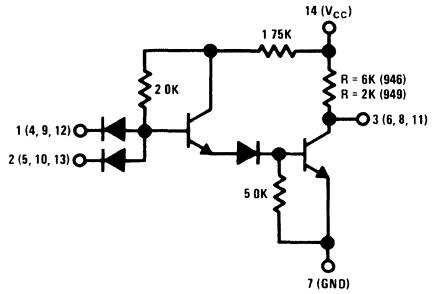
schematic diagrams*



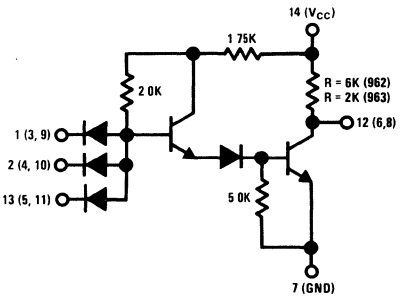
DM930/DM961



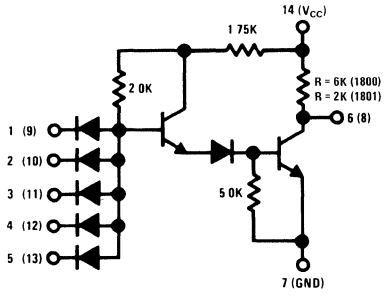
DM935/DM936/DM937



DM946/DM949



DM962/DM963



DM1800/DM1801

*Only one circuit element is shown. Pin connections are given in parentheses for other circuit elements

electrical characteristics

Pin 14 (V_{CC}) = 5 0 volts, Pin 7 = GND, unspecified pins open unless otherwise stated

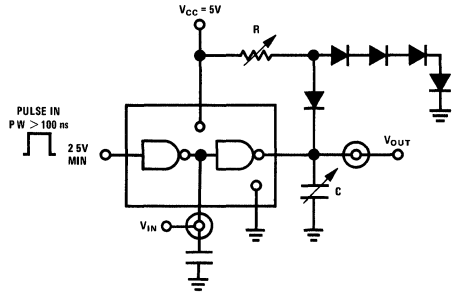
SYMBOL	PARAMETER	PART	CONDITIONS			LIMITS						UNITS
			INPUTS		OUTPUTS	0°C		25°C		75°C		
			INPUT UNDER TEST	OTHER		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Output Low Voltage	All gates	V_{IH}	V_{IH}	I_{OL}	–	0 45	–	0 45	–	0 50	V
V_{OH}	Output High Voltage	All gates* except 935	V_{IL}	V_R	I_{OH}	2 6	–	2 6	–	2 5	–	V
I_R	Input Reverse Current	All except 935	V_R	GND	–	–	5	–	5	–	10	μA
I_F	Input Forward Current	All except 935	V_F	V_R	–	–	–1 40	–	–1 40	–	–1 33	mA
I_{IN}	Input Current	935*	V_F	–	–	–	–1 40	–	–1 40	–	–1 33	mA
I_{CEX}	Output Leakage Current	6k gates 2k gates	GND GND	– –	V_{CEX} V_{CEX}	– –	– –	– –	100 100	– –	– –	μA μA
I_{SC}	Output Short Circuit Current	6k gates 2k gates	GND GND	– –	GND GND	– –	1 30 –	–0 61 –1 85	–1 30 –3 90	– –	–1 25 –	mA mA
I_{PD}	Power Supply Current per gate	6k gates 2k gates	V_R			– –	– –	– –	4 5 9	– –	– –	mA mA
I_{MAX}	Max Supply Current per gate (V_{CC} = 8V)	All	GND	–	–	–	–	–	4	–	–	mA
t_{pd-}	Turn-On Delay	6k gates 2k gates		R = 400Ω, C = 50 pF R = 400Ω, C = 50 pF		– –	– –	10 10	30 30	– –	– –	ns ns
t_{pd+}	Turn On Delay	6k gates 2k gates		R = 3 9kΩ, C = 30 pF R = 3 9kΩ, C = 30 pF		– –	– –	25 15	80 60	– –	– –	ns ns

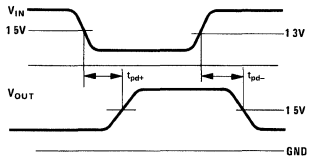
*Use an FD600 diode or equivalent on input under test

test conditions

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	(6k) I_{OL} mA	(6k) I_{OH} mA	(2k) I_{OL} mA	(2k) I_{OH} mA
0°C	2.0	1.2	4.0	0 45	–	12.0	–0.12	11 0	–0.5
+25°C	1.9	1.1	4.0	0.45	5.0	12.0	–0.12	11.0	–0.5
+75°C	1.8	0.95	4.0	0 50	–	11.4	–0.12	10.4	–0.5

switching time test circuit and waveforms



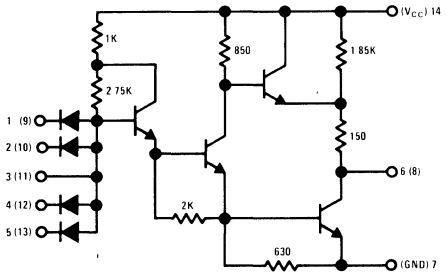


buffers and extender

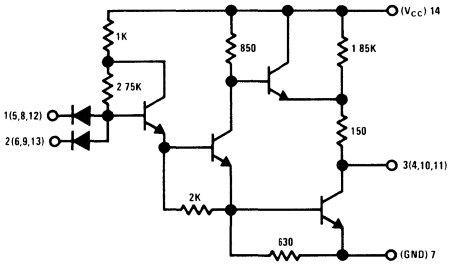
The DM932, DM944, DM957, and DM958 are power gates which are capable of sinking high currents.

The DM933 is an extender element which consists of two four input diode nodes and can be used to extend the fan-in of the DM930, DM961, DM932, and DM944.

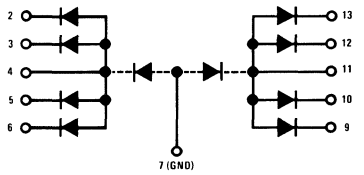
schematic diagrams*



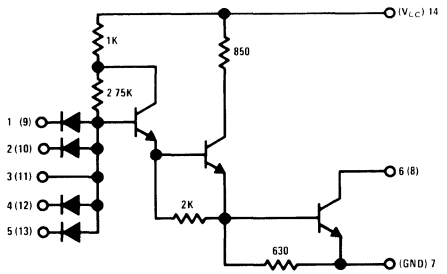
DM932



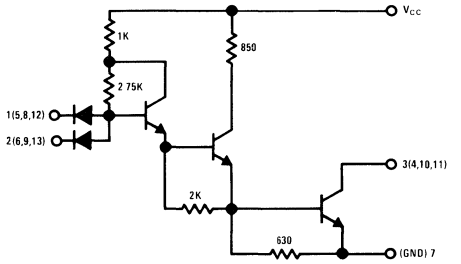
DM957



DM933



DM944



DM958

*Only one circuit element is shown Pin connections are given in parentheses for other circuit elements.

electrical characteristics

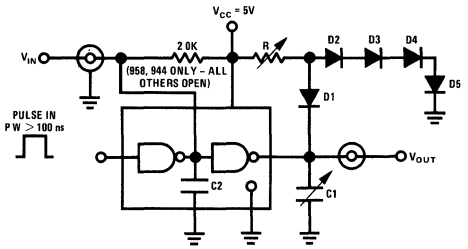
Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND, unspecified pins open unless otherwise stated.

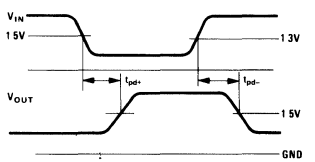
SYMBOL	PARAMETER	PART	CONDITIONS			LIMITS						UNITS
			INPUTS		OUTPUTS	0°C		25°C		75°C		
			INPUT UNDER TEST	OTHER		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OL}	Output Low Voltage	932,944 957,958	V_{IH}	V_{IH}	I_{OL}	–	0.45	–	0.45	–	0 50	V
V_{OH}	Output High Voltage	932,957	V_{IL}	V_R	I_{OH}	2 6	–	2.6	–	2 5	–	V
I_R	Input Reverse Current	932,944 957,958	V_R	GND	–	–	5	–	5	–	10	μA
I_R	Input Reverse Current	933	V_R	GND	GND	–	5	–	5	–	10	μA
I_F	Input Forward Current	932,944 957,958	V_F	V_R	–	–	–1 40	–	–1 40	–	–1 33	mA
V_{FD}	Input Forward Voltage	933	I_{FD}	GND	GND	0 75	0 90	0 68	0 82	0 60	0 75	V
I_{SC}	Output Short Cir. Cur	932,957	GND	–	GND	–16	–	–16	–	–14	–	mA
I_{CEX}	Output Leakage Current	932,957	GND	–	V_{CEX}	–	–	–	100	–	–	μA
		944,958	GND	–	V_{CEX}	–	25	–	100	–	200	μA
I_{PD}	Power Drain Current	932	–	–	–	–	–	–	30 0	–	–	mA
		957	–	–	–	–	–	–	60 0	–	–	mA
		944	–	–	–	–	–	–	22 5	–	–	mA
		958	–	–	–	–	–	–	4.5	–	–	mA
I_{MAX}	Max. Supply Current per gate (V_{CC} = 8V)	932,944 957,958	GND	–	–	–	–	–	4	–	–	mA
t_{pd-}	Turn-On Delay	932 957	R = 150Ω, C = 500 pF		–	–	–	15	40	–	–	ns
		944 958	R = 150Ω, C = 100 pF		–	–	–	10	35	–	–	ns
t_{pd+}	Turn-Off Delay	932 957	R = 510Ω, C = 500 pF		–	–	–	25	80	–	–	ns
		944 958	R = 510Ω, C = 20 pF		–	–	–	15	50	–	–	ns

test conditions

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	I_{FD} mA	V_{CEX} VOLTS	957 932 I_{OL} mA	958 944 I_{OL} mA	957 932 I_{OH} mA
0°C	2 0	1.2	4.0	0 45	–2mA	–	36	40	–2.0
+25°C	1.9	1.1	4.0	0.45	–2mA	5.0	36	40	–2.5
+75°C	1.8	0.95	4.0	0.50	–2mA	–	34	36	–3 0

switching time test circuit and waveforms





NOTE When testing 958 or 944 short diode D1, remove diodes D2, D3, D4 and D5 and add capacitor C2 = 20 pF as shown

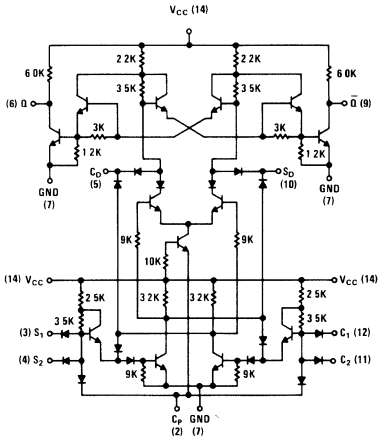
binaries

The DM945 and DM948 are R–S flip flops which can be externally cross coupled to perform in the JK mode. They are of the master slave type with output buffers to provide isolation from the output load These flip flops feature both asynchronous set and clear lines. The DM945 has a 6K pull-up resistor and the DM948 has a 2K pull-up resistor.

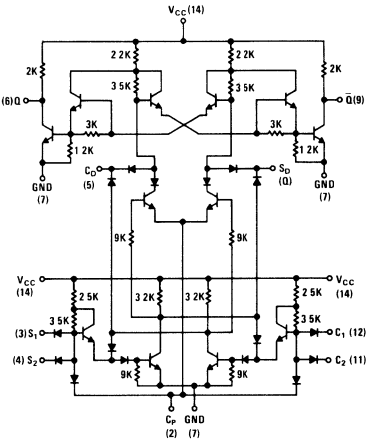
The DM9093 and DM9094 are dual JK flip flops of the DM945 and DM948 variety respectively. Both flip flops have separate clocks and no asynchronous clear lines.

The DM9097 and DM9099 are dual JK flip flops of the DM948 and DM945 variety respectively. Both flip flops have common clocks and both asynchronous set and clear lines.

schematic diagrams



DM945



DM948

truth tables

SYNCHRONOUS TRUTH TABLE

t_n				$t_n + 1$
S_1 Pin 3	S_2 Pin 4	C_1 Pin 12	C_2 Pin 11	Q Pin 6
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 – Low State (more negative)
1 – High State (more positive)
U – Indeterminate State
X – State of the input does not affect the state of the circuit

ASYNCHRONOUS TRUTH TABLE

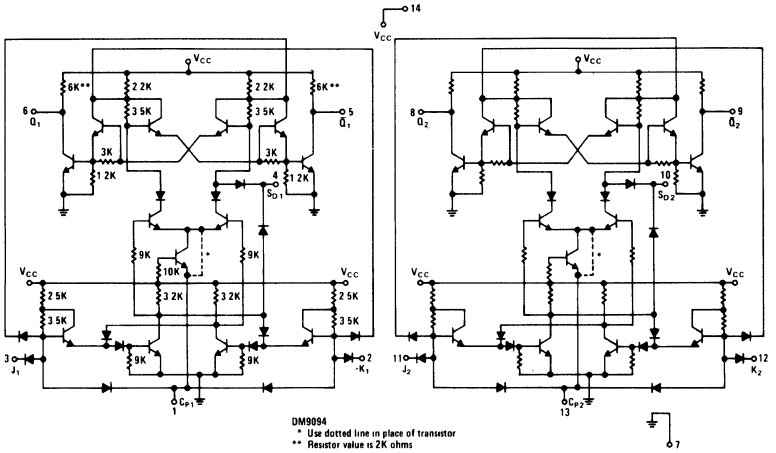
S_D Pin 10	C_D Pin 5	Q Pin 6	$\bar{Q}$ Pin 9
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

J–K TRUTH TABLE

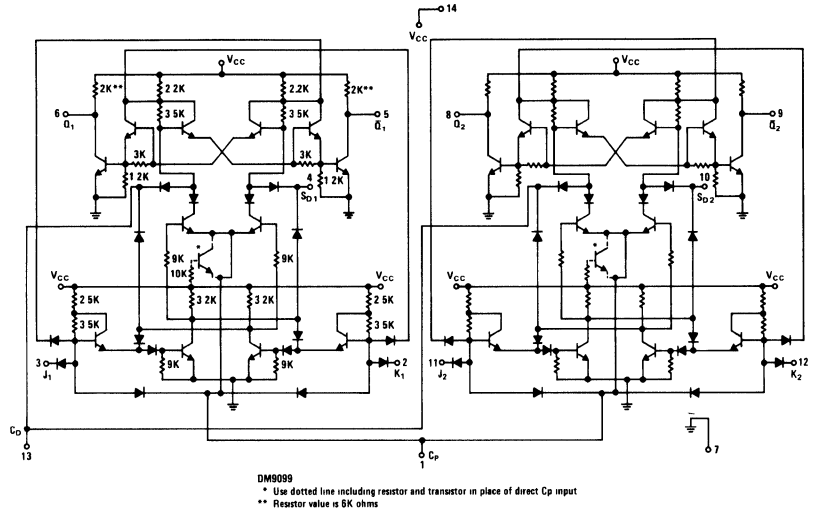
t_n		$t_n + 1$
S_1 Pin 3	C_1 Pin 12	Q Pin 6
0	0	QN
1	0	1
0	1	0
1	1	$\bar{Q}$N

(Connect S_2 to $\bar{Q}$, C_2 to Q) Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs, they are independent of all other inputs

schematic diagrams



DM9093/DM9094 (DM9093 shown)



DM9097/DM9099 (DM9097 shown)

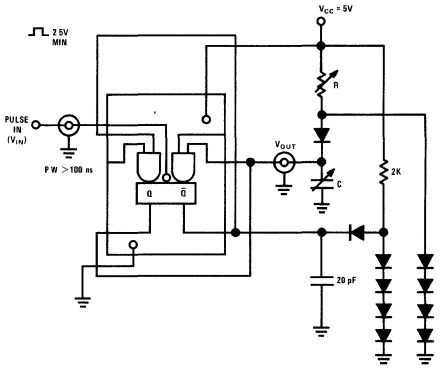
truth table

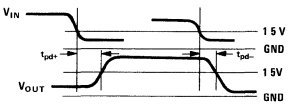
J–K TRUTH TABLE

t_n		$t_n + 1$
S_1 Pin 3	C_1 Pin 12	Q Pin 6
0	0	QN
1	0	1
0	1	0
1	1	$\overline{Q}$N

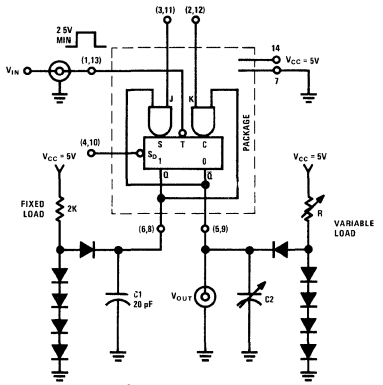
Direct set (S_D) and direct clear (C_D), override the synchronous inputs, they are independent of all other inputs

switching time test circuits and waveforms

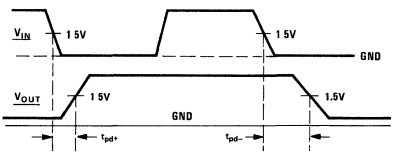




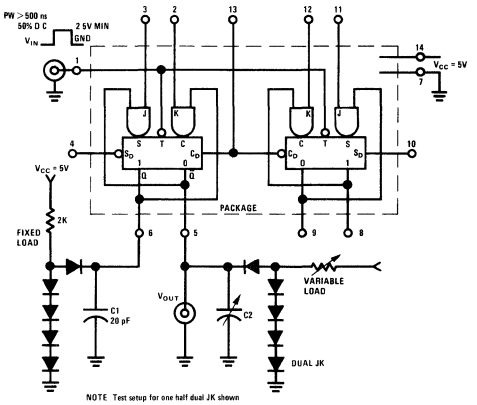
DM945/DM948



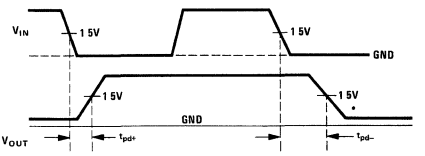
C1 and C2 include probe and jig capacity
All diodes are FD600 or equivalent at +25 C



DM9093/DM9094 (one-half circuit shown)



NOTE Test setup for one half dual JK shown



DM9097/DM9099

DM945/DM948

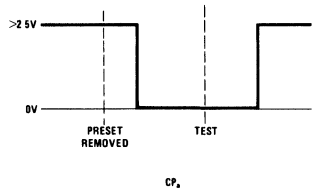
electrical characteristics

Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND

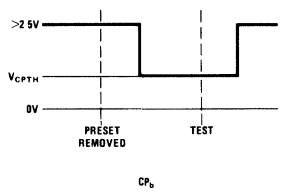
SYMBOL	PARAMETER	PART	CONDITIONS								LIMITS						UNITS	COMMENTS
			C_p	S_1	S_2	C_D	Q	S_D	C_2	C_1	0°C		25°C		75°C			
											MIN	MAX	MIN	MAX	MIN	MAX		
V_{OL}	Output Low Voltage	Both	CP_b	GND	–	–	I_{OL}	–	X	–	–	0.45	–	0.45	–	0.50	V	X=Momentary Gnd
V_{OH}	Output High Voltage (Data Inputs)	945	CP_a	V_{IH}	V_{IH}	X	I_{OH}	–	–	V_{IL}	2.6	–	2.6	–	2.5	–	V	X=Momentary Gnd
		948	CP_a	V_{IH}	V_{IH}	–	I_{OH}	–	–	V_{IL}	2.6	–	2.6	–	2.5	–	V	
V_{OH}	Output High Voltage (Set Reset Inputs)	Both	CP_a	GND	GND	V_{CC}	I_{OH}	V_{IL}	–	–	2.6	–	2.6	–	2.6	–	V	
I_{RD}	Input Reverse Current (Data Inputs)	Both	GND	V_R	–	–	–	–	–	–	–	5.0	–	5.0	–	10.0	μA	
I_R	Input Reverse Current (Set Reset Inputs)	Both	CP_a	GND	GND	V_R	–	V_{CC}	–	–	–	5.0	–	5.0	–	10.0	μA	
I_{RC}	Input Reverse Current (Clock Input)	Both	V_R	GND	GND	GND	–	–	–	–	–	30	–	30	–	40	μA	V_{AC} = 4.0 volts
I_{FD}	Input Forward Current (Data Inputs)	Both	V_R	V_F	V_R	–	–	–	–	–	–	–0.95	–	–0.95	–	–0.90	mA	
I_F	Input Forward Current (Set Reset Inputs)	Both	–	–	–	V_F	–	–	GND	GND	–	–2.8	–	–2.8	–	–2.67	mA	
I_{FC}	Input Forward Current (Clock Input)	945	V_F	–	–	V_{IL}	–	–	–	–	–	–2.8	–	–2.8	–	–2.66	mA	
		948	V_F	–	–	V_{IL}	–	–	–	–	–	–2.8	–	–2.8	–	–2.67	mA	
I_{CEX}	Output Leakage Current	Both	–	–	–	–	V_{CEX}	GND	–	–		–	–	100	–	–	μA	
I_{SC}	Short Circuit Current	945	CP_a	–	–	GND	GND	GND	–	–	–0.59	–1.41	–0.59	–1.41	–0.55	–1.38	mA	
		948	CP_a	–	–	GND	GND	GND	–	–	–1.77	–4.2	–1.77	–4.2	–1.60	–4.0	mA	
I_{PD}	Power Drain Current	945	V_{CC}	–	–	–	–	–	–	–	–	–	–	14	–	–	mA	
		948	V_{CC}	–	–	–	–	–	–	–	–	–	–	17	–	–	mA	
I_{MAX}	Max Supply Current (V_{CC} = 8V)	945	–	GND	GND	GND	–	GND	GND	GND	–	–	–	18	–	–	mA	
		948	–	GND	GND	GND	–	GND	GND	GND	–	–	–	23	–	–	mA	
t_{pd-}	Turn–On Delay	945	R = 330Ω, C = 50 pF								–	–	15	55	–	–	ns	
		948	R = 330Ω, C = 50 pF								–	–	15	55	–	–	ns	
t_{pd+}	Turn–Off Delay	945	R = 2.0kΩ, C = 30 pF								–	–	25	100	–	–	ns	
		948	R = 2.0kΩ, C = 30 pF								–	–	25	75	–	–	ns	

test conditions

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_F VOLTS	V_R VOLTS	945(6K) V_{CPTH} VOLTS	948(2K) V_{CPTH} VOLTS	945(6K) I_{OL} mA	948(2K) I_{OL} mA	945(6K) I_{OH} mA	948(2K) I_{OH} mA	V_{CEX} VOLTS
0° C	2.0	1.2	0.45	4.0	1.15	1.30	16.8	15.4	–0.12	–0.5	–
+25° C	1.9	1.1	0.45	4.0	0.95	1.15	16.8	15.4	–0.12	–0.5	5.0
+75° C	1.8	0.95	0.50	4.0	0.65	0.85	16.0	14.6	–0.12	–0.5	–



CP_a



CP_b

DM9093/DM9094/DM9097/DM9099

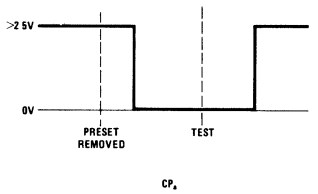
electrical characteristics

Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND

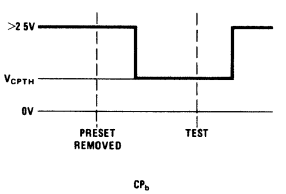
SYMBOL	PARAMETER	PART	CONDITIONS	LIMITS						UNITS
				0°C		+25°C		−75°C		
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Output Low Voltage	All	I_{OL} on output under test	–	0.45	–	0.45	–	0.50	V
V_{OH}	Output High Voltage	All	I_{OH} on output under test	2.6	–	2.6	–	2.5	–	V
I_{SC}	Output Short Circuit Current	2k	GND output under test	−1.77	−4.2	−1.77	−4.2	−1.60	−4.0	mA
		6k	GND output under test	−0.59	−1.41	−0.59	−1.41	−0.55	−1.38	mA
I_{FD}	Input Forward Current (Data Input)	All	V_F on input under test V_R on other inputs	–	−0.95	–	−0.95	–	−0.90	mA
I_{FC}	Input Forward Current (Clock and Direct Clear Inputs)	9097 9099	V_F on input under test V_R on other inputs	–	−5.6	–	−5.6	–	−5.34	mA
I_{FC}	Input Forward Current (Clock Input)	9093 9094	V_F on input under test V_R on others	–	−2.8	–	−2.8	–	−2.67	mA
I_F	Input Forward Current (Direct Set Inputs)	All	V_F on input under test V_R on other inputs	–	−2.8	–	−2.8	–	−2.67	mA
I_R	Input Reverse Current (All except clock inputs and Direct clear input on 9097, 9099)	All	V_R on input under test GND on other inputs	–	5.0	–	5.0	–	10.0	μA
I_R	Input Reverse Current Direct (Clear Input)	9097 & 9099	V_R on input under test GND on other inputs	–	10	–	10	–	20	μA
I_R	Input Reverse Current (Clock Inputs)	9093 & 9094	V_R on input under test GND on other inputs	–	20	–	20	–	30	μA
		9097 & 9099	V_R on input under test GND on other inputs	–	40	–	40	–	60	μA
I_{PD}	Power Drain Current	9093 9094 9099 9097	Inputs Open Inputs Open Inputs Open Inputs Open	–	– – – –	– – – –	28 34 28 34	– – – –	– – – –	mA mA mA mA
I_{MAX}	Max. Supply Current (V_{CC} = 8V)	9093 9099 9094 9097	GND all inputs	– –	– –	– –	36 45	– –	– –	mA mA
t_{pd-}	Turn–On Delay	All	R = 330Ω, C = 50 pF	–	–	15	55	–	–	ns
t_{pd+}	Turn–Off Delay	6k 2k	R = 2k, C = 30 pF R = 2k, C = 30 pF	– –	– –	25 25	100 75	– –	– –	ns ns

test conditions

TEMP.	(6k) I_{OL} mA	(2k) I_{OL} mA	(6k) I_{OH} mA	(2k) I_{OH} mA	V_F VOLTS	V_R VOLTS	V_{IH} VOLTS	V_{IL} VOLTS	9093-9 6K V_{CPTH}	9094-7 2K V_{CPTH}
0°C	16.8	15.4	−0.12	−0.5	0.45	4.0	2.0	1.2	1.15	1.30
+25°C	16.8	15.4	−0.12	−0.5	0.45	4.0	1.9	1.1	0.95	1.15
+75°C	16.0	14.6	−0.12	−0.5	0.50	4.0	1.8	0.95	0.65	0.85



CP_a



CP_b

Series 9000

REFERENCE

The following table references all Physical Dimension Drawings, Waveforms, and Test Circuits for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
		Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type		Fig.	Pg.	Fig.	Pg.
DM9002C	6-1	3	II	11	IV	J											
DM9003C	6-1	3	II	11	IV	J											
DM9004C	6-1	3	II	11	IV	J											
DM9005C	6-1	3	II	11	IV	J											
DM9006C	6-1	3	II	11	IV	J											
DM9008C	6-1	3	II	11	IV	J											
DM9009C	6-1	3	II	11	IV	J											
DM9012C	6-1	3	II	11	IV	J											
DM9016C	6-1	3	II	11	IV	J											
DM8300	6-4	5	II	12	IV	J	19	V	W					36	11-17	9	11-2
DM9300	6-4	5	II	12	IV	J	19	V	W					36	11-17	9	11-2
DM8301	6-6	5	II	12	IV	J	19	V	W					5	11-5	1	11-1
DM9301	6-6	5	II	12	IV	J	19	V	W					5	11-5	1	11-1
DM8309	6-8	5	II	12	IV	J	19	V	W					39	11-18	1	11-1
DM9309	6-8	5	II	12	IV	J	19	V	W					39	11-18	1	11-1
DM8312	6-10	5	II	12	IV	J	19	V	W					40	11-18	1	11-1
DM9312	6-10	5	II	12	IV	J	19	V	W					40	11-18	1	11-1
DM8322	6-12	5	II	12	IV	J	19	V	W					37	11-17	14	11-4
DM9322	6-12	5	II	12	IV	J	19	V	W					37	11-17	14	11-4
DM8601	6-14	3	II	11	IV	J	18	V	W					38	11-17	8	11-2
DM9601	6-14	3	II	11	IV	J	18	V	W					38	11-17	8	11-2

*Order Numbers: use Device Number suffixed with package letter, i.e., DM9002CN.

Series 9000

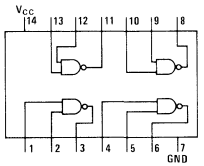
DM9002C quad 2-input NAND gate
DM9003C triple 3-input NAND gate
DM9004C dual 4-input NAND gate
DM9005C dual AND-OR-INVERT gate/expander
DM9006C dual 4-input expander
DM9008C 2-2-2-3-input AND-OR- INVERT gate
DM9009C dual 4-input NAND gate/buffer
DM9012C quad 2-input NAND gate(open collector)
DM9016C hex inverter

general description

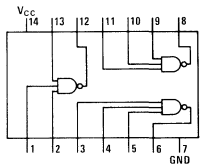
The above gate functions are commercial temperature range (0°C to +75°C) plug-in equivalents for the DM9000 Series devices. The "C" designation is used in place of the earlier "–59X" suffix.

connection diagrams (Dual-In-Line and Flat Packages)

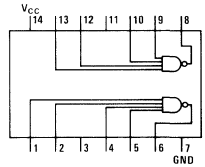
DM9002C



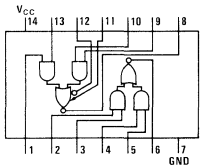
DM9003C



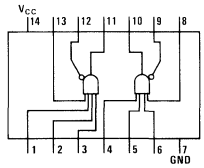
DM9004C



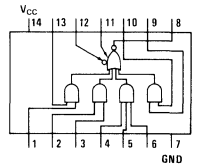
DM9005C



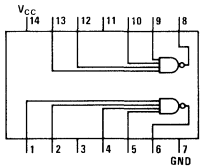
DM9006C



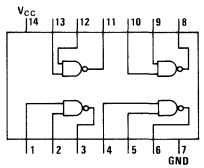
DM9008C



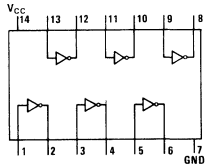
DM9009C



DM9012C



DM9016C



absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

DM90002C, DM9003C, DM9004C, DM9012C, DM9016C (Note 1)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4 75V	1 6		V
Logical "0" Input Voltage	V_{CC} = 4 75V		85	V
Logical "1" Output Voltage Except DM9012C	V_{CC} = 4 75V, I_{OUT} = −1 2 mA, V_{IN} = 85V	2 4		V
Logical "0" Output Voltage	V_{CC} = 4 75V, I_{OUT} = +14 1 mA, V_{IN} = 1 6V V_{CC} = 5 25V, I_{OUT} = +16 mA, V_{IN} = 5 25V		45 45	V V
Logical "1" Output Current (DM9012C)	V_{CC} = 4 75V, V_{OUT} = 5 5V, V_{IN} = .85V		250	µA
Logical "1" Input Current	V_{CC} = 5 25V, V_{IN} = 4.5V		60	µA
Logical "0" Input Current	V_{CC} = 5 25V, V_{IN} = 45V V_{CC} = 4 75V, V_{IN} = 45V		−1 6 −1 41	mA mA
Supply Current — Logical "0" Output (each gate)	V_{CC} = 5 0V		6 1	mA
Supply Current — Logical "1" Output (each gate)	V_{CC} = 5 0V		1 7	mA
Propagation Delay Time to a Logical "1" Except DM9012C	V_{CC} = 5 0V, C_L = 15 pF, T_A = 25°C	3 0	13	ns
DM9012C	V_{CC} = 5 0V, C_L = 15 pF, R_L = 4 kΩ	3 0	45	ns
Propagation Delay Time to a Logical "0" Except DM9012C	V_{CC} = 5 0V, C_L = 15 pF, T_A = 25°C	3 0	15	ns
DM9012C	V_{CC} = 5 0V, C_L = 15 pF, R_L = 400Ω, T_A = 25°C	3 0	15	ns

DM9005C, DM9006C, DM9008C (Note 1)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4 75V	1 6		V
Logical "0" Input Voltage	V_{CC} = 4 75V		85	V
Logical "1" Output Voltage	V_{CC} = 4 75V, I_{OUT} = −1 2 mA, V_{IN} = 85V	2 4		V
Logical "0" Output Voltage	V_{CC} = 4 75V, I_{OUT} = 14 1 mA, V_{IN} = 1 6V		45	V
	V_{CC} = 4 75V, I_{OUT} = 16 mA, V_{IN} = 5 25V		45	V
Logical "1" Input Current				
Except DM9005C Non-Extendable Gate	V_{CC} = 4 75V, V_{IN} = 4 5V		90	µA
DM9005C Non-Extendable Gate	V_{CC} = 4 75V, V_{IN} = 4 5V		60	µA
Logical "0" Input Current				
Except DM9005C Non-Extendable Gate	V_{CC} = 4 75V, V_{IN} = 45V		−2 12	mA
	V_{CC} = 5 25V, V_{IN} = 45V		−2 4	mA
DM9005C Non-Extendable Gate	V_{CC} = 4 75V, V_{IN} = 45V		−1 41	mA
	V_{CC} = 5 25V, V_{IN} = 45V		−1 6	mA
Supply Current — Logical "0" Output				
DM9005C Non-Extendable Gate	V_{CC} = 5 0V		7 7	mA
DM9005C Extendable Gate	V_{CC} = 5 0V		13.6	mA
DM9008C	V_{CC} = 5 0V		17.7	mA

Note 1: All devices are guaranteed across the 0°C to +75°C temperature range except where specified differently.

electrical characteristics (con't)

DM9005C, DM9006C, DM9008C (con't)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Supply Current — Logical "1" Output				
DM9005C Non-Extendable Gate	V_{CC} = 5 0V		3 4	mA
DM9005C Extendable Gate	V_{CC} = 5 0V		5 1	mA
DM9008C	V_{CC} = 5 0V		10 2	mA
ΔSupply Current				
Additional Supply Current when one DM9006C Extender is connected to a DM9005C Gate in the Logical "0" State	V_{CC} = 5 0V		2 05	mA
Additional in the Logical "1" State	V_{CC} = 5 0V		2 54	mA
Propagation Delay Time to a Logical "1"	V_{CC} = 5 0V, C_L = 15 pF, T_A = 25°C			
DM9005C Non-Extendable Gate Only		3 0	12	ns
DM9005C Extendable Gate, and DM9008C	C_N = 5 0 pF	3 0	15	ns
DM9006C (Note 2)		-2 0	4 0	ns
Propagation Delay Time to a Logical "0"	V_{CC} = 5 0V, C_L = 15 pF, T_A = 25°C			
DM9005C Non-Extendable Gate Only		3 0	14	ns
DM9005C Extendable Gate, and DM9008C	C_N = 5 0 pF	3 0	12	ns
DM9006C (Note 2)		-2 0	4 0	ns

DM9009C (Note 1)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4 75V	1 6		V
Logical "0" Input Voltage	V_{CC} = 4 75V		85	V
Logical "1" Output Voltage	V_{CC} = 4 75V, I_{OUT} = -3 6 mA, V_{IN} = 85V	2 4		V
Logical "0" Output Voltage	V_{CC} = 4 75V, I_{OUT} = 42 3 mA, V_{IN} = 1 6V		45	V
	V_{CC} = 5 25V, I_{OUT} = 48 mA, V_{IN} = 5 25V		45	V
Logical "1" Input Current	V_{CC} = 5 25V, V_{IN} = 4 5V		120	μA
Logical "0" Input Current	V_{CC} = 5 25V, V_{IN} = 45V		-3 2	mA
	V_{CC} = 4 75V, V_{IN} = 45V		-2 82	mA
Supply Current — Logical "0" Output	V_{CC} = 5 0V, V_{IN} = 4 5V		14 6	mA
Supply Current — Logical "1" Output	V_{CC} = 5 0V, V_{IN} = GND		3 4	mA
Propagation Delay to a Logical "1"	V_{CC} = 5 0V, C_L = 15 pF, T_A = 25°C	3 0	17	ns
Propagation Delay to a Logical "0"	V_{CC} = 5 0V, C_L = 15 pF, T_A = 25°C	2 0	13	ns

Note 1: All devices are guaranteed across the 0°C to +75°C temperature range except where specified differently

Note 2: The DM9006C is tested by measuring its propagation delay through the DM9005C The delay readings shall not exceed the DM9005C reading by the specified amount

6

Series 9000

DM9300/DM8300(SN54195/SN74195) 4-bit shift register

general description

The DM9300/DM8300 is a 4-bit multi-function shift register designed to work at typical speeds of 25 MHz.

It features a common asynchronous Reset input which resets the register independent of any other input In addition, the J and $\overline{K}$ inputs to the first flip flop enable greater flexibility in the operation of the register (See truth table)

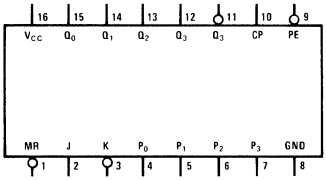
The $\overline{PE}$ (Parallel Enable) control allows information to be entered from the parallel inputs or be shifted right When the $\overline{PE}$ input is in the logical "0" state, the information on the parallel inputs will be entered into the flip flops on the subsequent clock pulse A logical "1" level on the PE control will allow shifting to the right

The outputs change state on the positive-going transition of the clock input

This register is completely compatible with Series 54/74 and CCSL devices Input diode clamps are provided for additional system reliability

connection diagram

Dual-In-Line and Flat Package



truth table

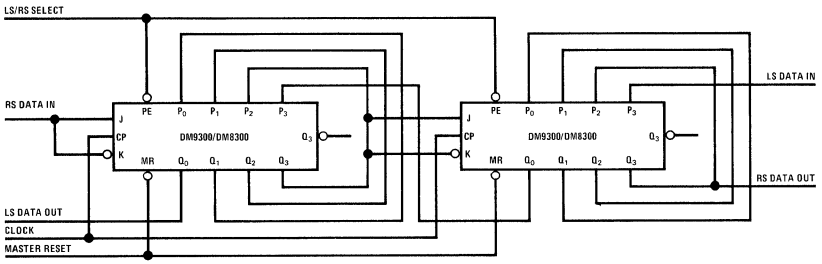
J	$\overline{K}$	Q_0 at t_{n+1}
0	0	0
0	1	Q_0 at t_n (no change)
1	0	$\overline{Q}_0$ at t_n (toggle)
1	1	1

($\overline{PE}$ = logical "1", $\overline{MR}$ = logical "1")

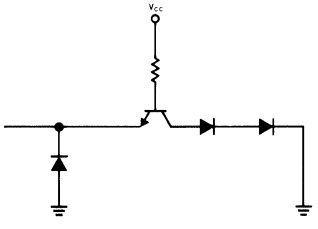
typical application

Eight Bit Left/Right Shift Register

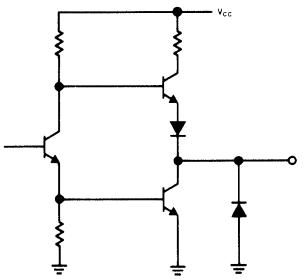
This register shifts left or right on each shift clock, depending upon the condition of the LS/RS select input If this input is high, right shift occurs and if low, left shift occurs



equivalent circuits



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
(Q_0 Q_1 Q_2 Q_3 AND $\overline{Q}_3$)

absolute maximum ratings

V_{CC} Voltage Range		-.5V to 7V
Input Voltage Range		-.5V to 5.5V
Output Voltage (Logical "1" state)		5.5V
Operating Temperature Range	DM9300	-55°C to +125°C
	DM8300	0°C to 75°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C MIN	LIMITS -55°C MAX	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5V, I_{OH} = -0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5V, I_{OL} = 9.6 mA V_{CC} = 4.5V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.10	-1.6		-1.6	mA	V_{CC} = 5.5V, V_F = 0.4V
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3		-1.24		-0.97	-1.24		-1.24	mA	V_{CC} = 4.5V
I_R	Input Leakage Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.5V, V_R = 4.5V

electrical characteristics (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN	LIMITS 0°C MAX	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +75°C MIN	LIMITS +75°C MAX	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75V, I_{OH} = -0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25V, I_{OL} = 9.6 mA
V_H	Input High Voltage	1.9		1.8			1.6		Volts	V_{CC} = 4.75V, I_{OL} = 8.5 mA Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.0	-1.6		-1.6	mA	V_{CC} = 5.25V
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3		-1.41		-0.9	-1.41		-1.41	mA	V_{CC} = 4.75V, V_F = 0.45V
I_R	Input Leakage Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.25V, V_R = 4.5V

switching characteristics (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		12	22	ns	V_{CC} = 5.0V, C_L = 15 pF
t_{pd-}	Turn On Delay		19	26	ns	(See Figs 1 & 2a)
f_{sr}	Shift Right Frequency	30	38		MHz	V_{CC} = 5.0V, C_L = 15 pF (See Figs 1 & 2c)
$\overline{CP}_{pw}$	Clock Pulse Width	17	11		ns	
t_s	Set-up Time	30	13		ns	V_{CC} = 5.0V
t_r	Release Time		10	0	ns	C_L = 15 pF
$t_s(\overline{PE})$	Set up Time for $\overline{PE}$	45	20		ns	(See Figs 2a & 2b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		17	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		28		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		13		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

SET UP TIME t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip flop(s) to respond

RELEASE TIME t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip flop(s) not to respond

RECOVERY TIME FOR $\overline{MR}$ $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip flop(s) to respond to the clock

Series 9000

DM9301/DM8301 BCD-to-decimal decoder

general description

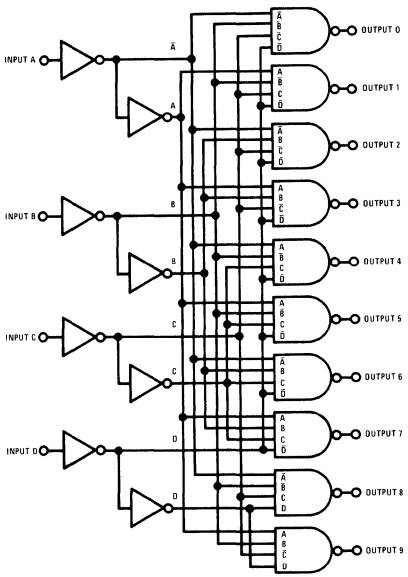
The DM9301/DM8301 utilizes Series 54/74 compatible circuitry to decode a four-bit BCD number to one-of-ten decimal outputs. These ten decimal outputs are capable of driving 10 standard TTL loads each.

The decoding logic is designed such that when binary numbers between 10 and 15 are applied to the inputs, no outputs are enabled.

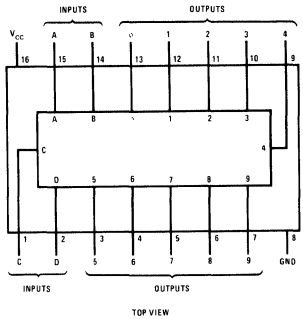
features

- 125 mW typical power dissipation
- 20 ns typical propagation delay
- Clamp diodes on inputs

logic and connection diagrams



Dual-In-Line and Flat Package



logic table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DM9301	−55°C to +125°C
DM8301	0°C to +70°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITION		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM9301 DM8301	V_{CC} = 4 5V V_{CC} = 4 75V		2 0			V
Logical "0" Input Voltage	DM9301 DM8301	V_{CC} = 4 5V V_{CC} = 4 75V				0 8	V
Logical "1" Output Voltage	DM9301 DM8301	V_{CC} = 4 5V V_{CC} = 4 75V	I_{OUT} = −600 μA	2 4			V
Logical "0" Output Voltage	DM9301 DM8301	V_{CC} = 4 5V V_{CC} = 4 75V	I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	DM9301 DM8301	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 4 5			40	μA
Logical "1" Input Current	DM9301 DM8301	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 5 5V			1	mA
Logical "0" Input Current	DM9301 DM8301	V_{CC} = 5 5V V_{CC} = 5 25V	V_{IN} = 0 4V		−1 0	−1 6	mA
Input Clamp Diode (All Inputs)	DM9301 DM8301	V_{CC} = 5 5V V_{CC} = 5 25V	I_{IN} = −12 mA		−1 0	−1 5	V
Output Short Circuit Current (Note 3)	DM9301 DM8301	V_{CC} = 5 5V V_{CC} = 5 25V	V_{OUT} = 0V	−20 −18	−32	−55	mA
Power Supply Current	DM9301 DM8301	V_{CC} = 5 5V V_{CC} = 5 25V			25	41	mA
Propagation Delay Time to a Logical "0"		V_{CC} = 5 0V, T_A = 25°C, C_{OUT} = 50 pF, F O = 10		8	19	30	ns
Propagation Delay Time to a Logical "1"		V_{CC} = 5 0V, T_A = 25°C, C_{OUT} = 50 pF, F O = 10		8	20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Min/max limits apply across the guaranteed operating temperature range −55°C to +125°C for DM9301 and 0°C to 70°C for the DM8301 unless otherwise specified All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output may be shorted at a time

Series 9000

DM9309/DM8309 dual 4-input multiplexer

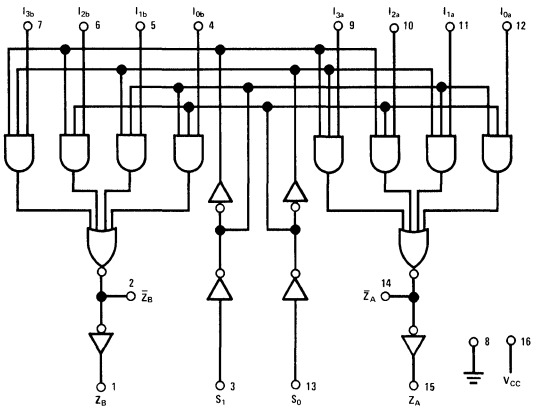
general description

The DM9309/DM8309 is a dual four-input digital multiplexer. It consists of two multiplexing circuits with common input select data logic. Each circuit contains four inputs and fully buffered complementary outputs.

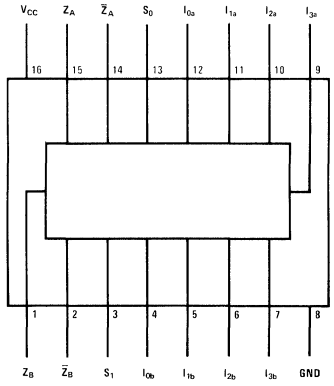
features

- Series 54/74 T^2L and DTL compatible
- Input clamping diode
- Fully buffered complementary outputs
- Fan-out of 10

logic and connection diagrams



Dual-In-Line and Flat Package



truth table

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0A}	I_{1A}	I_{2A}	I_{3A}	Z_A	$\overline{Z}_A$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0B}	I_{1B}	I_{2B}	I_{3B}	Z_B	$\overline{Z}_B$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Irrelevant

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM9309	4 5	5 5	V
DM8309	4 75	5 25	V
Temperature (T_A)			
DM9309	−55	+125	°C
DM8309	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 8V, I_{OH} = −800 μA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 8V, I_{OL} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 4V			−1 6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	−30 −27		−85	mA
Supply Current	V_{CC} = Max		27	44	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Data to Z, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		24	35	ns
Propagation Delay to a Logical "0" from Data to $\overline{Z}$, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		10	15	ns
Propagation Delay to a Logical "1" from Data to Z, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		20	28	ns
Propagation Delay to a Logical "1" from Data to $\overline{Z}$, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		15	22	ns
Data Select to Z					
t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		30	45	ns
t_{pd0}			25	37	ns
Data Select to $\overline{Z}$					
t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		17	25	ns
t_{pd0}			21	31	ns

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM9309 and across the 0°C to 70°C range for the DM8309 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3: Only one output at a time should be shorted

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Series 9000

DM9312/DM8312 8-input multiplexer

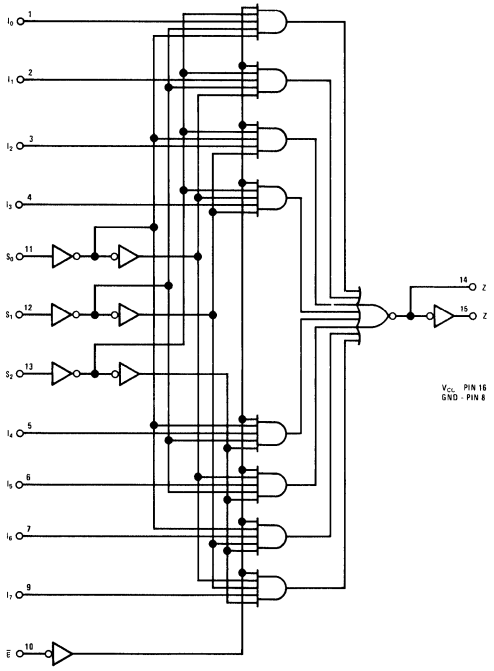
general description

The DM9312/DM8312 is an eight-input digital multiplexer which provides in one package the ability to select one bit of data from up to eight sources. When the enable input is taken to a logical "0", it will enable the multiplexer to function.

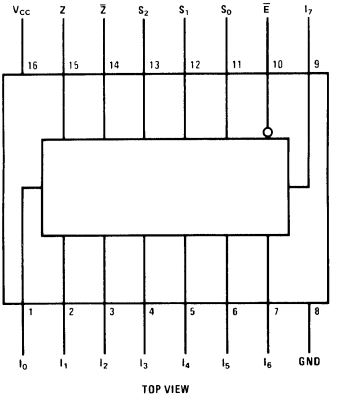
features

- Series 54/74 T²L and DTL compatible
- Input clamping diodes
- Selects one-of-eight data sources
- Fan-out of 10
- Fully buffered complementary outputs

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

truth table

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High Voltage Level X = Irrelevant
L = Low Voltage Level

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5 5V
Output Voltage	5 5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM9312	4 5	5.5	V
DM8312	4 75	5 25	V
Temperature (T_A)			
DM9312	−55	+125	°C
DM8312	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 8V, I_{OH} = −800 μA	2 4			V
Logical "1" Output Current	V_{CC} = Max, V_{OUT} = 5 5V, V_{IN} = 0V			250	μA
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 8V, I_{OL} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 4V			−1 6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max	−30 −27		−85	mA
Supply Current	V_{CC} = Max		33	44	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0" from Data to Z, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		23	34	ns
Propagation Delay to a Logical "0" from Data to $\overline{Z}$, t_{pd0}	V_{CC} = 5 0V, T_A = 25°C		9	14	ns
Propagation Delay to a Logical "1" from Data to Z, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		19	28	ns
Propagation Delay to a Logical "1" from Data to $\overline{Z}$, t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		15	23	ns
Data Select to Z					
t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		29	43	ns
t_{pd0}			25	37	ns
Data Select to $\overline{Z}$					
t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		20	30	ns
t_{pd0}			18	27	ns
Enable to Z					
t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		28	42	ns
t_{pd0}			25	37	ns
Enable to $\overline{Z}$					
t_{pd1}	V_{CC} = 5 0V, T_A = 25°C		17	25	ns
t_{pd0}			18	27	ns

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM9312 and across the 0°C to 70°C range for the DM8312 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

Note 3. Only one output at a time should be shorted

Series 9000

DM9322/DM8322 quad 2-input multiplexer

general description

The DM9322/DM8322 consists of four 2-input multiplexers with common input select logic and common output disable circuitry. It allows two groups of four bits each to be multiplexed to four parallel outputs. When the Enable input is at the logical "0" level the outputs reflect information on the selected inputs. However, when a logical "1" is applied, the outputs assume the logical "0" level.

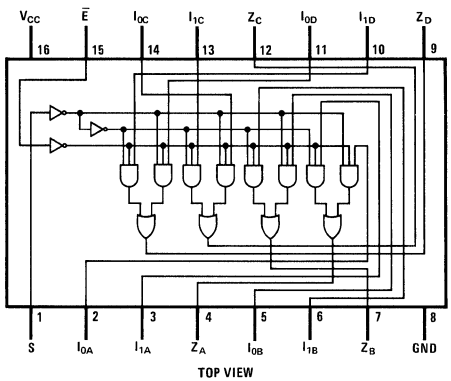
The DM9322/DM8322 is pin compatible and functionally compatible with the FSC9322 and the SN54157/SN74157. Features of the device are:

features

- Typically 10 ns from data to output
- Power dissipation 150 mW typ
- Pin compatible with FSC9322 and SN54157/SN74157
- Diode clamped inputs
- Available in either cavity or molded dual-in-line package

logic and connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

ENABLE $\bar{E}$	SELECT S	INPUT I_0	INPUT I_1	OUTPUT Z_X
1	X	X	X	0
0	1	X	0	0
0	1	X	1	1
0	0	0	X	0
0	0	1	X	1

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM9322	−55°C to 125°C
	DM8322	0°C to 70°C
Storage Temperature Range		−55°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM9322	V_{CC} = 4.5V		2.0			V
	DM8322	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM9322	V_{CC} = 4.5V				0.8	V
	DM8322	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM9322	V_{CC} = 4.5V	I_{OUT} = −1.2 mA V_{IN} = 2V	2.4			V
	DM8322	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM9322	V_{CC} = 4.5V	I_{OUT} = 12.4 mA V_{IN} = 0.8V			0.4	V
	DM8322	V_{CC} = 4.75V	I_{OUT} = 14.1 mA			0.45	
	DM9322	V_{CC} = 5.5V	I_{OUT} = 16 mA V_{IN} = 0.8V			0.4	V
	DM8322	V_{CC} = 5.25V	I_{OUT} = 16 mA			0.45	
Logical "1" Input Current	DM9322	V_{CC} = 5.5V	V_{IN} = 4.5V			60	μA
	DM8322	V_{CC} = 5.25V					
	DM9322	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8322	V_{CC} = 5.25V					
Logical "0" Input Current	DM9322	V_{CC} = 5.5V	V_{IN} = 0.4V		−1	−1.6	mA
	DM8322	V_{CC} = 5.25V					
	DM9322	V_{CC} = 4.5V				−1.24	mA
	DM8322	V_{CC} = 4.75V				−1.41	mA
Output Short Circuit Current (Note 3)	DM9322	V_{CC} = 5.5V		−35	−46	−80	mA
	DM8322	V_{CC} = 5.25V					
Supply Current − (each device)	DM9322 DM8322	V_{CC} = 5V	All Inputs = 4.5V		30.	43	mA
Input Clamp Voltage	DM9322	V_{CC} = 5V	I_{IN} = −12 mA		−1.0	−1.5	V
	DM8322	T_A = 25°C					
Propagation Delay to a Logical "0" from Data to Output, t_{pd0}		V_{CC} = 5.0V T_A = 25°C		6	11	16	ns
Propagation Delay to a Logical "0" from Select to Z_A, t_{pd0}		V_{CC} = 5.0V T_A = 25°C		8	17	27	ns
Propagation Delay to a Logical "1" from Data to Output, t_{pd1}		V_{CC} = 5.0V T_A = 25°C		4	8	15	ns
Propagation Delay to a Logical "1" from Select to Z_A, t_{pd1}		V_{CC} = 5.0V T_A = 25°C		5	15	25	ns
Enable to Output, t_{pd0}		V_{CC} = 5V T_A = 25°C		7	16	23	ns
Enable to Output, t_{pd1}		V_{CC} = 5V T_A = 25°C		6	14.	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM9322 and across the 0°C to 70°C range for the DM8322. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

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Series 9000

DM9601/DM8601 retriggerable monostable multivibrator

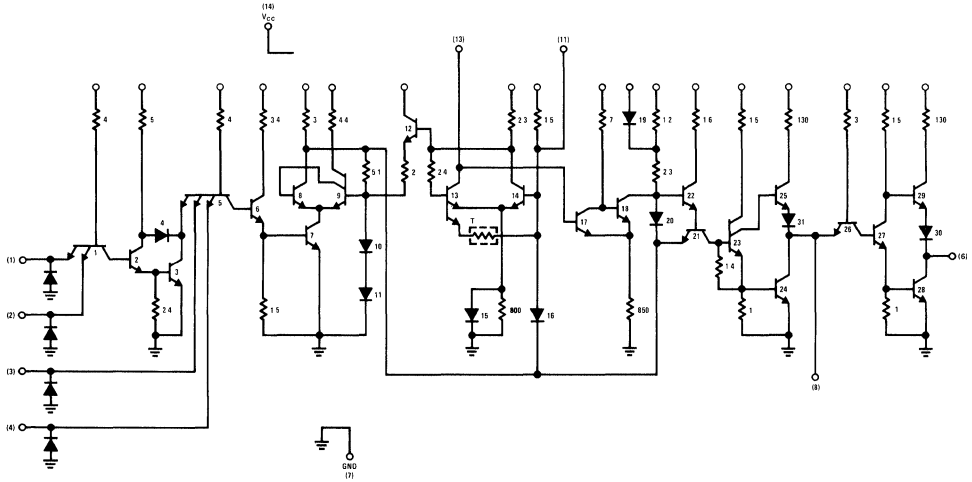
general description

The DM9601/DM8601 is both pin-for-pin and spec-for-spec interchangeable with the 9601 one-shot. Pulse widths range from 50 ns upward depending upon the values of the external R&C used. The retriggerable feature allows for output pulse widths to be extended beyond the normal range attainable with just a resistor and capacitor.

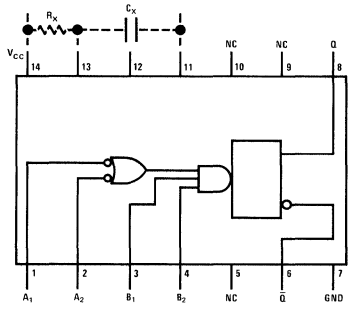
features

- Input Clamping Diodes
- Complementary DC Level Sensitive Inputs
- Flexibility of Operation—Optional Retriggering/Lockout Capability
- DTL/TTL Compatible Logic Levels
- High Speed Operation—Input Repetition Rate > 10 MHz
- Output Pulse Width Range 50 ns to ∞
- Leading or Trailing Edge Triggering
- Complementary Outputs

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

DM9601
absolute maximum ratings

Supply Voltage to Ground	−0.5V to +8.0V
Input Voltage	−0.5V to +5.5V
Voltage Applied to Outputs	−0.5V to $+V_{CC}$
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

TABLE I

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		−55°C		+25°C			+125°C			
		Min	Max.	Min	Typ.	Max	Min	Max		
V_{OH}	Output High Voltage	2 4		2 4	3 3		2 4		V	V_{CC} = 4 5V I_{OH} = −0 72 mA (Note 2)
V_{OL}	Output Low Voltage		0 4		0 2	0 4		0 4	V	V_{CC} = 4 5V I_{OL} = 10 mA (Note 2)
V_{IH}	Input High Voltage	2 0		1 7			1 4		V	V_{CC} = 4 5V
V_{IL}	Input Low Voltage		0 85			0 90		0 85	V	V_{CC} = 5 5V (Note 3)
I_F	Input Load Current		−1 6		−1 1	−1 6		−1 6	mA	V_{CC} = 5 5V V_F = 0 4V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5 5V V_R = 4 5V
I_{SC}	Short Circuit Current			−10		−40				V_{CC} = 5 0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5 5V
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5 0V R_X = 5 0 KΩ
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{pw}	Pulse Width Variation			3 08	3 42	3 76			μs	V_{CC} = 5 0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5 0	25	5 0		25	5 0	25	kΩ	

Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8. Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6

Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns)

DM8601
absolute maximum ratings

Supply Voltage to Ground	−0.5V to +8.0V
Input Voltage	−0.5V to +5.5V
Voltage Applied to Outputs	−0.5V to $+V_{CC}$
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

TABLE II

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		0°C		+25°C			+75°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2 4		2 4	3 4		2 4		V	V_{CC} = 4 75V I_{OH} = −0 96 mA (Note 2)
V_{OL}	Output Low Voltage		0 45		0 2	0 45		0 45	V	V_{CC} = 4 75V I_{OL} = 12 8 mA (Note 2)
V_{IH}	Input High Voltage	1 9		1 8			1 6		V	V_{CC} = 4 75V
V_{IL}	Input Low Voltage		0 85			0 85		0 85	V	V_{CC} = 5 25V (Note 3)
I_F	Input Load Current		−1 6		−1 0	−1 6		−1 6	mA	V_{CC} = 5 25V V_F = 0 45V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5 25V V_R = 4 5V
I_{SC}	Short Circuit Current			−10		−40			mA	V_{CC} = 5 0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5 25V GND Pins 1 & 2
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5 0V R_X = 5 0 KΩ
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$L_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{pw}	Pulse Width Variation			3 08	3 42	3.76			μs	V_{CC} = 5 0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5 0	50	5 0		50	5 0	50	kΩ	

Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8
Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6

Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns)

operating rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown on tables I and II. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{pw} may be calculated as follows:

   $$t_{pw} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$

   R_X in KΩ, C_X in pF and t_{pw} in ns

   For $C_X < 10^3$ pF, see curve.
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$
4. Set-up time(t_1) for input trigger pulse >40 ns. (See Figure 1)

   Release time(t_2) for input trigger pulse >40 ns. (See Figure 2)
5. Retrigger pulse width (see Figure 3) is calculated as follows:

   $$t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{pd+}$$

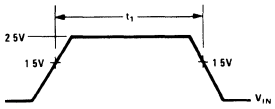


Figure 1

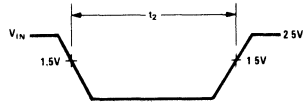


Figure 2

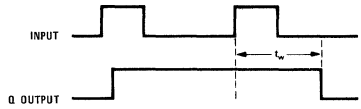


Figure 3

Series 10,000

REFERENCE

The following table references all Physical Dimension Drawings, Waveforms, and Test Circuits for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES											WAVE-FORMS		TEST CIRCUITS	
Devices	Pg	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)						
		Fig.	Pg.	Fig.	Pg	Type	Fig.	Pg	Type	Fig.	Pg.	Type	Fig	Pg.	Fig.	Pg.
DM10101	7-1			12	IV	J							41	11-18	10	11-2
DM10102	7-3			12	IV	J							41	11-18	10	11-2
DM10105	7-5			12	IV	J							41	11-18	10	11-2
DM10106	7-7			12	IV	J							41	11-18	10	11-2
DM10107	7-9			12	IV	J							41	11-18	10	11-2
DM10109	7-11			12	IV	J							41	11-18	10	11-2
DM10110	7-13			12	IV	J										
DM10111	7-15			12	IV	J										
DM10112	7-17			12	IV	J										
DM10115	7-19			12	IV	J										
DM10116	7-21			12	IV	J										
DM10117	7-23			12	IV	J										
DM10118	7-25			12	IV	J										
DM10119	7-27			12	IV	J										
DM10121	7-29			12	IV	J										
DM10124	7-31			12	IV	J										

*Order Numbers use Device No suffixed with package letter, i.e. DM10101J.

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Series 10,000

DM10101(MC10101) quad OR/NOR gate with strobe

general description

The DM10101 quad gate is a low power, high speed, standard ECL logic device. High Z input pulldowns allow high DC and AC fanout and eliminate the need to tie unused inputs to an external supply. The open emitter outputs allow maximum flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines. Wire-"OR"ing of outputs is available with the open emitter outputs.

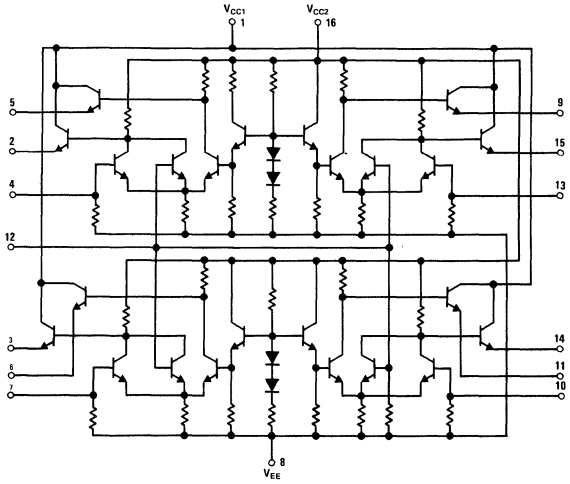
applications

The DM10101 is useful in control, bussing and communications in high speed central processors, high speed peripherals, digital communications systems, minicomputers and instrumentation. This device is commonly used for control and bussing data by using the wire OR capability of the basic ECL gate and/or the common enable input. The complementary outputs on all gates makes this part useful as a quad line driver for twisted pair lines thus reducing package count.

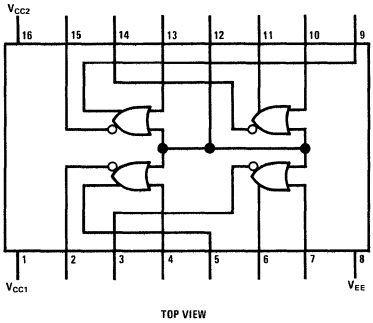
features

- Slow rise and fall times 3.5 ns
- High speed 2.0 ns
- Low power 25 mW/gate
- High fanout 50 mA/output
- 50Ω line driving capability
- High Z input pulldowns
- Open emitter follower outputs
- Wire OR capability
- Complementary output for added versatility
- Standard end power pins for conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	UNITS
−30°C	−0 89	−1 89	−1 205	−1 50	−5 2	V
+25°C	−0 81	−1 85	−1 105	−1 475	−5 2	V
+85°C	−0 70	−1 825	−1 035	−1 44	−5 2	V

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10101 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	13	–	–	–	–	265			μAdc	13					
	I_{inH}	12	–	–	–	–	550	–	–	μAdc	12	–	–	–	8	1, 16
	I_{inL}	12, 13	–	–	0 5	–	–	–	–	μAdc	–	12, 13	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	9	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	12	–	–	–	8	1, 16
		9	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	13	–	–	–	8	1, 16
		15	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	–	12	–	–	8	1, 16
		15	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	–	13	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	9	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	–	12	–	–	8	1, 16
		9	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	–	13	–	–	8	1, 16
		15	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	12	–	–	–	8	1, 16
		15	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	13	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	9	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	12	–	8	1, 16
		9	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	13	–	8	1, 16
		15	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	–	12	8	1, 16
		15	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	–	13	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	9	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	–	12	8	1, 16
		9	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	–	13	8	1, 16
		15	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	12	–	8	1, 16
		15	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	13	–	8	1, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	$t_{12+\ 15-}$	15	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	15	8	1, 16
	$t_{12-\ 15+}$	15	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	15	8	1, 16
	$t_{12+\ 9+}$	9	–	–	1 0	2 0	2 9	–		ns	–	–	12	9	8	1, 16
	$t_{12-\ 9-}$	9	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	9	8	1, 16
Rise Time	t_{15+}	15	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	15	8	1, 16
(20 to 80%)	t_{9+}	9	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	9	8	1, 16
Fall Time	t_{15-}	15	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	15	8	1, 16
(20 to 80%	t_{9-}	9	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	9	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2 0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner

Series 10,000

DM10102(MC10102) quad gate

general description

The DM10102 quad gate is a low power, high speed, standard ECL logic device. High Z input pulldowns allow high DC and AC fanout and eliminate the need to tie unused inputs to an external supply. The open emitter outputs allow maximum flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines. Wire Oring of outputs is available with the open emitter outputs.

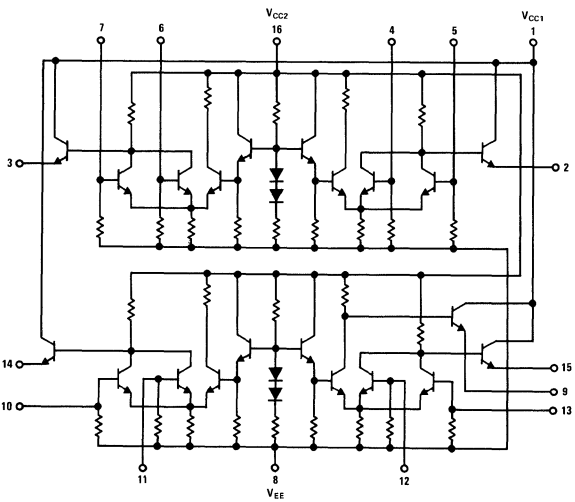
applications

The DM10102 is very useful in control, bussing, and communications in high speed central processors, high speed peripherals, digital communications systems, minicomputers and instrumentation This device is commonly used for control and bussing data by using the wire OR capability of the basic ECL gate. The additional non-inverting output on one gate adds to the flexibility of this part.

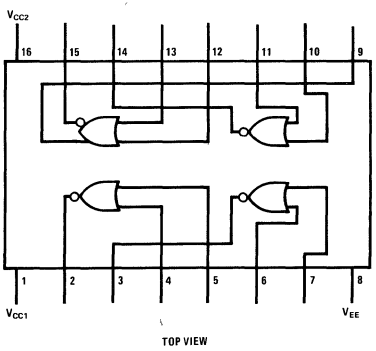
features

- Slow rise and fall times 3 5 ns
- High speed 2.0 ns
- Low power 25 mW/gate
- High fanout 50 mA/output
- 50Ω line driving capability
- High Z input pulldowns
- Open emitter follower outputs
- Wire OR capability
- Complementary output for added versatility
- Standard end power pins for conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

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absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	UNITS
−30°C	−0 89	−1 89	−1 205	−1 50	−5 2	V
+25°C	−0 81	−1 85	−1 105	−1 475	−5 2	V
+85°C	−0 70	−1 825	−1 035	−1 44	−5 2	V

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10102 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	12	–	–	–	–	265	–	–	μAdc	12	–	–	–	8	1, 16
	I_{inL}	12	–	–	0 5	–	–	–	–	μAdc	–	12	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	9	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	12	–	–	–	8	1, 16
		9	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	13	–	–	–	8	1, 16
		15	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	–	12	–	–	8	1, 16
		15	−1 06	−0 89	−0 96	–	−0 81	−0 89	−0 70	Vdc	–	13	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	9	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	–	12	–	–	8	1, 16
		9	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	–	13	–	–	8	1, 16
		15	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	12	–	–	–	8	1, 16
		15	−1 89	−1 675	−1 85	–	−1 65	−1 825	−1 615	Vdc	13	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	9	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	12	–	8	1, 16
		9	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	13	–	8	1, 16
		15	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	–	12	8	1, 16
		15	−1 08	–	−0 98	–	–	−0 91	–	Vdc	–	–	–	13	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	9	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	–	12	8	1, 16
		9	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	–	13	8	1, 16
		15	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	12	–	8	1, 16
		15	–	−1 655	–	–	−1 63	–	−1 595	Vdc	–	–	13	–	8	1, 16
Switching Times (50-ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	$t_{12+\ 15-}$	15	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	15	8	1, 16
	$t_{12-\ 15+}$	15	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	15	8	1, 16
	$t_{12+\ 9+}$	9	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	9	8	1, 16
	$t_{12-\ 9-}$	9	–	–	1 0	2 0	2 9	–	–	ns	–	–	12	9	8	1, 16
Rise Time	t_{15+}	15	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	15	8	1, 16
(20 to 80%)	t_{9+}	9	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	9	8	1, 16
Fall Time	t_{15-}	15	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	15	8	1, 16
(20 to 80%	t_{9-}	9	–	–	1 1	2 0	3 3	–	–	ns	–	–	12	9	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

Series 10,000

DM10105(MC10105) triple 2-3-2 OR/NOR gate

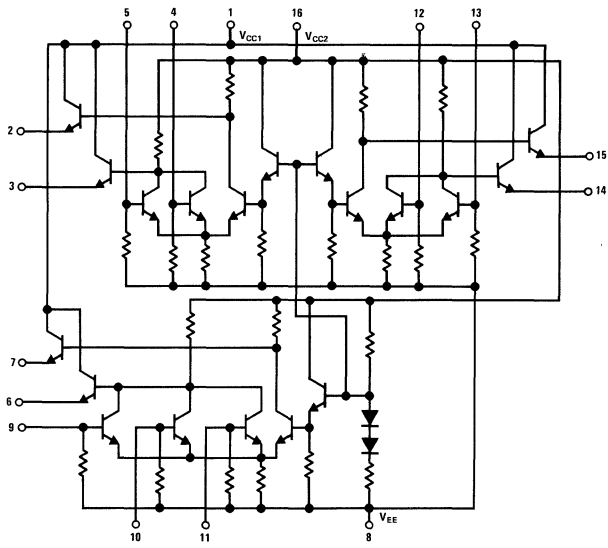
general description

The DM10105 triple gate is a low power, high speed, ECL logic device with the standard ECL high Z inputs and open emitter outputs. This offers the system designer maximum flexibility in layout and design. The open emitter output allows a maximum number of gates to be wire ORed. This device is useful in high speed digital communications systems, central processors, peripheral controllers, minicomputers, instrumentation, and testing systems. The DM10105 is a general purpose gate which generates both true and complement of a control signal and can be used to drive twisted pair lines.

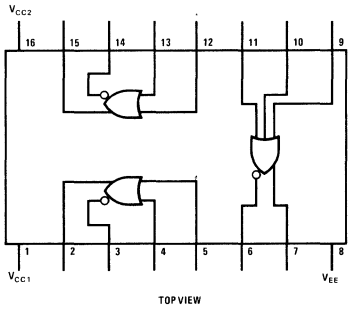
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Open emitter follower outputs for wire OR
- Complementary outputs simultaneous functions
- Standard end power pins conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

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absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30 C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0.810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10105 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED VELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	--	–	15	21	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1, 16
	I_{inL}	4	–	–	0 5	–	–	–	–	μAdc	–	4	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	3	-1 060	-0 890	-0 960	–	-0 810	-0 890	-0 700	Vdc	–	4	–	–	8	1, 16
		2	-1 060	-0 890	-0 960	–	-0 810	-0 890	-0 700	Vdc	4	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1 890	-1 675	-1 850	–	-1 650	-1 825	-1 615	Vdc	4	–	–	–	8	1, 16
		2	-1 890	-1 675	-1 850	–	-1 650	-1 825	-1 615	Vdc	–	4	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	3	-1 080	-	-0 980	–	–	− 910	–	Vdc	–	–	–	4	8	1, 16
		2	-1 080	–	-0 980	–	–	− 910	–	Vdc	–	–	4	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1 655	–	–	-1 630	–	-1 595	Vdc	–	–	4	–	8	1, 16
		2	–	-1 655	–	–	-1 630	–	-1 595	Vdc	–	–	–	4	8	1, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{4+3}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16
	t_{4-3+}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16
	t_{4+2+}	2	–	–	–	2 0	–	–	–	ns	–	–	4	2	8	1, 16
	$t_{4\,2}$	2	–	–	–	2 0	–	–	–	ns	–	–	4	2	8	1, 16
Rise Time	t_{3+}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16
(20 to 80%)	t_{2+}	2	–	–	–	2 0	–	–	–	ns	–	–	4	2	8	1, 16
Fall Time	t_3	3	–	–	–	2 0	–	–	–	ns	–	-	4	3	8	1, 16
(20 to 80%)	t_2	2	–	–	–	2 0	–	–	–	ns	–	–	4	2	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

Series 10,000

DM10106(MC10106) triple 4-3-3-input NOR gate

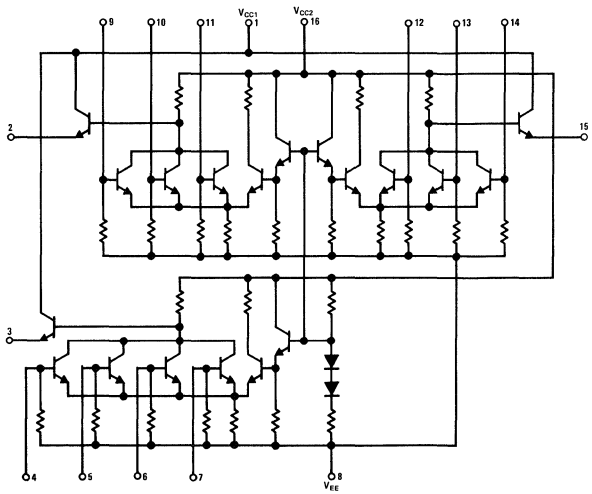
general description

The DM10106 triple gate is a low power, high speed, ECL logic device with the standard ECL high Z inputs and open emitter outputs. This offers the system designer maximum flexibility in layout and design. The open emitter output allows a maximum number of gates to be wire ORed. This device is useful in high speed digital communications systems, central processors, peripheral controllers, minicomputers, instrumentation, and testing systems. Busing data with wire OR is a useful function of the DM10106 and it is also useful as a general purpose gate.

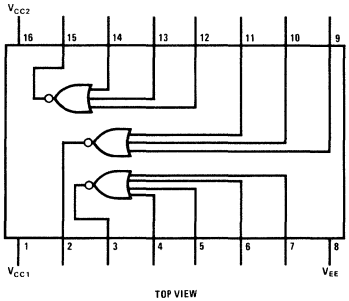
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Open emitter follower outputs for wire OR
- Standard end power pins conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

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absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30 C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10106 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	15	21	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1, 16
	I_{inL}	4	–	–	0 5	–	–	–	–	μAdc	–	4	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	3	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	4	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	4	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	–	4	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	4	–	8	1, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{4+3-}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16
	t_{4-3+}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16
Rise Time (20 to 80%)	t_{3+}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16
Fall Time (20 to 80%)	t_{3-}	3	–	–	–	2 0	–	–	–	ns	–	–	4	3	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

Series 10,000

DM10107(MC10107) triple EXCLUSIVE-OR/NOR gate

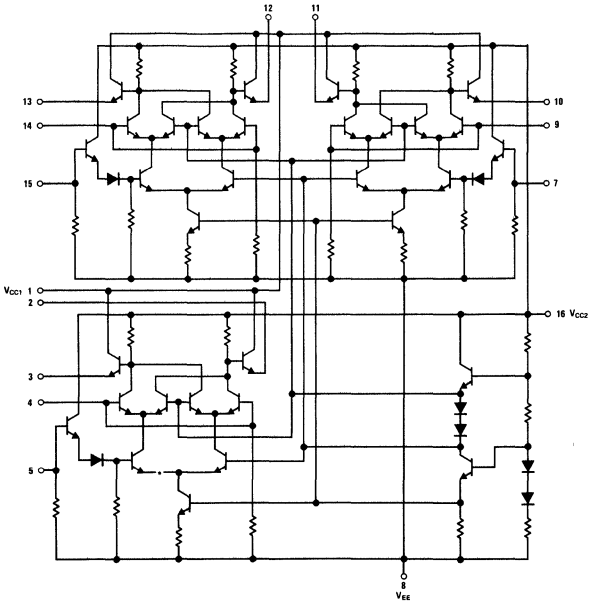
general description

The DM10107 triple gate is a low power, high speed, ECL logic device with the standard ECL high Z inputs and open emitter outputs. This offers the system designer maximum flexibility in layout and design. The open emitter output allows a maximum number of gates to be wired ORed This device is useful in high speed digital communications systems, central processors, peripheral controllers, minicomputers, instrumentation, and testing systems. The DM10107 provides the Exclusive OR and the complement function simultaneously. This device can selectively invert control signals, and can be used to build special purpose adders or counters.

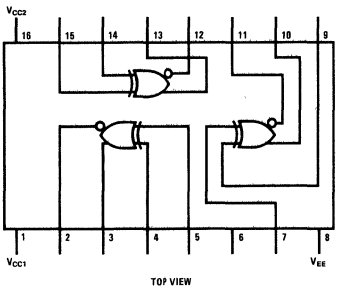
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Open emitter follower outputs for wire OR
- Standard end power pins conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



7

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30 C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts)				
	V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10107 TEST LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					
			−30°C		+25°C		+85°C								
			MIN	MAX	MIN	MAX	MIN	MAX		V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	GND
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	All Inputs	–	–	–	8	1, 16
Input Current	I_{inH}	4, 9, 14	–	–	–	355	–	–	μAdc	*	–	–	–	8	1, 16
		5, 7, 15	–	–	–	265	–	–	μAdc	*	–	–	–	8	1, 16
	I_{inL}	*	–	–	0 5		–	–	μAdc	–		–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	−0 810	−0 890	−0 700	Vdc	4, 5	–	–	–	8	1, 16
		2	−1 060	−0 890	−0 960	−0 810	−0 890	−0 700	Vdc	–	4, 5	–	–	8	1, 16
		3	−1 060	−0 890	−0 960	−0 810	−0 890	−0 700	Vdc	4	5	–	–	8	1, 16
		3	−1 060	−0 890	−0 960	−0 810	−0 890	−0 700	Vdc	5	4	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	2	−1 890	−1 675	−1 850	−1 650	−1 825	−1 615	Vdc	4	5	–	–	8	1, 16
		2	−1 890	−1 675	−1 850	−1 650	−1 825	−1 615	Vdc	5	4	–	–	8	1, 16
		3	−1 890	−1 675	−1 850	−1 650	−1 825	−1 615	Vdc	4, 5	–	–	–	8	1, 16
		3	−1 890	−1 675	−1 850	−1 650	−1 825	−1 615	Vdc	–	4, 5	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980	–	−0 910	–	Vdc	–	–	4, 5	–	8	1, 16
		2	−1 080	–	−0 980	–	−0 910	–	Vdc	–	–	–	4, 5	8	1, 16
		3	−1 080	–	−0 980	–	−0 910	–	Vdc	–	–	4	5	8	1, 16
		3	−1 080	–	−0 980	–	−0 910	–	Vdc	–	–	5	4	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1 655	–	−1 630	–	−1 595	Vdc	–	–	4	5	8	1, 16
		2	–	−1 655	–	−1 630	–	−1 595	Vdc	–	–	5	4	8	1, 16
		3	–	−1 655	–	−1 630	–	−1 595	Vdc	–	–	4, 5	–	8	1, 16
		3	–	−1 655	–	−1 630	–	−1 595	Vdc	–	–	–	4, 5	8	1, 16
Switching Times (50Ω Load)			TYP	MAX	TYP	MAX	TYP	MAX	UNITS			Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t^{++}	Inputs	–	–	2 0	–	–	–	ns	5, 7, 15	–	Input	Corresponding	8	1, 16
	t^{+-}	4, 9 or 14	–	–	2 0	–	–	–	ns	5, 7, 15	–	4, 9, or	OR/NOR	8	1, 16
	t^{-+}	to either	–	–	2 0	–	–	–	ns	5, 7, 15	–	14	Outputs	8	1, 16
	t^{--}	Output	–	–	2 0	–	–	–	ns	5, 7, 15	–			8	1, 16
	t^{++}	Inputs	–	–	2 8	–	–	–	ns	4, 9, 14	–	Input	Corresponding	8	1, 16
	t^{+-}	5, 7 or 15	–	–	2 8	–	–	–	ns	4, 9, 14	–	5, 7, or	OR/NOR	8	1, 16
	t^{-+}	to either	–	–	2 8	–	–	–	ns	4, 9, 14	–	15	Outputs	8	1, 16
	t^{--}	Ouput	–	–	2 8	–	–	–	ns	4, 9, 14	–			8	1, 16
Rise Time (20 to 80%)	t^{+}	**	–	–	2 5	–	–	–	ns	4, 9, 14	–	Any Input	Corresponding OR/NOR	8	1, 16
Fall Time (20 to 80%)	t^{-}	**	–	–	2 5	–	–	–	ns	4, 9, 14	–	Any Input	Outputs	8	1, 16

*Individually test each input applying V_{IH} or V_{IL} to input under test
**Any Output

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate The other gates are tested in the same manner

Series 10,000

DM10109 (MC10109) dual 4-5-input OR/NOR gate

general description

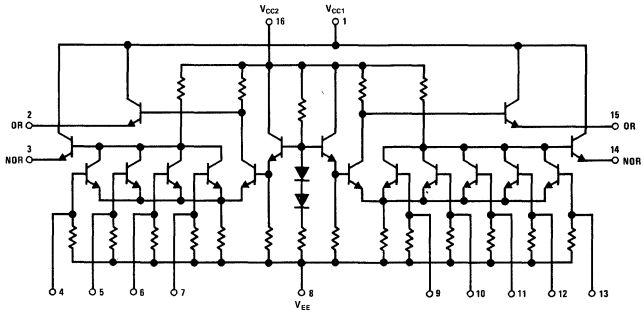
Open emitter outputs, high Z inputs, high speed, and low power are the outstanding characteristics of the DM10109 dual gate. The high Z inputs and open emitter outputs allow a maximum fanout with minimum power requirements. Slow rise and fall times, characteristic of ECL 10,000 series gates, allow conventional interconnect techniques. The open emitter outputs allow a maximum number of outputs to be wire ORed and still drive a heavy fanout. In addition, unused outputs may be left open and do not waste power. This device is designed for use in high speed central processor, peripheral controllers, minicomputers, digital communications systems, and instrumentation and testing systems.

The DM10109 is a general purpose gate that can be used in control. The complementary outputs are also useful in driving twisted pair lines when it is necessary to send control signals or data a long distance.

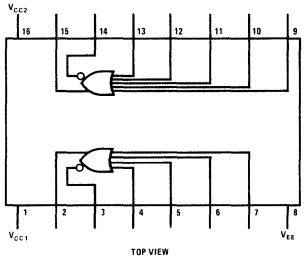
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Multiple open emitter follower outputs
- Multiple wire OR capability
- Complementary outputs
- Standard end power pins
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and connection diagrams



Dual-In-Line Package



absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10109 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	GND
Power Supply Drain Current	I_E	8	–	–	–	10	14	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1, 16
	I_{inL}	4	–	–	0 5	–	–	–	–	μAdc	–	4	–	–	8	1, 16
High Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	4	–	–	–	8	1, 16
		3	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	4	–	–	8	1, 16
Low Output Voltage	V_{OL}	2	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	–	4	–	–	8	1, 16
		3	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	4	–	–	–	8	1, 16
High Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	4	–	8	1, 16
		3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	–	4	8	1, 16
Low Threshold Voltage	V_{OLA}	2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	4	8	1, 16
		3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	4	–	8	1, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{4+2+}	2	–	–	1 0	2 0	2 9	–	–	ns	–	–	4	2	8	1, 16
	$t_{4\ 2}$	2	–	–	1 0	2 0	2 9	–	–	ns	–	–	4	2	8	1, 16
	t_{4+3}	3	–	–	1 0	2 0	2 9	–	–	ns	–	–	4	3	8	1, 16
	t_{4-3+}	3	–	–	1 0	2 0	2 9	–	–	ns	–	–	4	3	8	1, 16
Rise Time	t_{2+}	2	–	–	1 1	2 0	3 3	–	–	ns	–	–	4	2	8	1, 16
(20 to 80%)	t_{3+}	3	–	–	1 1	2 0	3 3	–	–	ns	–	–	4	3	8	1, 16
Fall Time	t_{2-}	2	–	–	1 1	2 0	3 3	–	–	ns	–	–	4	2	8	1, 16
(20 to 80%)	t_{3-}	3	–	–	1 1	2 0	3 3	–	–	ns	–	–	4	3	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

Series 10,000

DM10110(MC10110) dual 3-input/3-output OR gate

general description

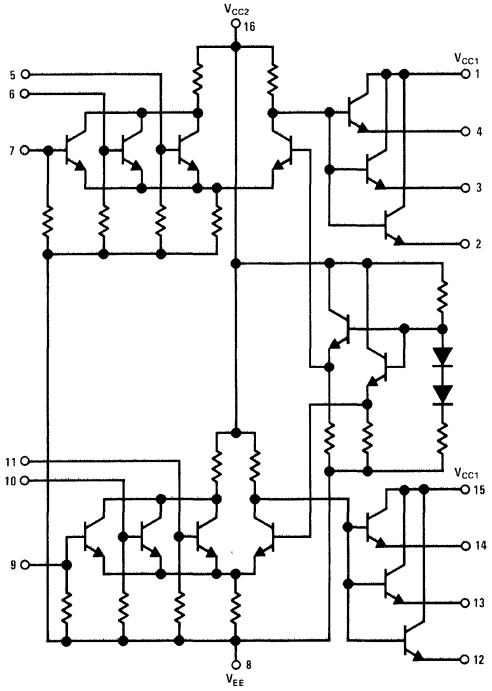
The DM10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the DM10110 particularly useful in clock distribution applications where minimum clock skew is desired.

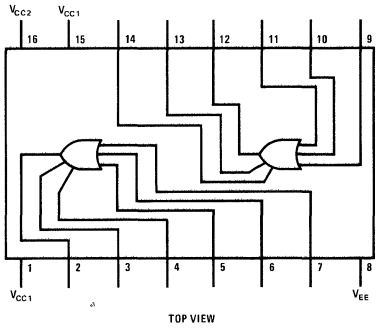
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Multiple open emitter follower outputs
- Multiple wire OR capability
- Standard end power pins
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10110 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	–	–	–	–	435	–	–	μAdc	•	–	–	–	8	1, 15, 16
	I_{inL}	5, 6, 7	–	–	0 5	–	–	–	–	μAdc	–	•	–	–	8	1, 15, 16
Logic "1" Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	5	–	–	–	8	1, 15, 16
		3	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	6	–	–	–	8	1, 15, 16
		4	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	7	–	–	–	8	1, 15, 16
Logic "0" Output Voltage	V_{OL}	2	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	–	5	–	–	8	1, 15, 16
		3	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	–	6	–	–	8	1, 15, 16
		4	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	–	7	–	–	8	1, 15, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	5	–	8	1, 15, 16
		3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	6	–	8	1, 15, 16
		4	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	7	–	8	1, 15, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	5	8	1, 15, 16
		3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	6	8	1, 15, 16
		4	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	7	8	1, 15, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{5+2+}	2	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
	$t_{5\ 2}$	2	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
	t_{5+3+}	3	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	$t_{5\ 3-}$	3	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{5+4+}	4	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
	t_{5-4-}	4	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
Rise Time	t_{2+}	2	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
(20 to 80%)	t_{3+}	3	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{4+}	4	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
Fall Time	t_{2-}	2	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
(20 to 80%)	t_{3-}	3	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{4-}	4	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	4	8	1, 15, 16

*Individually test each input applying V_{IH} or V_{IL} to pin under test

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2 0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

Series 10,000

DM10111(MC10111) dual 3-input/3-output NOR gate

general description

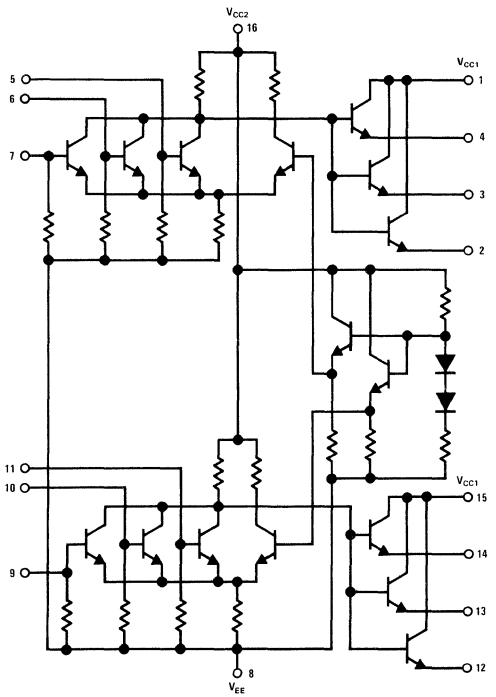
The DM10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the DM10111 particularly useful in clock distribution applications where minimum clock skew is desired.

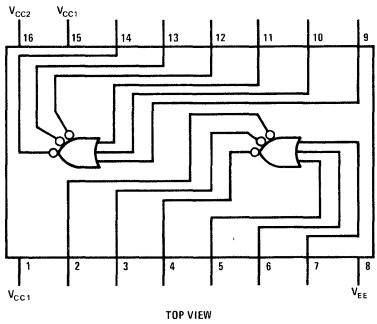
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Multiple open emitter follower outputs
- Multiple wire OR capability
- Standard end power pins
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10111 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	–	–	–	–	435	–	–	μAdc	*	–	–	–	8	1, 15, 16
	I_{inL}	5, 6, 7	–	–	0 5	–	–	–	–	μAdc	–	*	–	–	8	1, 15, 16
Logic "1" Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	5	–	–	8	1, 15, 16
		3	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	6	–	–	8	1, 15, 16
		4	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	7	–	–	8	1, 15, 16
Logic "0" Output Voltage	V_{OL}	2	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	5	–	–	–	8	1, 15, 16
		3	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	6	–	–	–	8	1, 15, 16
		4	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	7	–	–	–	8	1, 15, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980		–	−0 910	–	Vdc	–	–	–	5	8	1, 15, 16
		3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	–	6	8	1, 15, 16
		4	−1 080	–	−0 980	–		−0 910	–	Vdc	–	–	–	7	8	1, 15, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	5	–	8	1, 15, 16
		3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	6	–	8	1, 15, 16
		4	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	7	–	8	1, 15, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{5+2-}	2	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
	$t_{5\ 2+}$	2	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
	t_{5+3-}	3	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	$t_{5\ 3+}$	3	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{5+4}	4	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
	$t_{5\ 4+}$	4	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
Rise Time	t_{2+}	2	–	–	1 1	2 2	3 5	–		ns	–	–	5	2	8	1, 15, 16
(20 to 80%)	t_{3+}	3	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	3	8	1 15, 16
	t_{4+}	4	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
Fall Time	t_2	2	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
(20 to 80%)	t_3	3	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_4	4	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	4	8	1, 15, 16

*Individually test each input applying V_{inH} or V_{inL} to pin under test

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate The other gate is tested in the same manner

Series 10,000

DM10112(MC10112) dual 3-input 1 OR/2 NOR gate

general description

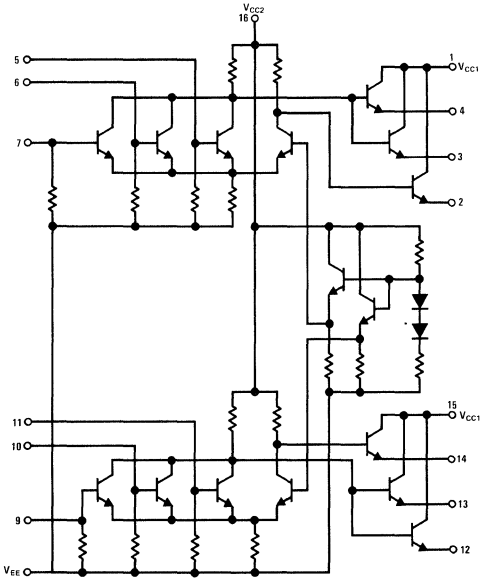
The DM10112 is a dual 3 input 1 OR/2 NOR gate. The DM10112 is useful for driving multiple transmission lines. The open emitter outputs allow the use of wire OR in data bus applications.

The ability to drive multiple transmission lines from a single gate make the DM10112 particularly useful in clock distribution applications where minimum clock skew is desired. The DM10112 is also useful for memory chip select decoding.

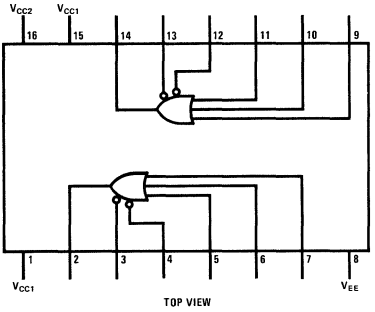
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Multiple open emitter follower outputs
- Multiple wire OR capability
- Standard end power pins
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

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absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10112 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	–	38	–	–	mAdc	–	–	–	–	8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	–	–	–	–	435	–	–	μAdc	*	–	–	–	8	1, 15, 16
	I_{inL}	5, 6, 7	–	–	0 5	–	–	–	–	μAdc	–	*	–	–	8	1, 15, 16
Logic "1" Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	5	–	–	–	8	1, 15, 16
		3	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	6	–	–	8	1, 15, 16
		4	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	–	7	–	–	8	1, 15, 16
Logic "0" Output Voltage	V_{OL}	2	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	–	5	–	–	8	1, 15, 16
		3	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	6	–	–	–	8	1, 15, 16
		4	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	7	–	–	–	8	1, 15, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	5	–	8	1, 15, 16
		3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	–	6	8	1, 15, 16
		4	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	–	7	8	1, 15, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	5	8	1, 15, 16
		3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	6	–	8	1, 15, 16
		4	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	7	–	8	1, 15, 16
Switching Times (50-ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{5+2+}	2	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
	t_{5-2-}	2	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
	t_{5+3-}	3	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{5-3+}	3	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{5+4-}	4	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
	t_{5-4+}	4	–	–	1 4	2 4	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
Rise Time	t_{2+}	2	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
(20 to 80%)	t_{3+}	3	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_{4+}	4	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	4	8	1, 15, 16
Fall Time	t_2	2	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	2	8	1, 15, 16
(20 to 80%)	t_{3-}	3	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	3	8	1, 15, 16
	t_4	4	–	–	1 1	2 2	3 5	–	–	ns	–	–	5	4	8	1, 15, 16

*Individually test each input using the pin connections shown

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2 0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

Series 10,000

DM10115(MC10115) quad differential amplifier

general description

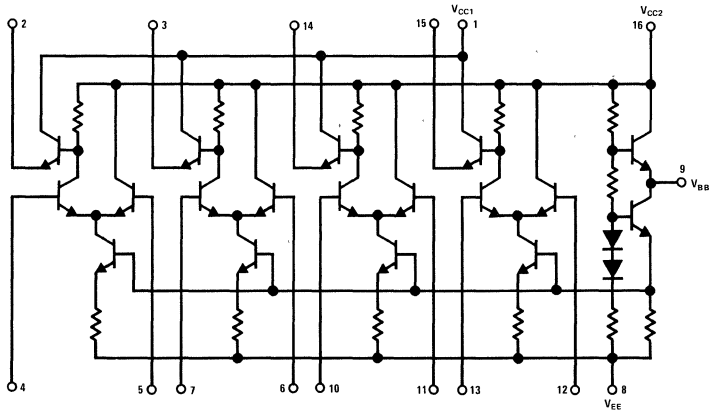
The DM10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the DM10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input must be connected to V_{BB} (pin 9) to prevent overloading the current source bias network.

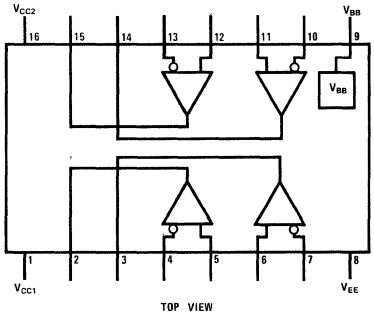
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0ns
- Low power
- High fanout 50 mA/output
- Open emitter follower outputs for wire OR
- Standard end power pins conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{BB}	V_{EE}
−30°C	−0 890	−1.890	−1 205	−1 500	From	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	Pin	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	9	−5.2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10115 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{BB}	V_{EE}	GND
Power Supply Drain Current	I_E	8	–	–	–	26	–	–	mAdc	–	4, 7, 10, 13	–	–	5, 6, 11, 12	8	1, 16
Input Current	I_{in}	4	–	–	–	100	–	–	μAdc	4	7, 10, 13	–	–	5, 6, 11, 12	8	1, 16
Input Leakage Current	I_R	4	–	–	–	1 0	–	–	μAdc	–	7, 10, 13	–	–	5, 6, 11, 12	8, 4	1, 16
Logic "1" Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	−0 810	−0 890	−0 700	Vdc	7, 10, 13	4	–	–	5, 6, 11, 12	8	1, 16
Logic "0" Output Voltage	V_{OL}	2	−1 890	−1 675	1 850	−1 650	−1 825	−1 615	Vdc	4	7, 10, 13	–	–	5, 6, 11, 12	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980		−0 910	–	Vdc	–	7, 10, 13	–	4	5, 6, 11, 12	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1 655	–	−1 630	–	−1 595	Vdc	–	7, 10, 13	4	–	5, 6, 11, 12	8	1, 16
Reference Voltage	V_{BB}	9	−1 420	−1 280	−1 350	−1 230	1 295	−1 150	Vdc	–	–	–	–	5, 6, 11, 12	8	1, 16
Switching Times (50 ohm Load)			TYP	MAX	TYP	MAX	TYP	MAX		Pulse In		Pulse Out			−3 2 Vdc	−2 0 Vdc
Propagation Delay	$t_{d\ 2+}$	2	2 0	–	2 0	–	2 0	–	ns	4		2		5, 6, 11, 12	8	1, 16
	t_{d+2-}	2	2 0	–	2 0	–	2 0	–	ns	4		2		5, 6, 11, 12	8	1, 16
Rise Time (20% to 80%)	t_{2+}	2	2 0	–	2 0	–	2 0	–	ns	4		2		5, 6, 11, 12	8	1, 16
Fall Time (20% to 80%)	t_{2-}	2	2 0	–	2 0		2 0	–	ns	4		2		5, 6, 11, 12	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

Series 10,000

DM10116 (MC10116) triple differential line receiver

general description

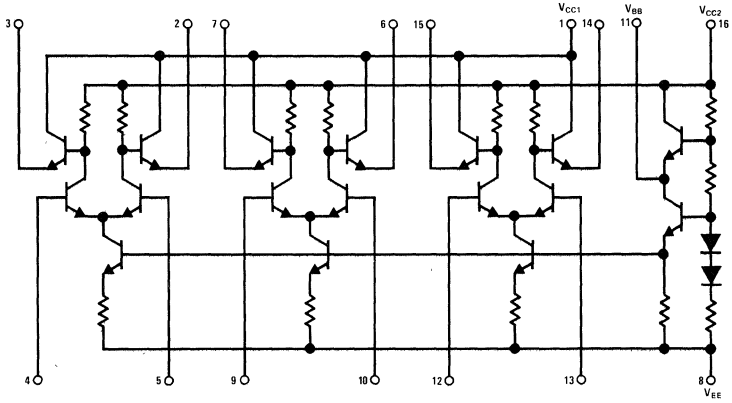
The DM10116 triple differential line receiver is designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt Trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the DM10116 with excellent common mode noise rejection. If any line receiver in a package is not used, one input must be connected to V_{BB} (pin 11) to prevent overloading the current source bias network.

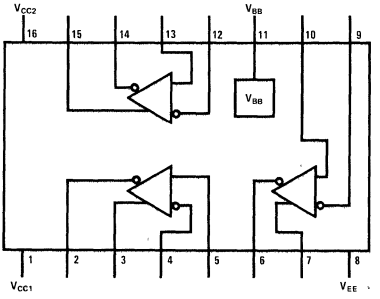
features

- Slow rise and fall times 3.5 ns
- High speed t_{pd} = 2.0 ns
- Low power
- High fanout 50 mA/output
- Open emitter follower outputs for wire OR
- Complementary outputs simultaneous functions
- Standard end power pins conventional layout
- Separate V_{CC} pins maintain high speed and minimize crosstalk and noise generation

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{BB}	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	From	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	Pin	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	11	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10116 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{BB}	V_{EE}	GND
Power Supply Drain Current	I_E	8	–	–	–	14	–	–	–	mAdc	–	4, 9, 12	–	–	5, 10, 13	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	100	–	–	μAdc	4	9, 12	–	–	5, 10, 13	8	1, 16
Input Leakage Current	I_R	4	–	–	–	–	1 0	–	–	μAdc	–	9, 12	–	–	5, 10, 13	8, 4	1, 16
High Output Voltage	V_{OH}	2	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	4	9, 12	–	–	5, 10, 13	8	1, 16
		3	−1 060	−0 890	−0 960	–	−0 810	−0 890	−0 700	Vdc	9, 12	4	–	–	5, 10, 13	8	1, 16
Low Output Voltage	V_{OL}	2	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	9, 12	4	–	–	5, 10, 13	8	1, 16
		3	−1 890	−1 675	−1 850	–	−1 650	−1 825	−1 615	Vdc	4	9, 12	–	–	5, 10, 13	8	1, 16
High Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	9, 12	4	–	5, 10, 13	8	1, 16
		3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	9, 12	–	–	4	5, 10, 13	8	1, 16
Low Threshold Voltage	V_{OLA}	2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	9, 12	–	4	5, 10, 13	8	1, 16
		3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	9, 12	–	4	–	5, 10, 13	8	1, 16
Reference Voltage	V_{BB}	11	−1 420	−1 280	−1 350	–	−1 230	−1 295	−1 150	Vdc	–	–	–	–	5, 10, 13	8	1, 16
Switching Times (50 ohm load)			TYP	MAX	MIN	TYP	MAX	TYP	MAX				Pulse In	Pulse Out		−3 2 Vdc	+2 0 Vdc
Propagation Delay	t_{4+2+}	2	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	2	5, 10, 13	8	1, 16
	t_{4-2-}	2	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	2	5, 10, 13	8	1, 16
	t_{4+3-}	3	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	3	5, 10, 13	8	1, 16
	t_{4-3+}	3	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	3	5, 10, 13	8	1, 16
Rise Time	t_{2+}	2	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	2	5, 10, 13	8	1, 16
(20% to 80%)	t_{3+}	3	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	3	5, 10, 13	8	1, 16
Fall Time	t_{2-}	2	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	2	5, 10, 13	8	1, 16
(20% to 80%)	t_{3-}	3	2 0	–	–	2 0	–	2 0	–	ns	–	–	4	3	5, 10, 13	8	1 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

Series 10,000

DM10117(MC10117C)
dual 2-wide OR-AND/OR-AND-INVERT gate

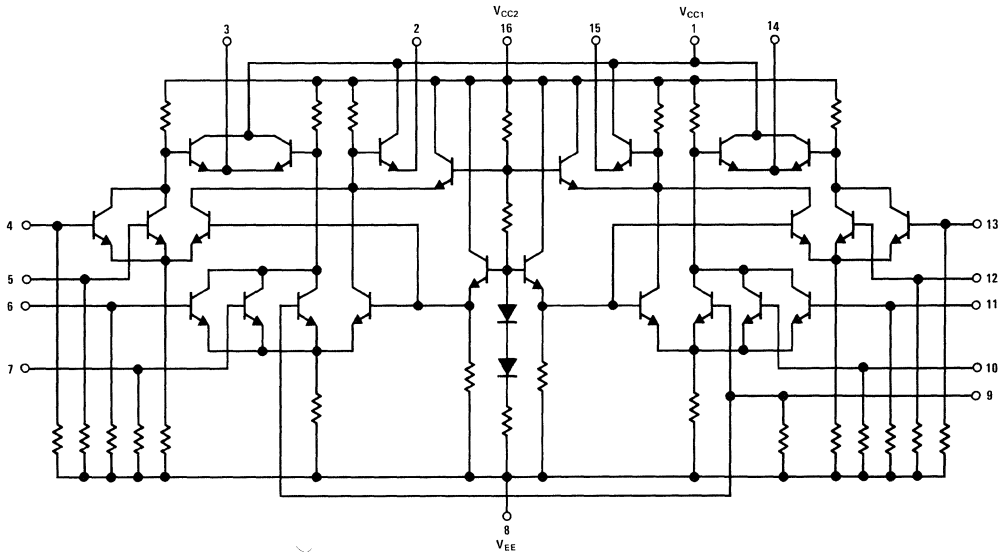
general description

The DM10117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

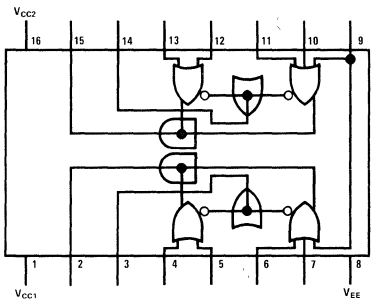
features

- Slow rise and fall times 4.0 ns
- High speed t_{pd} = 2.5 ns for two levels of logic
- Low power 100 mW/pkg
- High fanout 50 mA/output
- 50Ω line driving capability
- High Z input pulldowns — for lower power dissipation
- Open emitter follower outputs
- Internal collector dot and emitter dot — for maximum logic utility and speed
- Wire OR capability — for buss oriented systems
- Complementary outputs — added versatility
- Standard end power pins — standard layout requirements

schematic and connection diagrams



Dual-In-Line Package



$2 = (4 + 5) \bullet (6 + 7 + 9)$
$3 = (4 + 5) \bullet (6 + 7 + 9)$

TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10117 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1, 16
		9	–	–	–	–	355	–	–	μAdc	9	–	–	–	8	1, 16
	I_{inL}	4	–	–	0 5	–	–	–	–	μAdc	–	4	–	–	8	1, 16
		9	–	–	0 5	–	–	–	–	μAdc	–	9	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	−1 060	−0 780	−0 960	–	−0 700	−0 890	−0 590	Vdc	4, 9	–	–	–	8	1, 16
		3	−1 060	−0 780	−0 960	–	−0 700	−0 890	−0 590	Vdc	–	4, 9	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	2	−2 000	−1 675	−1 990	–	−1 650	−1 920	−1 615	Vdc	–	4, 9	–	–	8	1, 16
		3	−2 000	−1 675	−1 990	–	−1 650	−1 920	−1 615	Vdc	4, 9	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	4, 9	–	8	1, 16
		3	−1 080	–	−0 980	–	–	−0 910	–	Vdc	–	–	–	4, 9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	4, 9	8	1, 16
		3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	4, 9	–	8	1, 16
Switching Times (50Ω Load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{4+2+}	2	–	–	–	2 3	–	–	–	ns	9	–	4	2	8	1, 16
	t_{4-2-}	2	–	–	–	2 3	–	–	–	ns	9	–	4	2	8	1, 16
	t_{4+3}	3	–	–	–	2 3	–	–	–	ns	9	–	4	3	8	1, 16
	t_{4-3+}	3	–	–	–	2 3	–	–	–	ns	9	–	4	3	8	1, 16
Rise Time	t_{2+}	2	–	–	–	2 2	–	–	–	ns	9	–	4	2	8	1, 16
(20 to 80%)	t_{3+}	3	–	–	–	2 2	–	–	–	ns	9	–	4	3	8	1, 16
Fall Time	t_{2-}	2	–	–	–	2 2	–	–	–	ns	9	–	4	2	8	1, 16
(20 to 80%)	t_{3-}	3	–	–	–	2 2	–	–	–	ns	9	–	4	3	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner

Series 10,000

DM10118(MC10118) dual 2-wide OR-AND gate

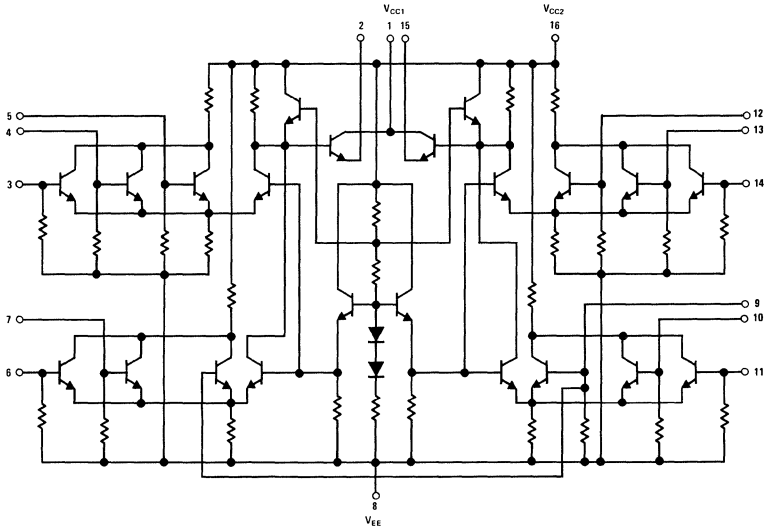
general description

The DM10118 is a basic logic building block providing the OR-AND function, useful in data control and digital multiplexing applications.

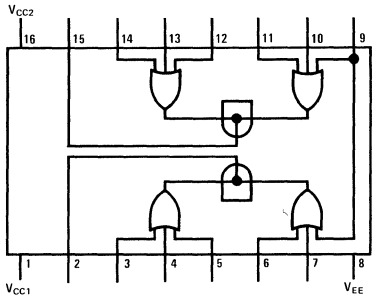
features

- Slow rise and fall times 4.0 ns
- High speed t_{pd} = 2.5 ns for two levels of logic
- Low power 100 mW/package
- High fanout 50 mA/output
- 50Ω line driving capability
- High Z input pulldowns – for lower power dissipation
- Open emitter follower outputs
- Internal collector dot for maximum logic utility and speed
- Wire OR capability – for bus oriented systems
- Standard end power pins – standard layout requirements

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

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absolute maximum ratings

Supply Voltage	-8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	-30°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
-30°C	-0 890	-1 890	-1 205	-1 500	-5 2
+25°C	-0 810	-1 850	-1 150	-1 475	-5 2
+85°C	-0 700	-1 825	-1 035	-1 440	-5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10118 TEST LIMITS -30°C MIN	-30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	20	26	-	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	6	–	–	–	–	265	–	–	μAdc	6	–	–	–	8	1, 16
		7	–	–	-	–	265	–	–	μAdc	7	–	–	–	8	1, 16
		9	–	–	-	–	355	–	–	μAdc	9	–	–	–	8	1, 16
	I_{inL}	6	–	–	0 5	–	–	–	–	μAdc	–	6	–	–	8	1, 16
		7	–	–	0 5	–	–	–	–	μAdc	–	7	–	–	8	1, 16
		9	–	–	0 5	-	–	–	–	μAdc	–	9	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1 060	-0 890	-0 960	–	-0 810	-0 890	-0 700	Vdc	3, 9	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	2	-2 000	-1 675	-1 990	–	-1 650	-1 920	-1 615	Vdc	–	3, 9	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1 080	–	-0 980	-	–	-0 910		Vdc	–	–	3,9	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1 655	–	-	-1 630	–	-1 595	Vdc	–	–	–	3, 9	8	1, 16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3 2V	+2 0V
Propagation Delay	t_{6+2+}	2	–	–	1 4	2 3	3 4	-	–	ns	3	–	6	2	8	1, 16
	$t_{6\ 2}$	2	–	-	1 4	2 3	3 4	–	–	ns	3	–	6	2	8	1, 16
Rise Time (20 to 80%)	t_+	2	-	-	1 5	2 5	4 0	–	–	ns	3	–	6	2	8	1, 16
Fall Time (20 to 80%)	t_-	2	–	–	1 5	2 5	4 0	–	–	ns	3	–	6	2	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

Series 10,000

DM10119(MC10119) 4-wide 4-3-3-3-input OR/AND gate

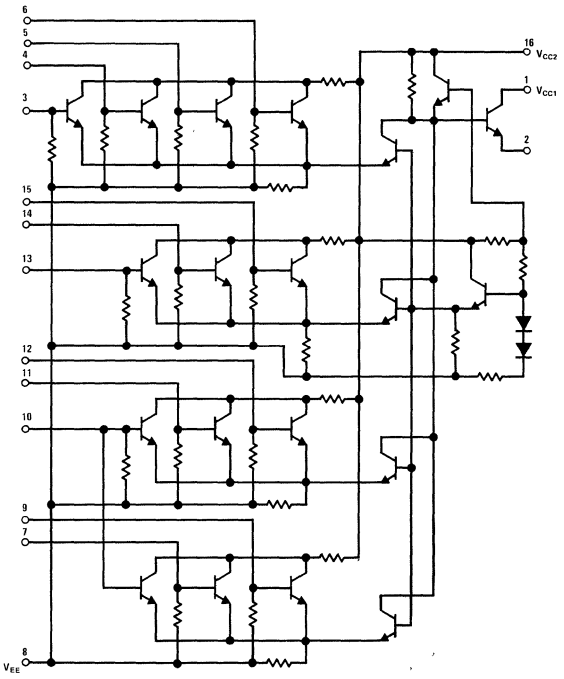
general description

The DM10119 is a 4-Wide 4-3-3-3 Input OR/AND gate with one input from two gates common to pin 10. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

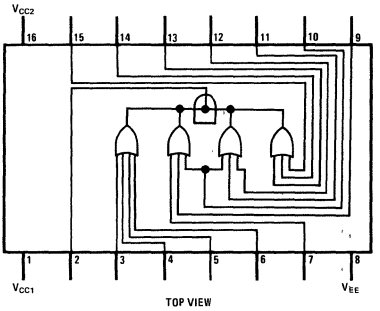
features

- Slow rise and fall times 4.0 ns
- High speed t_{pd} = 2.5 ns for two levels of logic
- Low power 100 mW/package
- High fanout 50 mA/output
- 50Ω line driving capability
- High Z input pulldowns – for lower power dissipation
- Open emitter follower outputs
- Internal collector dot for maximum logic utility and speed
- Wire OR capability – for bus oriented systems
- Standard end power pins – standard layout requirements

schematic and logic diagrams



Dual-In-Line Package



TOP VIEW

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absolute maximum ratings

Supply Voltage	-8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	-30°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
-30°C	-0 890	-1 890	-1 205	-1 500	-5.2
+25°C	-0 810	-1 850	-1 105	-1 475	-5 2
+85°C	-0 700	-1 825	-1 035	-1 440	-5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10119 TEST LIMITS -30°C MIN	-30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1, 16
		9	–	–	–	–	265	–	–	μAdc	9	–	–	–	8	1, 16
		10	–	–	–	–	355	–	–	μAdc	10	–	–	–	8	1, 16
	I_{inL}	7	–	–	0 5	–	–	–	–	μAdc	–	7	–	–	8	1, 16
		9	–	–	0 5	–	–	–	–	μAdc	–	9	–	–	8	1, 16
		10	–	–	0 5	–	–	–	–	μAdc	–	10	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1 060	-0 890	-0 960	–	-0 810	-0 890	-0 700	Vdc	3, 10, 15	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	2	-2 000	-1 675	-1 990	–	-1 650	-1 920	-1 615	Vdc	–	3, 10, 15	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1 080	–	-0 980	–	–	-0 910	–	Vdc	–	–	3, 10, 15	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1 655	–	–	-1.630	–	-1 595	Vdc	–	–	–	3, 10, 15	8	1, 16
Switching Times (50 ohm load)													Pulse In	Pulse Out	-3 2V	+2 0V
Propagation Delay	t_{4+2+}	2	–	–	1 4	2 3	3 4	–	–	ns	10, 13	–	4	2	8	1, 16
	$t_{4\ 2}$	2	–	–	1 4	2 3	3 4	–	–	ns	10, 13	–	4	2	8	1, 16
Rise Time (20 to 80%)	t_+	2	–	–	1 5	2 5	4 0	–	–	ns	10, 13	–	4	2	8	1, 16
Fall Time (20 to 80%)	t_-	2	–	–	1 5	2 5	4 0	–	–	ns	10, 13	–	4	2	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained Outputs are terminated through a 50-ohm resistor to -2.0 volts Test procedures are shown for only one gate. The other inputs are tested in the same manner.

Series 10,000

DM10121(MC10121) OR-AND/OR-AND-INVERT gate

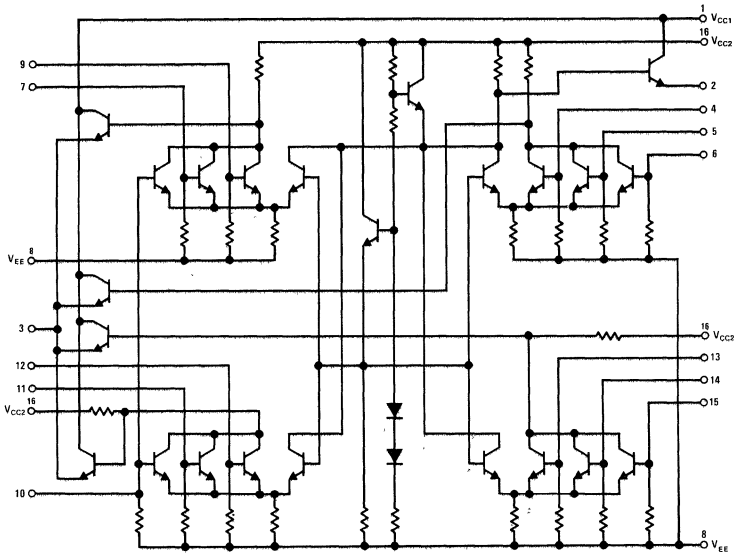
general description

The DM10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.

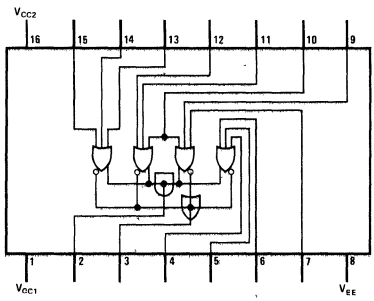
features

- Slow rise and fall times 4.0 ns
- High speed t_{pd} = 2.5 ns for two levels of logic
- Low power 100 mW/pkg
- High fanout 50 mA/output
- 50Ω line driving capability
- High Z input pulldowns — for lower power dissipation
- Open emitter follower outputs
- Internal collector dot and emitter dot — for maximum logic utility and speed
- Wire OR capability — for buss oriented systems
- Complementary outputs — added versatility
- Standard end power pins — standard layout requirements

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Supply Voltage	−8V
Input Voltage	0 to V_{EE}
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

@ TEST TEMP	TEST VOLTAGE VALUES (Volts) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0 890	−1 890	−1 205	−1 500	−5 2
+25°C	−0 810	−1 850	−1 105	−1 475	−5 2
+85°C	−0 700	−1 825	−1 035	−1 440	−5 2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10121 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}	(V_{CC}) GND
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	7	–	–	–	–	265	–	–	μAdc	7	–	–	–	8	1, 16
		9	–	–	–	–	265	–	–	μAdc	9	–	–	–	8	1, 16
		10	–	–	–	–	355	–	–	μAdc	10	–	–	–	8	1, 16
	I_{inL}	7	–	–	0 5	–	–	–	–	μAdc	–	7	–	–	8	1, 16
		9	–	–	0 5	–	–	–	–	μAdc	–	9	–	–	8	1, 16
		10	–	–	0 5	–	–	–	–	μAdc	–	10	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	3	−1 060	−0 780	−0 960	–	−0 700	−0 890	−0 590	Vdc	–	4	–		8	1, 16
		2	−1 060	−0 780	−0 960	–	−0 700	−0 890	−0 590	Vdc	4, 10, 13	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	−2 000	−1 675	−1 990	–	−1 650	−1 920	−1 615	Vdc	4, 10, 13	–	–	–	8	1, 16
		2	−2 000	−1 675	−1 990	–	−1 650	−1 920	−1 615	Vdc	–	4	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	3	−1 080	–	−0 980	–		−0 910	–	Vdc	–	–	–	4	8	1, 16
		2	−1 080	–	−0 980	–		−0 910	–	Vdc	–	–	4, 10, 13	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	4, 10, 13	–	8	1, 16
		2	–	−1 655	–	–	−1 630	–	−1 595	Vdc	–	–	–	4	8	1, 16
Switching Times (50-ohm load)													Pulse In	Pulse Out	−3 2V	+2 0V
Propagation Delay	t_{4+3}	3	–	–	–	2 3	–	–	–	ns	10, 13	–	4	3	8	1, 16
	t_{4-3+}	3	–	–	–	2 3	–	–	–	ns	10, 13	–	4	3	8	1, 16
	t_{4+2+}	2	–	–	–	2 3	–	–	–	ns	10, 13	–	4	2	8	1, 16
	t_{4-2-}	2	–	–	–	2 3	–	–	–	ns	10, 13	–	4	2	8	1, 16
Rise Time	t_{3+}	3	–	–	–	2 5	–	–	–	ns	10, 13	–	4	3	8	1, 16
(20 to 80%)	t_{2+}	2	–	–	–	2 5	–	–	–	ns	10, 13	–	4	2	8	1, 16
Fall Time	t_3	3	–	–	–	2 5	–	–	–	ns	10, 13	–	4	3	8	1, 16
(20 to 80%)	t_{2-}	2	–	–	–	2 5	–	–	–	ns	10, 13	–	4	2	8	1, 16

Note: Each DM10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained Outputs are terminated through a 50-ohm resistor to −2.0 volts Test procedures are shown for only one gate. The other inputs are tested in the same manner.

Series 10,000

DM10124(MC10124) quad TTL to ECL translator/differential line driver

general description

The DM10124 is a quad TTL to ECL translator which may also be used as a quad TTL to ECL differential line driver. The input levels are compatible with the series 7400, series 74H00 and Schottky series 74S00.

The output logic levels are ECL 10,000 compatible over the recommended operating temperature range. Complementary emitter follower outputs provide for inverting, non-inverting or differential line driving applications. A common TTL strobe input is provided which when held at a TTL logic "0" forces all true (non-inverting) outputs to an ECL logic logical "0" LOW and all compliments (inverting) outputs to an ECL logical "1" HIGH.

features

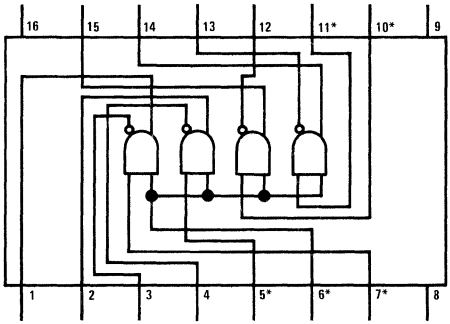
- High speed — $t_{pd} \simeq 3.5$ ns typical
- Power dissipation — 250 mW/pkg typical
- Complementary outputs with ECL 10,000 levels
- High output capacity, drives 8 50Ω lines
- TTL compatible inputs, input strobe
- Four translators per package

applications

The DM10124 may be used as either an inverting or non-inverting TTL to ECL translator. One differential line driving application includes very high speed data transmission in a TTL system by converting the data to ECL levels and driving through terminated twisted line pairs. The DM10125 is the logical complement to the DM10124 and can be used to translate the differential ECL levels back to standard TTL ones. The advantages of ECL transmission line characteristics (i.e. controlled edge speeds, terminations, very high speed data rates) may then be utilized in a TTL system.

connection diagram

Dual-In-Line Package



TOP VIEW

* = TTL LEVELS
V_{CC} = PIN 9 = +5.0V
V_{EE} = PIN 8 = -5.2V
GND = PIN 16 = 0V

absolute maximum ratings

Supply Voltage:	
V_{EE}	−8V
V_{CC}	+7V
Input Voltage	+5.5V
Output Current	50 mA
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C

electrical characteristics

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	DM10124 TEST LIMITS							UNITS	CONDITIONS
			−30°C		+25°C			+85°C			
			MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Power Supply Drain Current	I_{EE}	8					38			mA	Inputs & Outputs
	I_{CC}	9					25			mA	OPEN
Logic "1" Input Current	I_{IH}	2, 7, 10, 11					4			μA	$V_{IN} = V_{IH} = +2.7V$
	I_{IH}	6					16			μA	
Logic "0" Input Current	I_{IL}	5, 7, 10, 11					−1.6			mA	$V_{IN} = V_{IL} = +0.4V$
	I_{IL}	6					6.0			mA	
Logic "1" Input Voltage	V_{IHA}				+2.0					V	Threshold Inputs — Use for Test
Logic "0" Input Voltage	V_{ILA}						0.8			V	
Input Clamp Voltage		5, 6, 10, 11					−1.5			V	Measured at $I_T = -12$ mA
Logic "1" Output Voltage	V_{OH}	1, 2, 14, 15	−1.06	−0.89	−0.96		−0.81	−0.89	−0.70	V	50Ω to −2.0V All Inputs = V_{IH} = 2.7
Logic "1" Output Voltage	V_{OH}	3, 4, 12, 13	−1.06	-0.89	−0.96		−0.81	−0.89	−0.70	V	50Ω to −2.0V Pin 6 = V_{IL} = 0.4V
Logic "0" Output Voltage	V_{OL}	1, 2, 14, 15	−1.89	−1.675	−1.85		−1.65	−1.825	−1.615	V	50Ω to −2.0V Pin 6 = V_{IL} = +0.4V
Logic "0" Output Voltage	V_{OL}	3, 4, 12, 13	−1.89	−1.675	−1.85		−1.65	−1.825	−1.615	V	50Ω to −2.0V All Inputs = V_{IN} = +2.7
Logic "1" Threshold Voltage	V_{OHA}	1, 2, 14, 15	−1.08		−0.98			−0.91		V	50Ω to −2.0V Inputs at V_{IHA} = +2.0
Logic "1" Threshold Voltage	V_{OHA}	3, 4, 12, 13	−1.08		−0.98			−0.91		V	50Ω to −2.0V Input at V_{ILA} = +0.8
Logic "0" Threshold Voltage	V_{OLA}	1, 2, 14, 15		−1.655			−1.63		1.595	V	50Ω to −2.0V Inputs at V_{ILA} = +0.8
Logic "0" Threshold Voltage	V_{OLA}	3, 4, 12, 13		−1.655			−1.63		−1.595	V	50Ω to −2.0V Inputs at V_{IHA} = +2.0
Switching Times 50Ω Load	$t_{pd}++$	5, 6, 7, 10, 11			1.0	3.5	5.0			ns	Each Input in Sequence, Undriven Inputs to V_{CC} (NOM) = +5V
Propagation Delay (3V P-P Input at $t_r = t_f$ = 2 ns, 20% - 80%)	$t_{pd}--$	5, 6, 7, 10, 11			1.0	3.5	5.0			ns	
	$t_{pd}+-$	5, 6, 7, 10, 11			1.0	3.5	5.0			ns	
	$t_{pd}-+$	5, 6, 7, 10, 11			1.0	3.5	5.0			ns	
Rise Time 20% - 80%	t_r	Outputs			1.1	2.0	3.3			ns	
Fall Time 20% - 80%	t_f	Outputs			1.1	2.0	3.3			ns	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

CMOS

REFERENCE

The following table references all Physical Dimension Drawings, Waveforms, and Test Circuits for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES											WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)						
		Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Fig.	Pg.
MM54C00	8-1			8	III	D							8-3		8-3	
MM74C00	8-1	3	II										8-3		8-3	
MM54C02	8-1			8	III	D							8-3		8-3	
MM74C02	8-1	3	II										8-3		8-3	
MM54C04	8-4			8	III	D							8-4		8-4	
MM74C04	8-4	3	II										8-4		8-4	
MM54C10	8-6			8	III	D							8-8		8-8	
MM74C10	8-6	3	II										8-8		8-8	
MM54C20	8-6			8	III	D							8-8		8-8	
MM74C20	8-6	3	II										8-8		8-8	
MM54C42	8-9			9	III	D										
MM74C42	8-9	5	II													
MM54C73	8-11			8	III	D							8-13		8-13	
MM74C73	8-11	3	II										8-13		8-13	
MM54C74	8-14			8	III	D							8-16		8-16	
MM74C74	8-14	3	II										8-16		8-16	
MM54C76	8-11			9	III	D							8-13		8-13	
MM74C76	8-11	5	II										8-13		8-13	
MM54C95	8-17			8	III	D										
MM74C95	8-17	3	II													
MM54C107	8-11			8	III	D							8-13		8-13	
MM74C107	8-11	3	II										8-13		8-13	
MM54C151	8-19			9	III	D							8-21		8-21	
MM74C151	8-19	5	II										8-21		8-21	
MM54C154	8-22			10	III	D							8-24			
MM74C154	8-22	7	III										8-24			
MM54C157	8-25			9	III	D										
MM74C157	8-25	5	II													
MM54C160	8-27			9	III	D							8-30			
MM74C160	8-27	5	II										8-30			
MM54C161	8-27			9	III	D							8-30			
MM74C161	8-27	5	II										8-30			
MM54C162	8-27			9	III	D							8-30			
MM74C162	8-27	5	II										8-30			
MM54C163	8-27			9	III	D							8-30			
MM74C163	8-27	5	II										8-30			
MM54C164	8-31			8	III	D							8-33		8-33	
MM74C164	8-31	3	II										8-33		8-33	
MM54C173	8-35			9	III	D							8-36			
MM74C173	8-35	5	II										8-36			
MM54C192	8-38			9	III	D										
MM74C192	8-38	5	II													
MM54C193	8-38			9	III	D										
MM74C193	8-38	5	II													
MM54C195	8-41			9	III	D							8-42			
MM74C195	8-41	5	II										8-42			

*Order Numbers· use Device No. suffixed with package letter, i.e. MM54C00D.

CMOS

MM54C00/MM74C00 quad two-input NAND gate
MM54C02/MM74C02 quad two-input NOR gate

general description

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

features

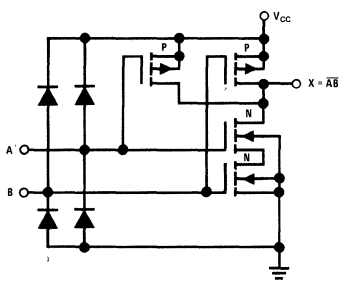
■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.3 V_{CC} typ
■ Low power	10 nW typ
■ Low power T²L compatible	drive 2 LT²L loads

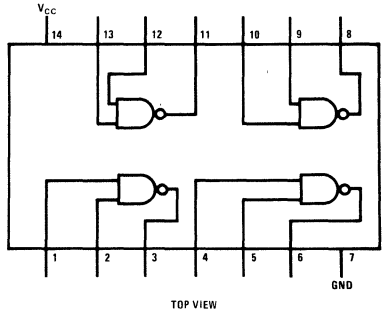
applications

- Automotive
- Instrumentation
- Alarm systems
- Remote metering
- Data terminals
- Medical electronics
- Industrial controls
- Computers

schematic and connection diagrams

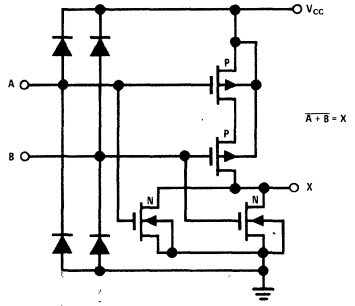
MM54C00/MM74C00

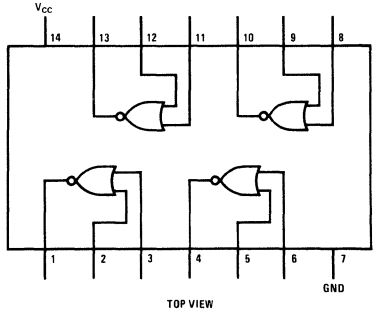




TOP VIEW

MM54C02/MM74C02





TOP VIEW

8

absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to +V_{CC} + 0.3V
Operating Temperature MM54C00,MM54C02	−55°C to +125°C
MM74C00,MM74C02	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{CC} Range	+3V to +15V

electrical characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise specified.

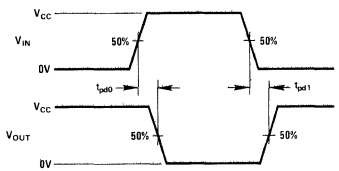
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS to CMOS					
Logical "1" Input Voltage V_{IN} (1)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8.0			V
Logical "0" Input Voltage V_{IN} (0)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage V_{OUT} (1)	V_{CC} = 5.0V, V_{IN} = 1.5, I_O = −10 μA	4.5			V
	V_{CC} = 10.0V, V_{IN} = 7.0, I_O = −10 μA	9.0			V
Logical "0" Output Voltage V_{OUT} (0)	V_{CC} = 5.0V, V_{IN} = 3.5, I_O = 10 μA			0.5	V
	V_{CC} = 10.0V, V_{IN} = 8.0, I_O = 10 μA			1.0	V
Logical "1" Input Current I_{IN} (1)	V_{CC} = 15V, V_{IN} = 15V			1	μA
Logical "0" Input Current I_{IN} (0)	V_{CC} = 15V, V_{IN} = 0V	−1			μA
Output Short Circuit Current I_{OS} (1)	V_{CC} = 5.5V, V_{IN} = 0, V_O = 0	1		6	mA
(Note 2)	V_{CC} = 11.0V, V_{IN} = 0, V_O = 0	7.5		30	mA
Output Short Circuit Current I_{OS} (0)	V_{CC} = 5.5V, V_{IN} = V_O = V_{CC}	1.5		10	mA
(Note 2)	V_{CC} = 11.0V, V_{IN} = V_O = V_{CC}	10		40	mA
Supply Current I_{CC}	V_{CC} = 15V			1	μA
Propagation Delay Time to a	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		50	90	ns
Logical "0" t_{pd0}	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		25	60	ns
Propagation Delay Time to a	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		50	90	ns
Logical "1" t_{pd1}	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		30	60	ns
LOW POWER TTL to CMOS					
Logical "1" Input Voltage V_{IN} (1)	54C V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage V_{IN} (0)	54C V_{CC} = 4.5V			0.8	V
	74C V_{CC} = 4.75V				
Logical "1" Output Voltage V_{OUT} (1)	54C V_{CC} = 4.5V, I_O = −10 μA	4.4			V
	74C V_{CC} = 4.75V, I_O = −10 μA				
Logical "0" Output Voltage V_{OUT} (0)	54C V_{CC} = 4.5V, I_O = 10 μA			0.8	V
	74C V_{CC} = 4.75V, I_O = 10 μA				
Propagation Delay Time to a	V_{CC} = 5.0V, C_L = 15 pF, T_A = 25°C		125		ns
Logical "0" $t_{pd(0)}$					
Propagation Delay Time to a	V_{CC} = 5.0V, C_L = 15 pF, T_A = 25°C		125		ns
Logical "1" $t_{pd(1)}$					
CMOS to Low Power TTL (tenth power)					
Logical "1" Input Voltage V_{IN} (1)	54C V_{CC} = 4.5V	4.0			V
	74C V_{CC} = 4.75V	4.0			
Logical "0" Input Voltage V_{IN} (0)	54C V_{CC} = 4.5V			1.0	V
	74C V_{CC} = 4.75V			1.0	
Logical "1" Output Voltage V_{OUT} (1)	54C V_{CC} = 4.5V, V_{IN} = 0.8, I_O = −100 μA	2.4			V
	74C V_{CC} = 4.75V, V_{IN} = 0.8, I_O = −100 μA	2.4			
Logical "0" Output Voltage V_{OUT} (0)	54C V_{CC} = 4.5V, V_{IN} = 4.0, I_O = 360 μA			0.4	V
	74C V_{CC} = 4.75V, V_{IN} = 4.0, I_O = 360 μA			0.4	V
Propagation Time to a	V_{CC} = 5.0V, C_L = 50 pF, R_L = 20k,		60		ns
Logical "0" $t_{pd(0)}$	T_A = 25°C				
Propagation Time to a	V_{CC} = 5.0V, C_L = 50 pF, R_L = 20k,		45		ns
Logical "1" $t_{pd(1)}$	T_A = 25°C				

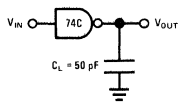
Note 1: These devices should not be connected under power on conditions

Note 2: Only one output at a time may be shorted.

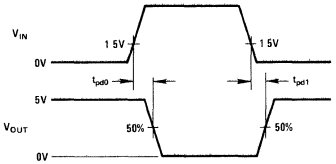
switching time waveforms and ac test circuits

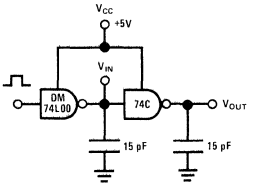
CMOS to CMOS



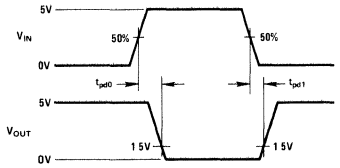


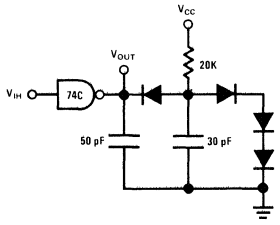
TTL to CMOS





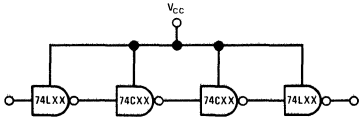
CMOS to low power T^2L



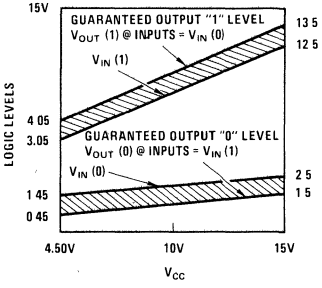


applications

74C Compatibility



Guaranteed noise margin as a function of V_{CC}



CMOS

MM54C04/MM74C04 hex inverter

general description

The MM54C04/MM74C04 hex inverter is constructed from complementary MOS (CMOS) enhancement transistors to achieve lower power and high noise margin.

features

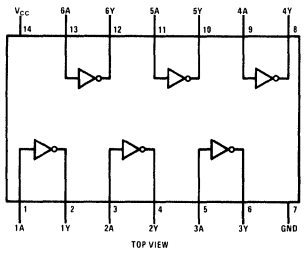
- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} typ
- Low power — 10 nW typ
- Tenth power TTL compatible — drive 2 LPTTL loads

applications

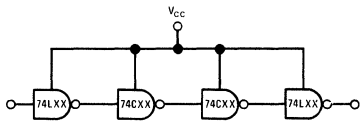
- Automotive
- Instrumentation
- Alarm systems
- Remote metering
- Data terminals
- Medical electronics
- Industrial controls
- Computers

connection diagram

Dual-In-Line Package

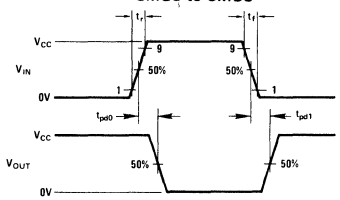


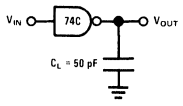
74C Compatibility



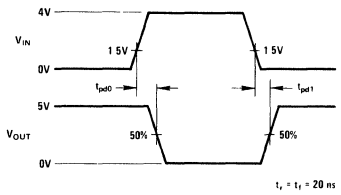
switching time waveforms

CMOS to CMOS

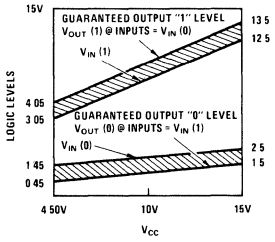




TTL to CMOS



Guaranteed Noise Margin as a Function of V_{CC}



absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	MM54C04	$-55°C$ to $125°C$
	MM74C04	$0°C$ to $70°C$
Storage Temperature		$-65°C$ to $150°C$
Package Dissipation		500 nW
Lead Temperature (Soldering, 10 sec)		$300°C$
Operating V_{CC} Range		+3V to +15V

electrical characteristics

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage $V_{IN(1)}$	$V_{CC} = 5V$		3 5			V
	$V_{CC} = 10V$		8			V
Logical "0" Input Voltage $V_{IN(0)}$	$V_{CC} = 5V$				1.5	V
	$V_{CC} = 10V$				2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	$V_{CC} = 5V$	$I_0 = -10\mu A$			0 5	V
	$V_{CC} = 10V$	$I_0 = -10\mu A$			1 0	V
Logical "0" Output Voltage $V_{OUT(0)}$	$V_{CC} = 5V$	$I_0 = +10\mu A$	4.5			V
	$V_{CC} = 10V$	$I_0 = +10\mu A$	9.0			V
Logical "1" Input Current $I_{IN(1)}$	$V_{CC} = 15V$	$V_{IN} = 15V$			1	μA
Logical "0" Input Current $I_{IN(0)}$	$V_{CC} = 15V$	$V_{IN} = 0V$	-1			μA
Supply Current I_{CC}	$V_{CC} = 15V$			01	5	μA
Input Capacitance	Any Input			5		pF
Propagation Delay Time to a Logical "1," t_{pd1}	$V_{CC} = 5V$	$C_L = 50$ pF, $T_A = 25°C$		40	90	ns
	$V_{CC} = 10V$	$C_L = 50$ pF, $T_A = 25°C$		25	60	ns
Propagation Delay Time to a Logical "0," t_{pd0}	$V_{CC} = 5V$	$C_L = 50$ pF, $T_A = 25°C$		40	90	ns
	$V_{CC} = 10V$	$C_L = 50$ pF, $T_A = 25°C$		25	60	ns
LOW POWER TO CMOS						
Logical "1" Input Voltage $V_{IN(1)}$	54C	$V_{CC} = 4\ 5V$	$V_{CC} - 1\ 5$			V
	74C	$V_{CC} = 4\ 75V$				
Logical "0" Input Voltage $V_{IN(0)}$	54C	$V_{CC} = 4\ 5V$			0.8	V
	74C	$V_{CC} = 4\ 75V$				
Logical "1" Output Voltage $V_{OUT(1)}$	54C	$V_{CC} = 4\ 5V$, $I_0 = -10\mu A$	0 4			
	74C	$V_{CC} = 4\ 75V$, $I_0 = -10\mu A$				
Logical "0" Output Voltage $V_{OUT(0)}$	54C	$V_{CC} = 4\ 5V$, $I_0 = +10\mu A$			4.4	V
	74C	$V_{CC} = 4\ 75V$, $I_0 = +10\mu A$				
Propagation Delay Time to a Logical "1," t_{pd1}	$V_{CC} = 5V$	$C_L = 15$ pF, $T_A = 25°C$		125		ns
Propagation Delay Time to a Logical "0," t_{pd0}	$V_{CC} = 5V$	$C_L = 15$ pF, $T_A = 25°C$		125		ns
CMOS TO LOW POWER						
Logical "1" Input Voltage $V_{IN(1)}$	54C	$V_{CC} = 4\ 5V$	4 0			V
	74C	$V_{CC} = 4\ 75V$				
Logical "0" Input Voltage $V_{IN(0)}$	54C	$V_{CC} = 4\ 5V$			1 0	V
	74C	$V_{CC} = 4\ 75V$				
Logical "1" Output Voltage $V_{OUT(1)}$	54C	$V_{CC} = 4\ 5V$, $I_0 = -100\mu A$	2 4			V
	74C	$V_{CC} = 4\ 75V$, $I_0 = -100\mu A$				
Logical "0" Output Voltage $V_{OUT(0)}$	54C	$V_{CC} = 4\ 5V$, $I_0 = 360\mu A$			0 4	V
	74C	$V_{CC} = 4\ 75V$, $I_0 = 360\mu A$				

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

CMOS

MM54C10/MM74C10 triple three-input NAND gate
MM54C20/MM74C20 dual four-input NAND gate

general description

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range No DC power other than that caused by leakage current is consumed during static conditions All inputs are protected against static discharge damage.

features

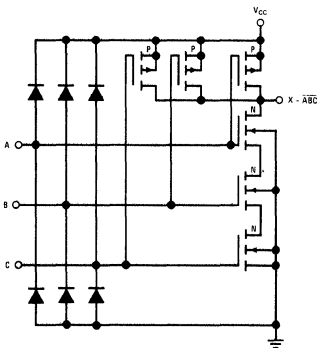
- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} typ
- Low power — 10 nW typ
- Low power T²L compatible — drive 2 LPT²L loads

applications

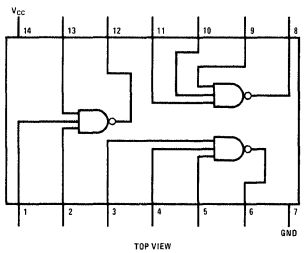
- Automotive
- Instrumentation
- Alarm systems
- Remote metering
- Data terminals
- Medical electronics
- Industrial controls
- Computers

schematic and connection diagrams

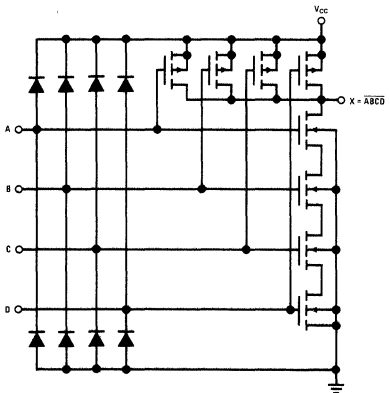
MM54C10/MM74C10



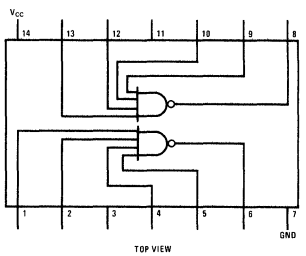
Dual-In-Line Package



MM54C20/MM74C20



Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $+V_{CC} + 0.3V$
Operating Temperature MM54C10, MM54C20	$-55^{\circ}C$ to $+125^{\circ}C$
MM74C10, MM74C20	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$
Operating V_{CC} Range	+3V to +15V

electrical characteristics

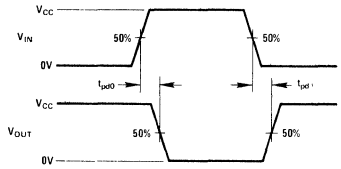
Min/Max limits apply across the guaranteed temperature range unless otherwise specified.

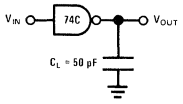
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS to CMOS						
Logical "1" Input Voltage V_{IN} (1)	$V_{CC} = 5.0V$		3.5			V
	$V_{CC} = 10.0V$		8.0			V
Logical "0" Input Voltage V_{IN} (0)	$V_{CC} = 5.0V$			1.5		V
	$V_{CC} = 10.0V$			2.0		V
Logical "1" Output Voltage V_{OUT} (1)	$V_{CC} = 5.0V$, $V_{IN} = 1.5$, $I_O = -10\,\mu A$		4.5			V
	$V_{CC} = 10.0V$, $V_{IN} = 2$, $I_O = -10\,\mu A$		9.0			V
Logical "0" Output Voltage V_{OUT} (0)	$V_{CC} = 5.0V$, $V_{IN} = 3.5$, $I_O = 10\,\mu A$				0.5	V
	$V_{CC} = 10.0V$, $V_{IN} = 8.0$, $I_O = 10\,\mu A$				1.0	V
Logical "1" Input Current I_{IN} (1)	$V_{CC} = 15V$, $V_{IN} = 15V$				1	μA
Logical "0" Input Current I_{IN} (0)	$V_{CC} = 15V$, $V_{IN} = 0V$		-1			μA
Supply Current I_{CC}	$V_{CC} = 15V$			0.01	2	μA
Input Capacitance	Any Input			7		pF
Propagation Delay Time to a Logical "0" t_{pd0}	54C10/74C10	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		50	90	ns
		$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		25	60	ns
	54C20/74C20	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		70	110	ns
		$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		30	75	ns
Propagation Delay Time to a Logical "1" t_{pd1}	54C10/74C10	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		60	100	ns
		$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		35	60	ns
	54C20/74C20	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		70	115	ns
		$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		40	80	ns
LOW POWER TTL to CMOS						
Logical "1" Input Voltage V_{IN} (1)	54C $V_{CC} = 4.5V$		$V_{CC} - 1.5$			V
	74C $V_{CC} = 4.75V$					
Logical "0" Input Voltage V_{IN} (0)	54C $V_{CC} = 4.5V$				0.8	V
	74C $V_{CC} = 4.75V$					
Logical "1" Output Voltage V_{OUT} (1)	54C $V_{CC} = 4.5V$, $I_O = -10\,\mu A$		4.4			V
	74C $V_{CC} = 4.75V$, $I_O = -10\,\mu A$					
Logical "0" Output Voltage V_{OUT} (0)	54C $V_{CC} = 4.5V$, $I_O = 10\,\mu A$				0.8	V
	74C $V_{CC} = 4.75V$, $I_O = 10\,\mu A$					
Propagation Delay Time to a Logical "0" $t_{pd(0)}$	$V_{CC} = 5.0V$, $C_L = 15$ pF, $T_A = 25^{\circ}C$			125		ns
Propagation Delay Time to a Logical "1" $t_{pd(1)}$	$V_{CC} = 5.0V$, $C_L = 15$ pF, $T_A = 25^{\circ}C$			125		ns
CMOS to Low Power TTL (tenth power)						
Logical "1" Input Voltage V_{IN} (1)	54C $V_{CC} = 4.5V$		4.0			V
	74C $V_{CC} = 4.75V$		4.0			V
Logical "0" Input Voltage V_{IN} (0)	54C $V_{CC} = 4.5V$				1.0	V
	74C $V_{CC} = 4.75V$				1.0	V
Logical "1" Output Voltage V_{OUT} (1)	54C10 $V_{CC} = 4.5V$, $V_{IN} = 1.0$, $I_O = -100\,\mu A$		2.4			V
	74C10 $V_{CC} = 4.75V$, $V_{IN} = 1.0$, $I_O = -100\,\mu A$		2.4			V
	54C20 $V_{CC} = 4.5V$, $V_{IN} = 0.8$, $I_O = -100\,\mu A$		2.4			V
	74C20 $V_{CC} = 4.75V$, $V_{IN} = 0.8$, $I_O = -100\,\mu A$		2.4			V
Logical "0" Output Voltage V_{OUT} (0)	54C $V_{CC} = 4.5V$, $V_{IN} = 4.0$, $I_O = 360\,\mu A$				0.4	V
	74C $V_{CC} = 4.75V$, $V_{IN} = 4.0$, $I_O = 360\,\mu A$				0.4	V
Propagation Time to a Logical "0" $t_{pd(0)}$	$V_{CC} = 5.0V$, $C_L = 50$ pF, $R_L = 20k$, $T_A = 25^{\circ}C$			60		ns
Propagation Time to a Logical "1" $t_{pd(1)}$	$V_{CC} = 5.0V$, $C_L = 50$ pF, $R_L = 20k$, $T_A = 25^{\circ}C$			45		ns

Note 1: These devices should not be connected under power on conditions.

switching time waveforms and ac test circuits

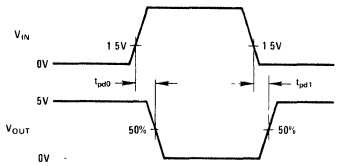
CMOS to CMOS

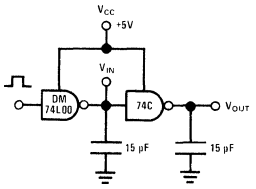




Test Circuit

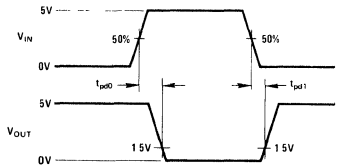
TTL to CMOS

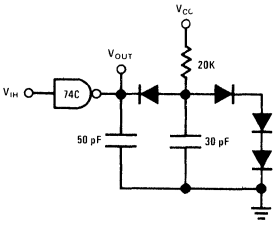




Test Circuit

CMOS to low power T^2L

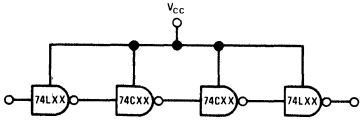




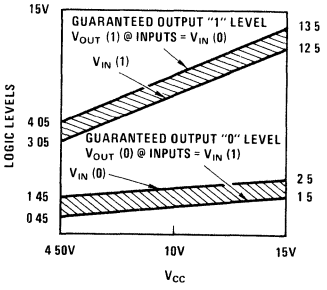
Test Circuit

applications

74C Compatibility



Guaranteed noise margin as a function of V_{CC}



CMOS

MM54C42/MM74C42 BCD to decimal decoder

general description

The MM54C42/MM74C42 one of ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1."

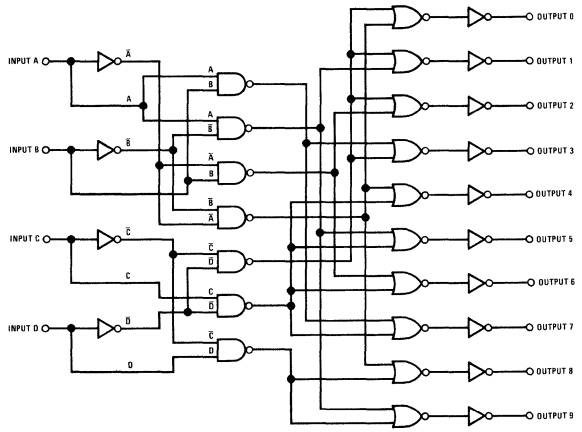
features

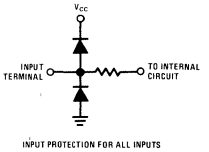
- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 10 MHz (typ.) with 10V V_{CC}

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

schematic diagram

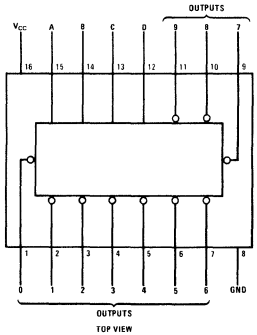




INPUT PROTECTION FOR ALL INPUTS

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature MM54C42	−55°C to +125°C
MM74C42	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperture (Soldering, 10 sec)	300°C

electrical characteristics Min/Max limits apply across temperature range unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 5.0V	3 5			V
		V_{CC} = 10 0V	8			V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 5 0V			1 5	V
		V_{CC} = 10.0V			2	V
Logical "1" Output Voltage	$V_{OUT(1)}$	V_{CC} = 5 0V, I_O = −10 μA	4.5			V
		V_{CC} = 10 0V, I_O = −10 μA	9.0			V
Logical "0" Output Voltage	$V_{OUT(0)}$	V_{CC} = 5 0V, I_O = +10 μA			0.5	V
		V_{CC} = 10 0V, I_O = +10 μA			1	V
Logical "1" Input Current	$I_{IN(1)}$	V_{CC} = 15 0V, V_{IN} = 15V			1	μA
Logical "0" Input Current	$I_{IN(0)}$	V_{CC} = 15.0V, V_{IN} = 0V	−1			μA
Supply Current	I_{CC}	V_{CC} = 15.0V		0 05	30	μA
Input Capacitance		Any Input		5		pF
Propogation Delay Time to a Logical "0" or Logical "1"		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	300	ns
		V_{CC} = 10 0V, C_L = 50 pF, T_A = 25°C		90	140	ns
CMOS TO TENTH POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V				
Logical "0" Input Voltage	$V_{IN(0)}$	54C, V_{CC} = 4 5V			0.8	V
		74C, V_{CC} = 4.75V				
Logical "1" Output Voltage	$V_{OUT(1)}$	54C, V_{CC} = 4 5V, I_O = −100 μA	2 4			V
		74C, V_{CC} = 4.75V, I_O = −100 μA				
Logical "0" Output Voltage	$V_{OUT(0)}$	54C, V_{CC} = 4 5V, I_O = 360 μA			0.4	V
		74C, V_{CC} = 4 75V, I_O = 360 μA				
Propagation Delay Time to a Logical "0" or Logical "1"		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250	400	ns

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

CMOS

MM54C73/MM74C73 dual J-K flip flop with clear
MM54C76/MM74C76 dual J-K flip flop with clear and preset
MM54C107/MM74C107 dual J-K flip flop with clear

general description

These dual JK flip flops are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement transistors. Each flip flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

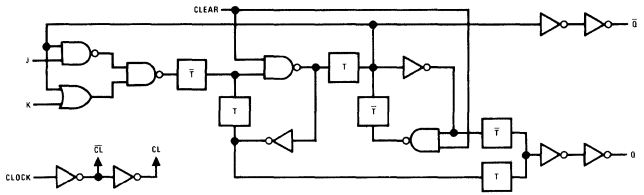
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ)
- Low power — 50 nW (typ)
- Medium speed operation — 10 MHz (typ) with 10V supply

applications

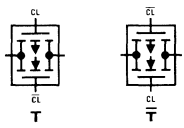
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

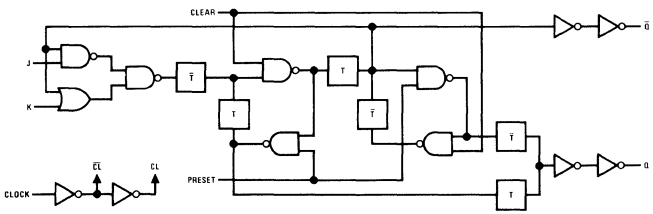
logic and connection diagrams



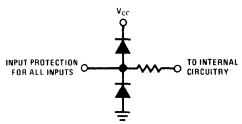
MM54C73/MM74C73 and MM54C107/MM74C107

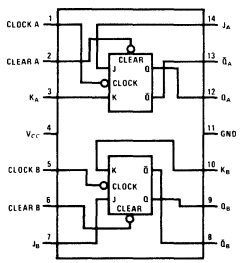
Transmission Gate



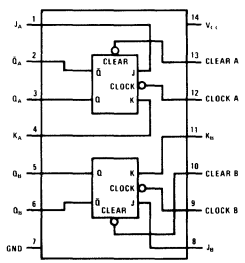


MM54C76/MM74C76

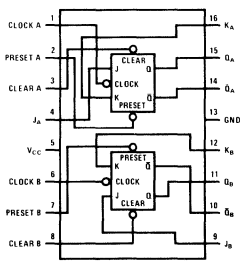




MM54C73/MM74C73



MM54C107/MM74C107



MM54C76/MM74C76

absolute maximum ratings

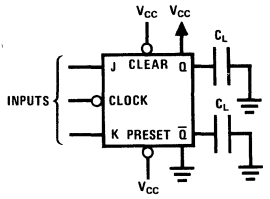
Voltage at any pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature MM54CXX	−55°C to 125°C
MM74CXX	0°C to 70°C
Storage Temperature	−65°C to 150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{CC} Range	+3V to 15V

electrical characteristics

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			1.5 2.0	V V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	4.5 9.0			V V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			0.5 1.0	V V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	10	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		180 80	300 130	ns ns
Propagation Delay Time to a Logical "0" From Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		200 80	300 130	ns ns
Propagation Delay Time to a Logical "1" From Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10 V, C_L = 50 pF, T_A = 25°C		200 80	300 130	ns ns
Time Prior to Clock Pulse That Data Must be Present, t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		90 40	130 60	ns ns
Time After Clock Pulse That J and K Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		−40 −20	0 0	ns ns
Minimum Clock Pulse Width t_{WL} = t_{WH}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90 40	130 60	ns ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90 40	130 60	ns ns
Maximum Toggle Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	2.5 5	5 10		MHz MHz
Clock Pulse Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C			15 5	μs μs
LOW POWER TTL TO CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Votlage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_0 = −100μA 74C, V_{CC} = 4.75V, I_0 = −100μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_0 = 360μA 74C, V_{CC} = 4.75V, I_0 = 360μA			0.4	V
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" From Clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250		ns

Note 1: These devices should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

ac test circuit



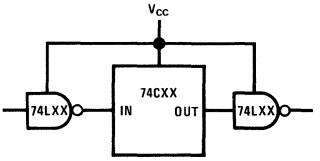
truth table

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

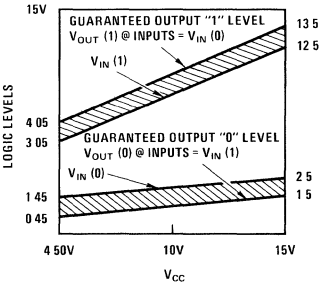
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

typical applications

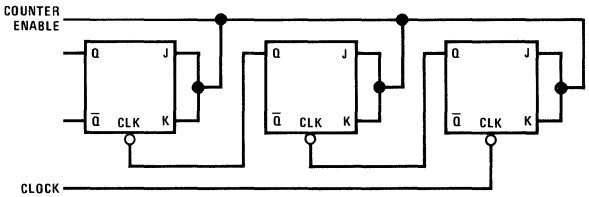
74C Compatibility



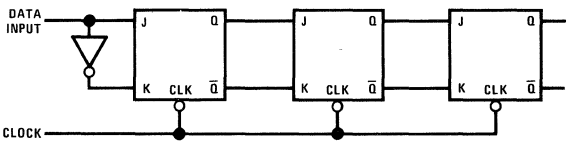
Guaranteed Noise Margin as a Function of V_{CC}



Ripple Binary Counters

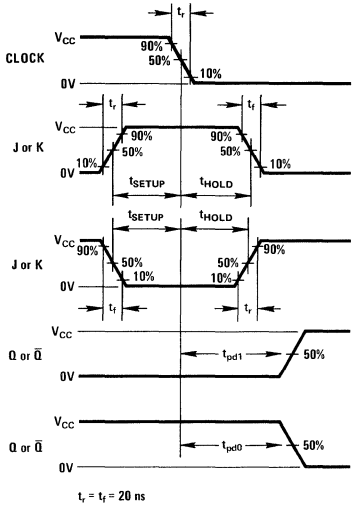


Shift Registers



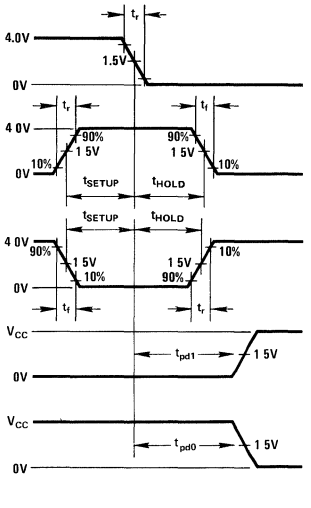
switching time waveforms

CMOS TO CMOS



$t_r = t_f = 20$ ns

TTL TO CMOS



CMOS

MM54C74/MM74C74 dual D flip flop

general description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

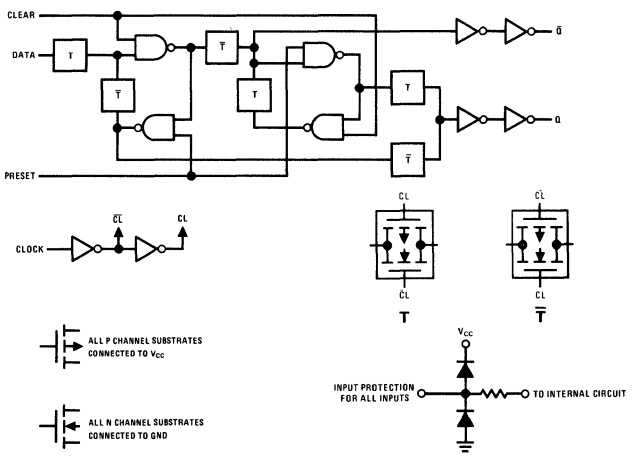
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2LPT^{2}L loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

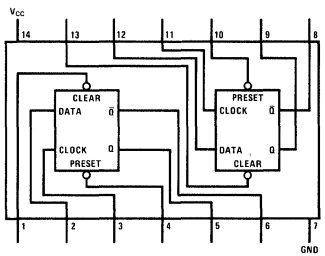
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams



Dual-In-Line Package



NOTE A logic "0" on clear sets Q to logic "0"
A logic "0" on preset sets Q to logic "1"

TOP VIEW

absolute maximum ratings

Voltage at any pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating temperature MM54C74	−55°C to 125°C
MM74C74	0°C to 70°C
Storage temperature	−65°C to 150°C
Package dissipation	500 mW
Lead temperature (Soldering, 10 sec)	300°C
Operating V_{CC} range	+3V to +15V

electrical characteristics

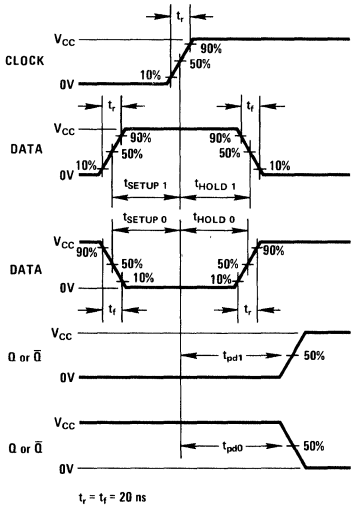
Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.01		μA
Input Capacitance	Any Input		5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70		ns
Propagation Delay Time to a Logical "0" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90		ns
Propagation Delay Time to a Logical "1" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90		ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		30		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		15		
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		70		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		30		ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		90		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40		ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF			5.0	μs
	V_{CC} = 10.0V, C_L = 50 pF			2.0	μs
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.75V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = −100 μA	2.4			V
	74C, V_{CC} = 4.75V, I_D = −100 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.50V, I_D = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_D = 360 μA				
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" from clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250		V

Note 1: These devices should not be connected under power on conditions

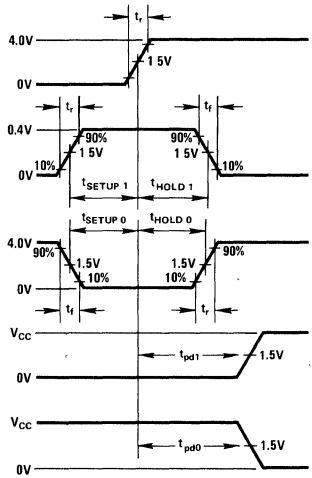
switching time waveforms

CMOS to CMOS

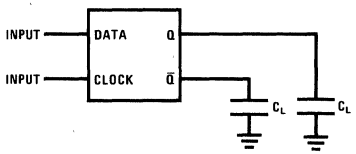


$t_r = t_f = 20$ ns

TTL to CMOS

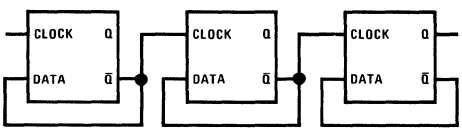


ac test circuit

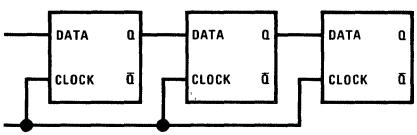


typical applications

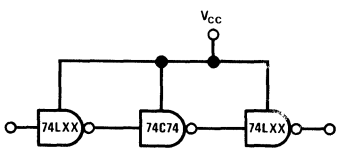
Ripple Counter (Divide by 2^n)



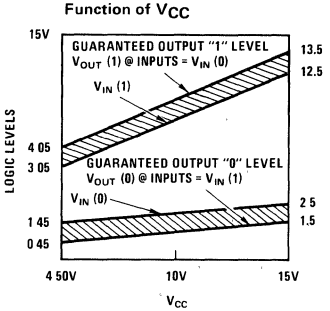
Shift Register



74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



CMOS

MM54C95/MM74C95 4-bit right-shift left-shift register

general description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right shift or left shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

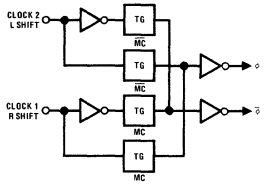
features

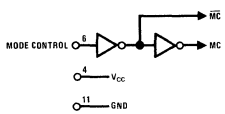
- Medium speed operation — 10 MHz typ (V_{CC} = 10V, C_L = 50 pF
- High noise immunity — 0 45 V_{CC} typ
- Low power — 100 nW typ
- Tenth power TTL compatible — Drive 2 LTTL loads
- Wide supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking

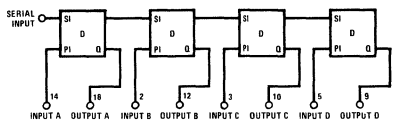
applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

block and connection diagrams

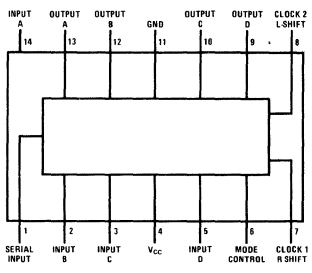






MODE CONTROL = 0 FOR RIGHT SHIFT
MODE CONTROL = 1 FOR LEFT SHIFT OR PARALLEL LOAD

Dual-In-Line Package



TOP VIEW

8

absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V	Package Dissipation		500 mW
Operating Temperature	MM54C95	−55°C to +125°C	Operating V_{CC} Range		+3V to +15V
	MM74C95	0°C to +70°C	Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature		−65°C to +150°C			

electrical characteristics

Max/min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			1.5 2	V V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	4.5 9			V V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			5 1	V V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.50	50	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\bar{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		200 80	400 160	ns ns
Time Prior to Clock Pulse That Data Must be Preset t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		15 10		ns ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C				ns ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		100 50		ns ns
Minimum Mode Control Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		100 40		ns ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	10 5			μs μs
Maximum Input Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		5 10	3 7	MHz MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = −100 μA 74C, V_{CC} = 4.75V, I_D = −100 μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_D = 360 μA 74C, V_{CC} = 4.75V, I_D = 360 μA			0.4	V
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\bar{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		175		ns

Note 1: These devices should not be connected under "Power On" conditions

CMOS

MM54C151/MM74C151 8 channel digital multiplexer

general description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the stroke input forces W to a logical "0" and Y to a logical "1".

All inputs are protected against electrostatic effects.

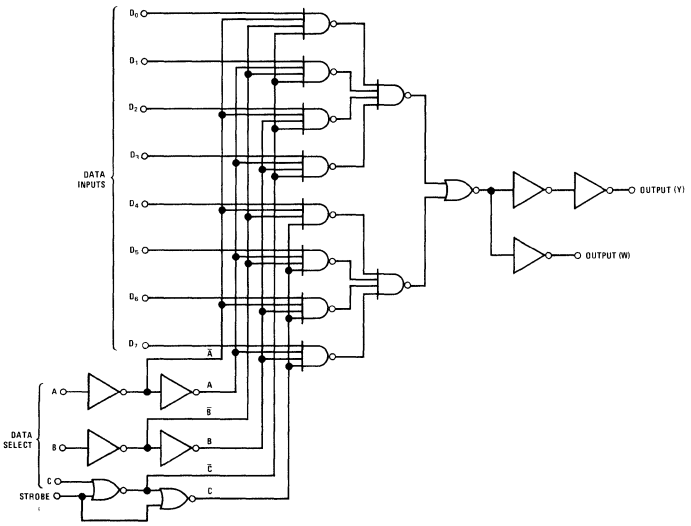
features

- Supply voltage range 3V to 15V
- Tenth power TTL drive 2 LPTTL loads compatible
- High noise immunity 0.45 V_{CC} typ
- Low power 50 nW typ

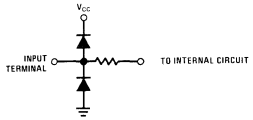
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

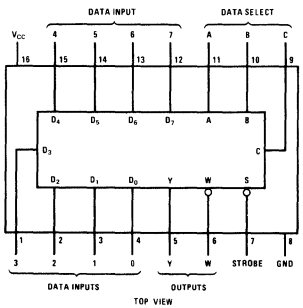
logic and connection diagrams



Input Protection For All Inputs



Dual-In-Line Package



8

absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V
Operating Temperature	MM54C151	−55°C to +125°C
	MM74C151	0°C to +70°C
Storage Temperature		−65°C to +150°C
Package Dissipation		500 mW
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

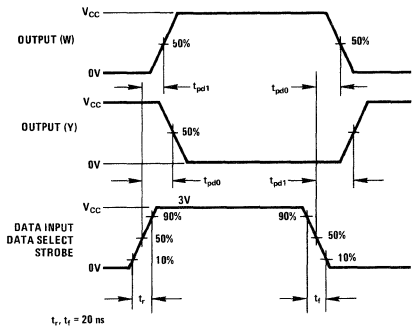
Min/Max limits apply across temperature range across otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10.0V	8			V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10.0V			2	V
Logical "1" Output Voltage	$V_{OUT(1)}$	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
		V_{CC} = 10.0V, I_O = −10 μA	9			V
Logical "0" Output Voltage	$V_{OUT(0)}$	V_{CC} = 5.0V, I_O = +10 μA			0.5	V
		V_{CC} = 10.0V, I_O = +10 μA			1	V
Logical "1" Input Current	$I_{IN(1)}$	V_{CC} = 15.0V, V_{IN} = 15V			1	μA
Logical "0" Input Current	$I_{IN(0)}$	V_{CC} = 15.0V, V_{IN} = 0V	−1			μA
Supply Current	I_{CC}	V_{CC} = 15.0V		0.05	30	μA
Input Capacitance		Any Input		5		pF
Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	270	ns
		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	130	ns
Propagation Delay Time to a Logical "0" or Logical "1" from Data to W		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	300	ns
		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	140	ns
Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	360	ns
		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		110	170	ns
CMOS TO TENTH POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V				
Logical "0" Input Voltage	$V_{IN(0)}$	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V				
Logical "1" Output Voltage	$V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −100 μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −100 μA				
Logical "0" Output Voltage	$V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360 μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360 μA				
Propagation Delay Time to a Logical "0" t_{pd0} or a Logical "1" t_{pd1} from Data Input, to Y		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	320	ns

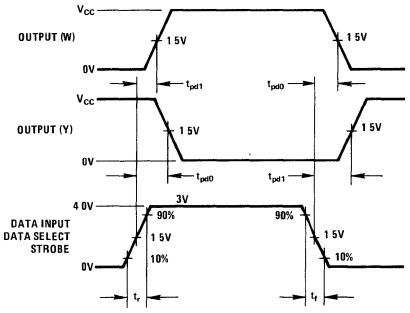
Note 1: This device should not be connected under power on conditions.

switching time waveforms

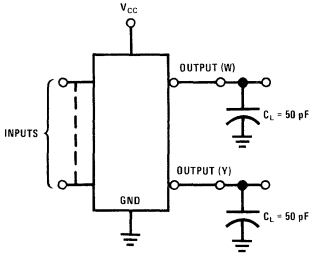
CMOS to CMOS (t_{pd1} & t_{pd0})



TTL to CMOS (t_{pd1} & t_{pd0})



ac test circuit



truth table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

CMOS

MM54C154/MM74C154 4-line to 16-line decoder/demultiplexer

general description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

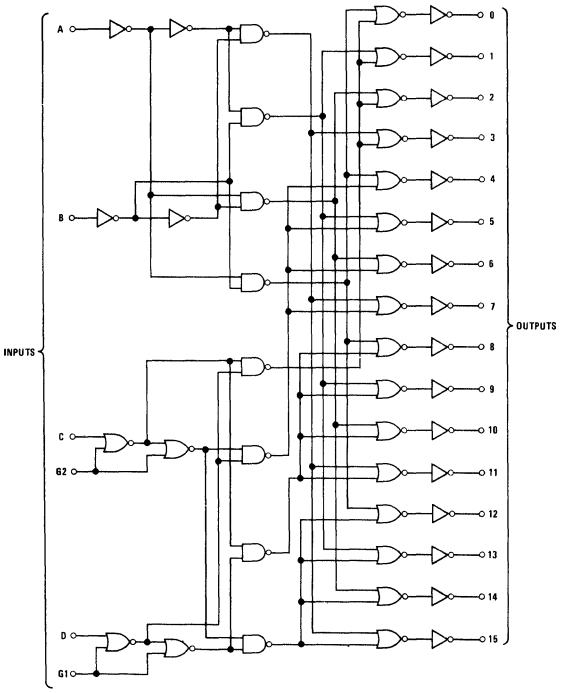
features

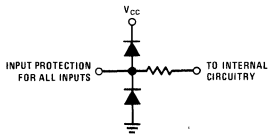
- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise margin 1V guaranteed
- High noise immunity 0.45 V_{CC} typ
- Low power 100μW typ

applications

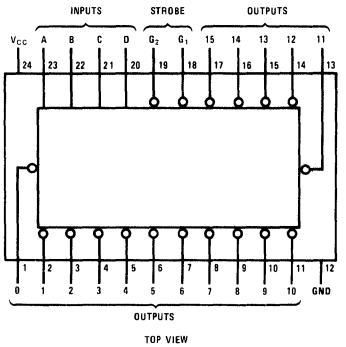
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams





Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C154	−55°C to +125°C
MM74C154	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating Range, V_{CC}	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

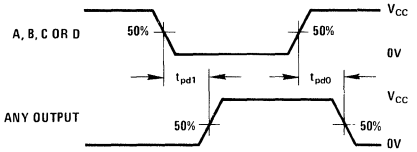
electrical characteristics

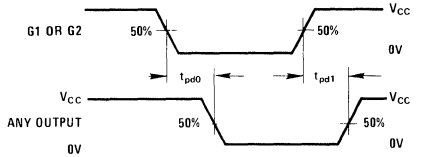
(Min/max limits apply across temperature range unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3 5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10 V			1 5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4 5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0 5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V			1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1			μA
Supply Current (I_{CC})	V_{CC} = 15V				μA
Input Capacitance	Any Input		5		pF
Propagation Delay to a Logical "0" From Any Input to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		275	400	ns
Propagation Delay to a Logical "0" From G1 or G2 to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		275	400	ns
Propagation Delay to a Logical "1" From Any Input to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		265	400	ns
Propagation Delay to a Logical "1" From G1 or G2 to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		265	400	ns
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4 5 74C V_{CC} = 4 75	V_{CC} − 1 5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4 5 74C V_{CC} = 4 75			0 8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4 5V, I_O = −100μA 74C V_{CC} = 4 75V, I_O = −100μA	2 4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4 5V, I_O = 360μA 74C V_{CC} = 4 75V, I_O = 360μA			0 4	V

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

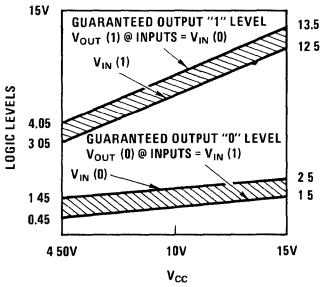
switching time waveforms





$t_r = t_f = 20$ ns

Guaranteed Noise Margin as a Function of V_{CC}



truth table

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

CMOS

MM54C157/MM74C157 quad 2-input multiplexer

general description

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement transistors. They consist of four 2-input multiplexers with a common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1" the outputs assume logical "0." Select decoding is done internally resulting in a single select input only.

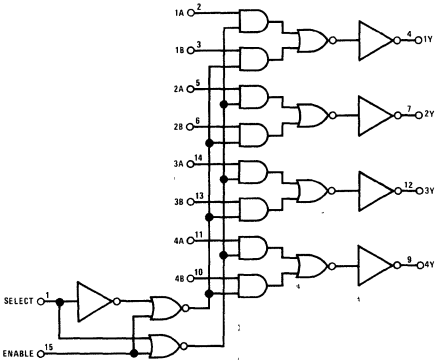
features

- Supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power — 50 nW (typ)
- Tenth power TTL compatible — drive 2 LPTTL loads

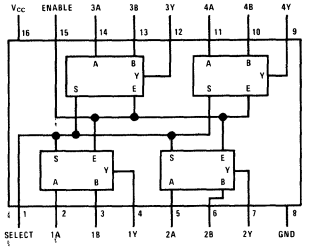
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

schematic and connection diagrams

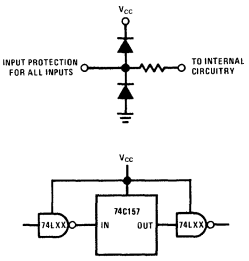


Dual-In-Line Package



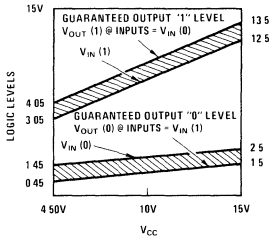
truth table

ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1



74L Compatibility

Guaranteed Noise Margin as a Function of V_{CC}



absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} to $0.3V$
Operating Temperature	MM54C157	$-55^{\circ}C$ to $125^{\circ}C$
	MM74C157	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature		$-65^{\circ}C$ to $150^{\circ}C$
Package Dissipation		500 nW
Lead Temperature (Soldering, 10 sec)		$300^{\circ}C$
Operating V_{CC} Range		+3V to 15V

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5 0V	3 5			V
	V_{CC} = 10 0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5 0V			1.5	V
	V_{CC} = 10 0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5 0V	4 5			V
	V_{CC} = 10 0V	9 0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5 0V			0.5	V
	V_{CC} = 10 0V			1 0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15 0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15 0V	-1 0			μA
Supply Current I_{CC}	V_{CC} = 15 0V		0.050	10	μA
Input Capacitance	Any Input		5		pF
Propagation Delay from Data to Output (t_{pd0} or t_{pd1})	V_{CC} = 5 0V C_L = 50 pF, T_A = $25^{\circ}C$		150	250	ns
	V_{CC} = 10 0V C_L = 50 pF, T_A = $25^{\circ}C$		70	110	ns
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	V_{CC} = 5 0V C_L = 50 pF, T_A = $25^{\circ}C$		180	300	ns
	V_{CC} = 10 0V C_L = 50 pF, T_A = $25^{\circ}C$		80	130	ns
Propagation Delay from Enable to Output (t_{pd0})	V_{CC} = 5 0V C_L = 50 pF, T_A = $25^{\circ}C$		180	300	ns
	V_{CC} = 10 0V C_L = 50 pF, T_A = $25^{\circ}C$		80	130	ns
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C V_{CC} = 4 5V	V_{CC} - 1 5			V
	74C V_{CC} = 4 75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C V_{CC} = 4 5V			0 8	V
	74C V_{CC} = 4 75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C V_{CC} = 4 5V, I_O = $-100\ \mu A$	2.4			V
	74C V_{CC} = 4 75V, I_O = $-100\ \mu A$				
Logical "0" Output Voltage $V_{OUT(0)}$	54C V_{CC} = 4.5V, I_O = $360\ \mu A$			0 4	V
	74C V_{CC} = 4 75V, I_O = $360\ \mu A$				
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	V_{CC} = 5 0V C_L = 50 pF, T_A = $25^{\circ}C$		250		ns

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

CMOS

MM54C160/MM74C160 decade counter with asynchronous clear
MM54C161/MM74C161 binary counter with asynchronous clear
MM54C162/MM74C162 decade counter with synchronous clear
MM54C163/MM74C163 binary counter with synchronous clear

general description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

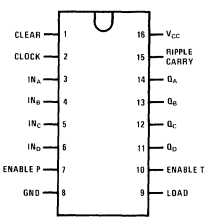
features

- High noise margin — 1V guaranteed
- High noise immunity — 0.45 V_{CC} typ
- Tenth power TTL compatible — drives 2 LPTTL loads
- Wide supply voltage range — 3V to 15V
- Internal look-ahead for fast counting scemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

connection diagram

(For Logic Diagrams See Page 3)

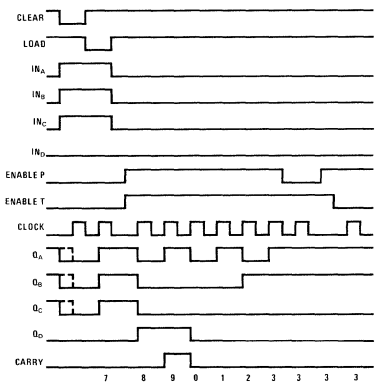
Dual-In-Line Package



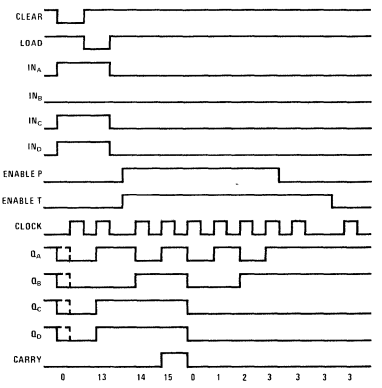
TOP VIEW

logic waveforms

C160, --- C162 Decade Counters



C161, --- C163 Binary Counters



8

absolute maximum ratings

Voltage at Any Pin (Note 1)	−0 3V to V_{CC} +0.3V
Operating Temperature MM54C160/1/2/3	−55°C to +125°C
MM74C160/1/2/3	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

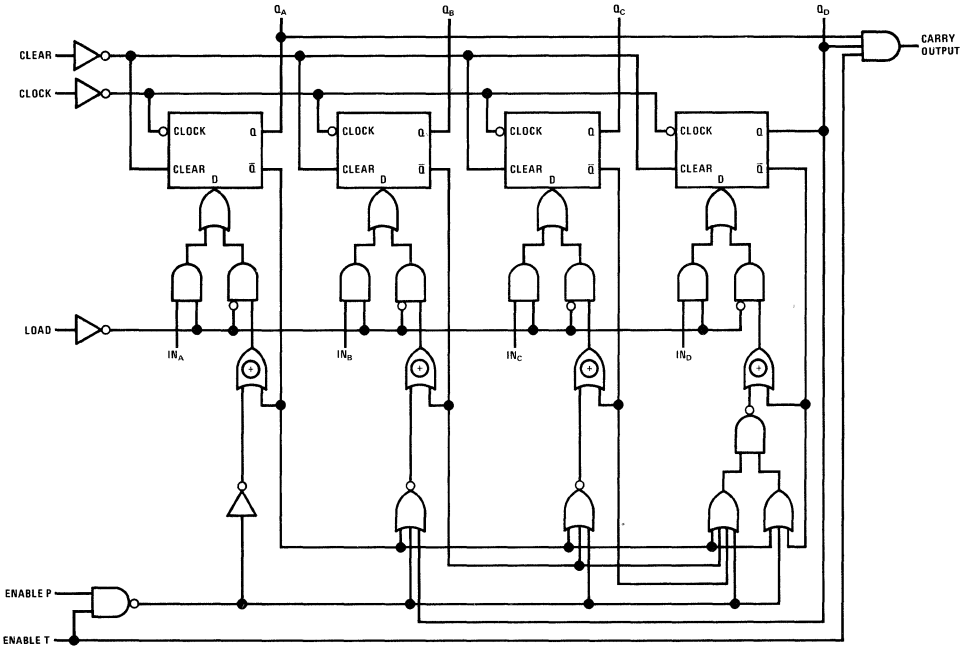
electrical characteristics Min/Max limits apply across temperature range unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS to CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5V	3 5			V
	V_{CC} = 10V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5V			1 5	V
	V_{CC} = 10V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5V I_O = −10 μA	4 5			V
	V_{CC} = 10V I_O = −10 μA	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5V I_O = +10 μA			0 5	V
	V_{CC} = 10V I_O = +10 μA			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15V V_{IN} = 15V			1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15V V_{IN} = 0V	−1			μA
Supply Current I_{CC}	V_{CC} = 15V		0 05	50	μA
Input Capacitance	Any Input		5		pF
Propagation delay time from clock to Q t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		250		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		90		ns
Propagation delay time from clock to carry out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		290		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120		ns
Propagation delay time from T enable to carry out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		160		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		70		ns
Propagation time from clear to Q (C162 and C163 only) t_{pd0}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		190		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		80		ns
Time prior to clock that data or load must be present t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		90		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		30		ns
Time prior to clock that enable P or T must be present t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		170		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		70		ns
Time prior to clock that clear must be present (162, 163 only) t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		50		ns
Minimum clock pulses width t_{WL} or t_{WH}	V_{CC} = 5V; C_L = 50 pF, T_A = 25°C		90		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		35		ns
Maximum clock rise or fall time	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C			15	μs
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C			5	μs
Maximum clock frequency	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		5		MHz
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		12		MHz
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage	54C V_{CC} = 4.5V	V_{CC} − 1 5			
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage	54C V_{CC} = 4.5V			0 8	
	74C V_{CC} = 4 75V				
Logical "1" Output Voltage	54C V_{CC} = 4.5V I_O = −100 μA	2.4			
	74C V_{CC} = 4.75V				
Logical "0" Output Voltage	54C V_{CC} = 4 5V I_O = 380 μA				
	74C V_{CC} = 4 75V			0.4	

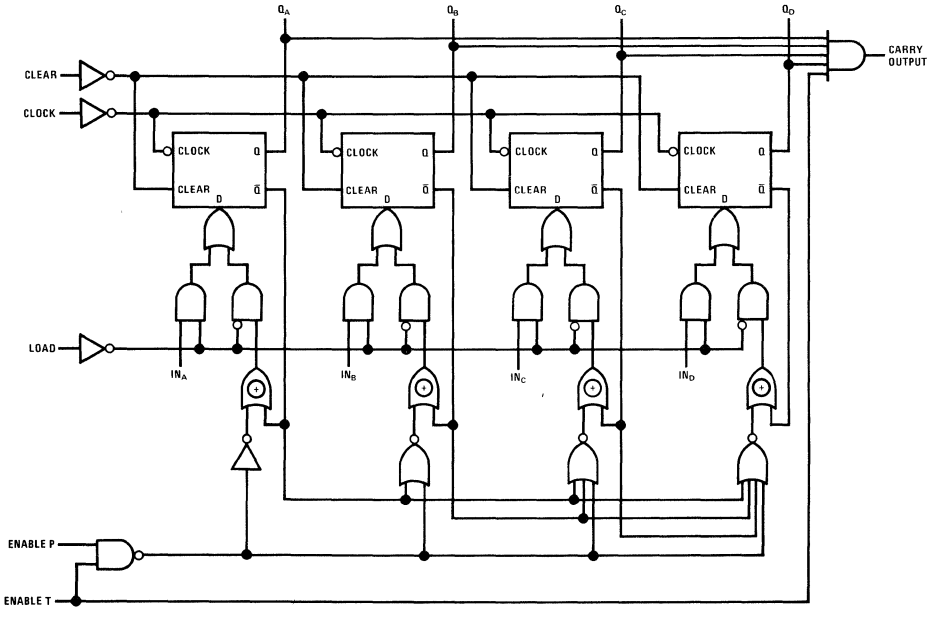
Note 1: This device should not be connected during power on conditions

logic diagrams

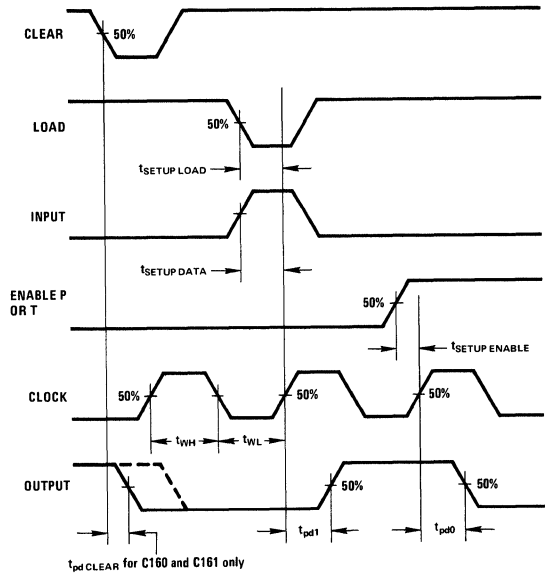
Logic Diagram C160/C162; Clear is Sychronous for the C162



Logic Diagram C161/C163; Clear is Synchronous for the C163



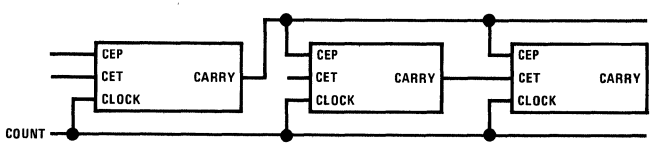
switching time waveforms



NOTE 1: ALL INPUT PULSES ARE FROM GENERATORS HAVING THE FOLLOWING CHARACTERISTICS: $t_r = t_f = 20$ ns PRR ≤ 1 MHz DUTY CYCLE $\leq 50\%$, $Z_{OUT} \approx 50\Omega$.

NOTE 2. ALL TIMES ARE MEASURED FROM 50% TO 50%.

cascading packages



CMOS

MM54C164/MM74C164
8-bit parallel-out serial shift registers

general description

The MM54C164/MM74C164 shift registers are are a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. A high-level input enables the other input which will then determine the state of the first flip flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

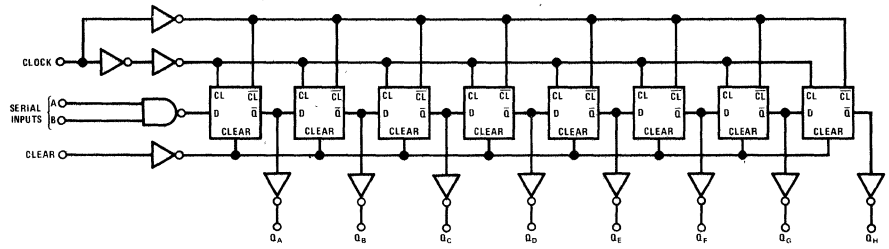
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} typ
- Low power — 50 mW typ
- Medium speed operation — 10 MHz typ with 10V supply

applications

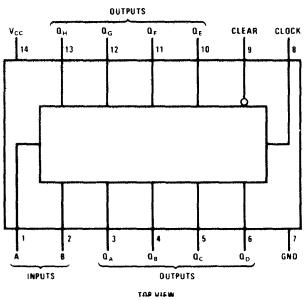
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote meterly
- Computers

block diagram



connection diagram

Dual-In-Line Package



truth table

Serial Inputs A and B

INPUTS t_n		OUTPUT t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V
Operating Temperature	MM54C164	−55°C to +125°C
	MM74C164	0°C to +70°C
Storage Temperature		−65°C to +150°C
Package Dissipation		500 mW
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		300°C

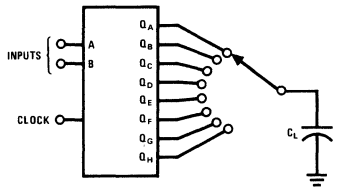
electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

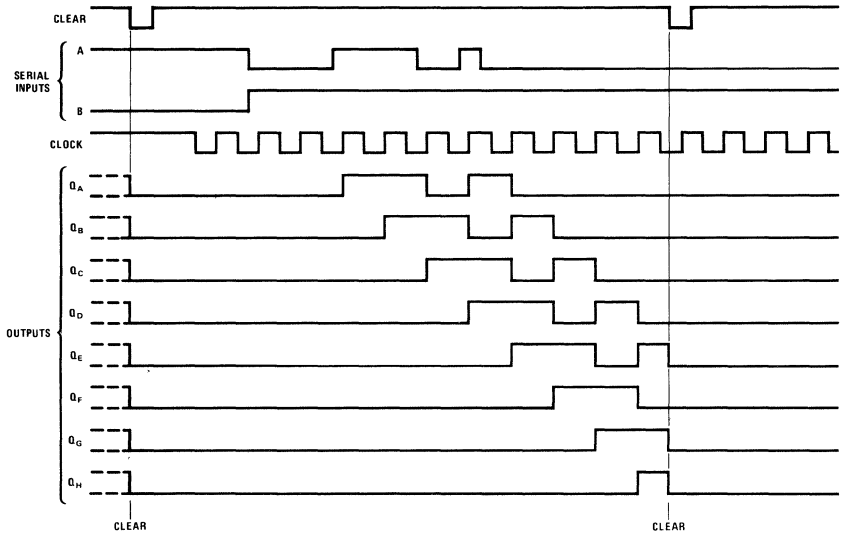
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V I_O = −10 μA	4.5			V
	V_{CC} = 10.0V I_O = −10 μA	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V I_O = −10 μA			5	V
	V_{CC} = 10.0V I_O = −10 μA			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V V_{IN} = 15V			1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V V_{IN} = 0V	−1			μA
Supply Current I_{CC}	V_{CC} = 15.0V		.05	50	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" or	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		230	310	ns
Logical "1" From Clock to Q	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	120	ns
Propagation Delay Time to a Logical "1" From	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		280	380	ns
Clear to Q	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		110	150	ns
Time Prior to Clock Pulse That Data Must be	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		110		ns
Present t_{SETUP}	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		30		ns
Time After Clock Pulse That Data Must be	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
Held	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		120		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		50		ns
Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		150		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		55		ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		1		ms
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		130		μs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C V_{CC} = 4.5V	V_{CC}−1.5			V
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C V_{CC} = 4.5V			8	V
	74C V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C V_{CC} = 4.5V, I_O = −100 μA	2.4			V
	74C V_{CC} = 4.75V, I_O = −100 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C V_{CC} = 4.5V, I_O = 360 μA			4	V
	74C V_{CC} = 4.75V, I_O = 360 μA				
Propagation Delay Time to a Logical "0" or Logical "1" From Clock To Q			320		ns

Note 1: These devices should not be connected under power on conditions.

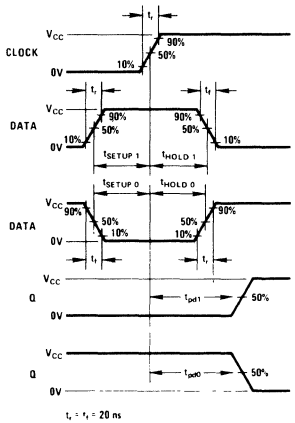
ac test circuit



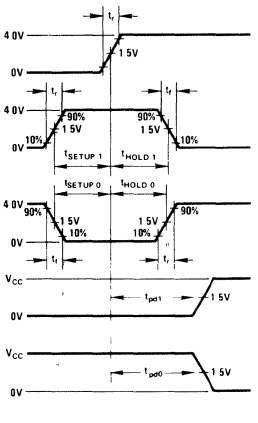
switching time waveforms



CMOS to CMOS

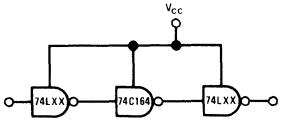


TTL to CMOS

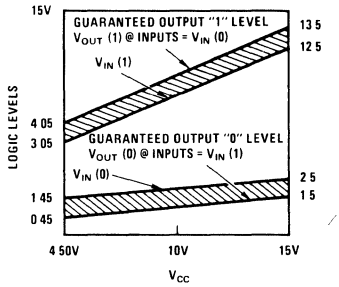


typical applications

74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



CMOS

MM54C173/MM74C173 TRI-STATE® quad D flip flop

general description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors The four D type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive going transition.

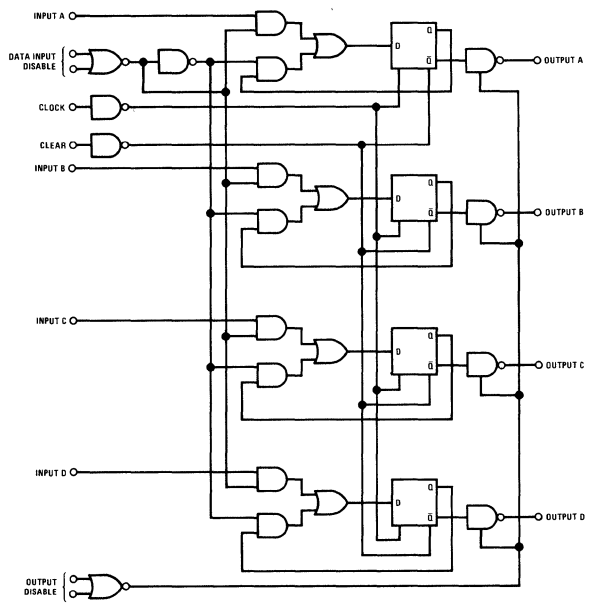
features

- Supply voltage range 3V to 15V
- Tenth power TTL compatible Drive 2 LPTTL loads
- High noise immunity 0 45 V_{CC} typ
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disabled without gating the clock

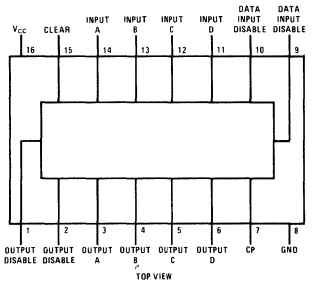
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams



Dual-In-Line Package



8

absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3 to V_{CC} +0.3V
Operating Temperature	MM54C173	−55°C to +125°C
	MM74C173	0°C to +70°C
Storage Temperature		−65°C to +150°C
Package Dissipation		500 mW
Operating V_{CC} Range		+3V to +15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			.5	V
	V_{CC} = 10.0V			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1	μA
Logical "0" Input Current $I_{IN(0)}$		−1			μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		001		μA
	V_{CC} = 15V, V_O = 0V		.001		μA
Supply Current I_{CC}	V_{CC} = 15V		001	10	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		220	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	200	ns
Input Data Setup Time, $t_{S\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		40	80	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		15	30	ns
Input Data Hold Time, $t_{H\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Input Disable Setup Time, $t_{S\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		35	70	ns
Input Disable Hold Time, $t_{H\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Delay From Output Disable to High Impedance State (From Logical "1" or Logical "0" Level), t_{IH}, t_{OH}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "1" Level, t_{HI} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "0" Level, t_{HO} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Propagation Delay From Clear to Output t_{pdR}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	490	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	180	
Maximum Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		5	3 5	MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		10	7	
Minimum Clear Pulse Width	V_{CC} = 5 0V, C_L = 50 pF, T_A = 25°C		150		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70		
Maximum Clock Rise and Fall Time	V_{CC} = 5 0V, C_L = 50 pF	10			μs
	V_{CC} = 10.0V, C_L = 50 pF	5			μs

Note 1: These devices should not be connected under "Power On" conditions.

electrical characteristics (con't)

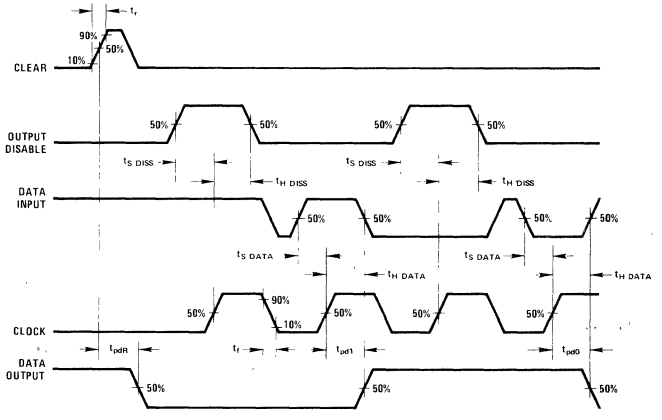
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} −1.5			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −100μA 74C, V_{CC} = 4.75V, I_O = −100μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			4	V
Propagation Delay Time to a Logical "0", t_{pd0} or Logical "1" t_{pd1} From Clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		500		ns

truth table

Truth Table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

switching time waveforms



CMOS

MM54C192/MM74C192 synchronous 4-bit up/down decade counter
MM54C193/MM74C193 synchronous 4-bit up/down binary counter

general description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters. While the MM54C193 and MM74C193 are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive going transition of this clock.

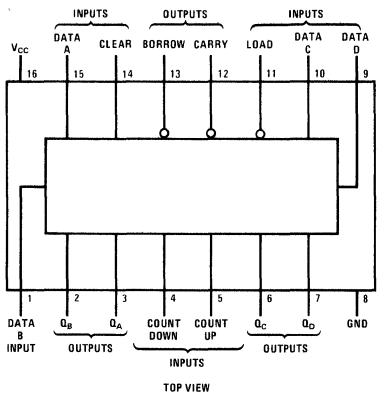
These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1." The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

features

- High noise margin — 1V guaranteed
- Tenth power TTL compatible — drive 2 LPTTL loads
- Wide supply range — 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} typ

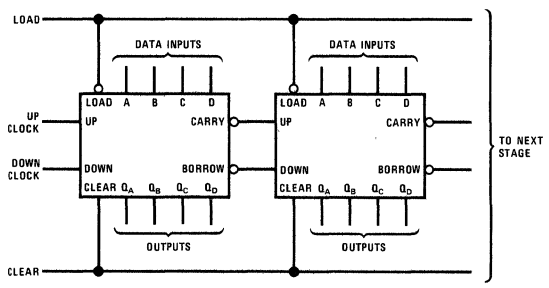
connection diagram

Dual-In-Line Package

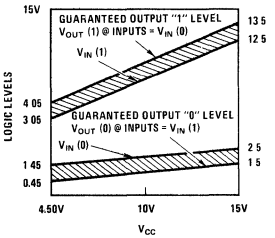


TOP VIEW

cascading packages



Guaranteed Noise Margin as A Function of V_{CC}



absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C192, MM54C193	−55°C to +125°C
MM74C192, MM74C193	−70°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

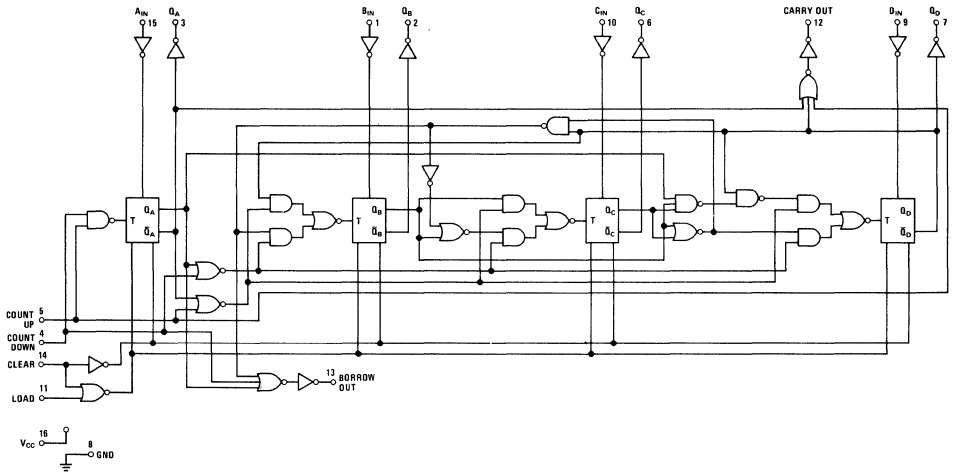
electrical characteristics (Min/max limits apply across temperature range unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO MOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3 5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10V			1 5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4 5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0 5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V			1 0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1 0			μA
Supply Current (I_{CC})	V_{CC} = 15V			50	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to Q From Count Up or Down (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		250 100	400 160	ns ns
Propagation Delay Time to Borrow From Count Down (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120 50	200 80	ns ns
Propagation Delay Time to Carry From Count Up (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120 50	200 80	ns ns
Time Prior to Load That Data Must be Present (t_{SETUP})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100 30	160 50	ns ns
Minimum Clear Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF T_A = 25°C		300 120	480 190	ns ns
Minimum Load Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100 40	160 65	ns ns
Propagation Delay Time to Q From Load (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		300 120	480 190	ns ns
Minimum Count Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120 35	200 80	ns ns
Maximum Count Frequency	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C	2 5 6	4 10		MHz MHz
Count Rise and Fall Time	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C			15 5	μs μs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4 5V 74C V_{CC} = 4 75V	V_{CC}−1 5 V_{CC}−1 5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4 5V 74C V_{CC} = 4 75V			0 8 0 8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4 5V, I_O = −100μA 74C V_{CC} = 4 75V, I_O = −100μA	2 4 2 4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4 5V, I_O = 360μA 74C V_{CC} = 4 75V, I_O = 360μA			0 4 0 4	V V

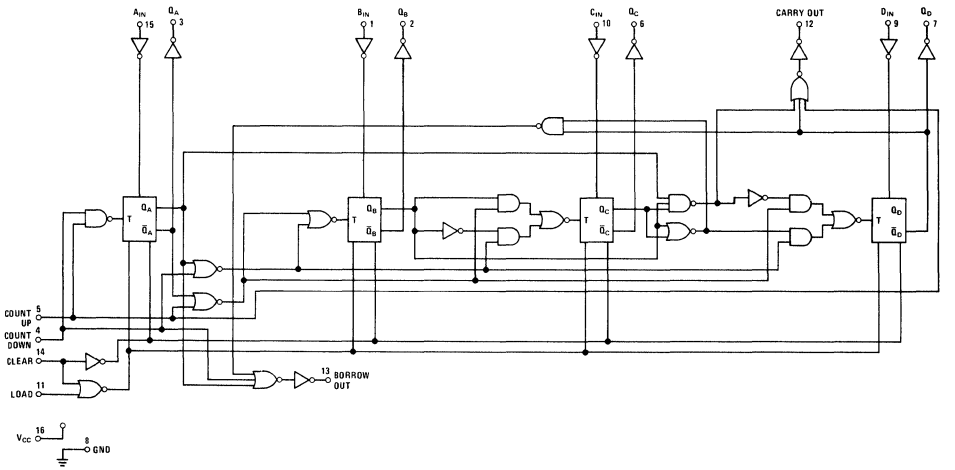
Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

8

schematic diagrams



MM54C192 Synchronous 4-Bit Up/Down Decade Counter



MM54C193 Synchronous 4-Bit Up/Down Binary Counter

CMOS

MM54C195/MM74C195 4-bit register

general description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, $J\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The following two modes of operation are possible:

Parallel Load

Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the $J\overline{K}$ inputs. These inputs allow the first stage to perform as a $J\overline{K}$, D or T-type flip flop as shown in the truth table.

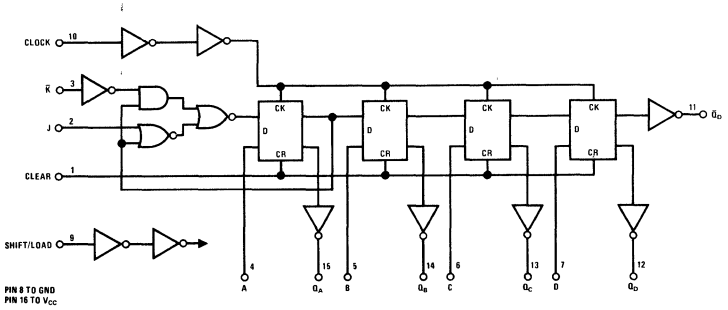
features

- Medium speed operation — 10 MHz (typ) with 10V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ)
- Low power — 100 nW (typ)
- Tenth power TTL compatible — drive 2 LPTTL loads
- Supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- Positive edge triggered clocking
- Diode clamped inputs to protect against static charge

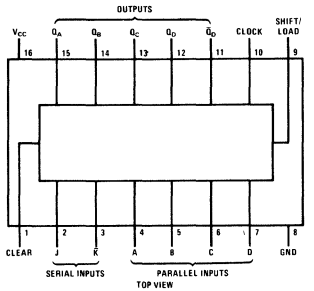
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

schematic and connection diagrams



Dual-In-Line Package



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absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	MM54C195	$-55°C$ to $+125°C$
	MM74C195	$0°C$ to $+70°C$
Storage Temperature		$-65°C$ to $150°C$
Package Dissipation		500 mW
Lead Temperature (Soldering, 10 sec)		$300°C$
Operating V_{CC} Range		$+3V$ to $+15V$

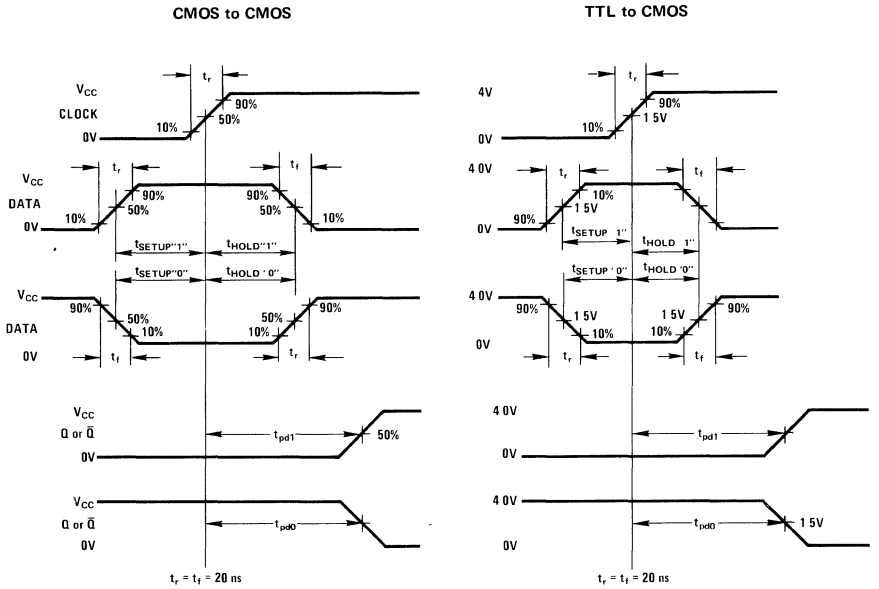
electrical characteristics

Max/Min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage $V_{IN(1)}$	$V_{CC} = 5.0V$		3.0			V
	$V_{CC} = 10.0V$		8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	$V_{CC} = 5.0V$				1.5	V
	$V_{CC} = 10.0V$				2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	$V_{CC} = 5.0V$		4.5			V
	$V_{CC} = 10.0V$		9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	$V_{CC} = 5.0V$				0.5	V
	$V_{CC} = 10.0V$				1.0	V
Logical "1" Input Current $I_{IN(1)}$	$V_{CC} = 15.0V$				1.0	μA
Logical "0" Input Current $I_{IN(0)}$	$V_{CC} = 15.0V$		1.0			μA
Supply Current I_{CC}	$V_{CC} = 15.0V$			0.050	20	μA
Input Capacitance	Any Input			5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		200	300	ns
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$		75	130	ns
Propagation Delay Time to a Logical "0" From Clear	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		100	300	ns
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$		50	130	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		60	100	ns
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$		15	50	ns
Time Prior to Clock Pulse That Shift/Load Must be Present t_{SETUP}	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		110	150	ns
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$		60	90	ns
Time After Clock Pulse That Data Must be Held	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		-10	0	ns
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$		-5	0	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		100	200	ns
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$		50	100	ns
Minimum Clear Pulse Width	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		90	130	ns
	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		40	60	ns
Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$	$C_L = 50$ pF	5.0			μs
	$V_{CC} = 10.0V$	$C_L = 50$ pF	2.0			μs
Maximum Input Clock Frequency	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$	2.5	5		MHz
	$V_{CC} = 10.0V$	$C_L = 50$ pF, $T_A = 25°C$	5	10.0		MHz
LOW POWER TTL/CMOS INTERFACE						
Logical "1" Input Voltage $V_{IN(1)}$	54C	$V_{CC} = 4.5V$	$V_{CC}-1.5$			V
	74C	$V_{CC} = 4.75V$				
Logical "0" Input Voltage $V_{IN(0)}$	54C	$V_{CC} = 4.5V$			0.8	V
	74C	$V_{CC} = 4.75V$				
Logical "1" Output Voltage $V_{OUT(1)}$	54C	$V_{CC} = 4.5V$, $I_D = -100\ \mu A$	2.4			V
	74C	$V_{CC} = 4.75V$, $I_D = -100\ \mu A$				
Logical "0" Output Voltage $V_{OUT(0)}$	54C	$V_{CC} = 4.5V$, $I_D = 360\ \mu A$			0.4	V
	74C	$V_{CC} = 4.75V$, $I_D = 360\ \mu A$				
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$	$C_L = 50$ pF, $T_A = 25°C$		250		ns

Note 1: These devices should not be connected under power on conditions.

switching time waveforms

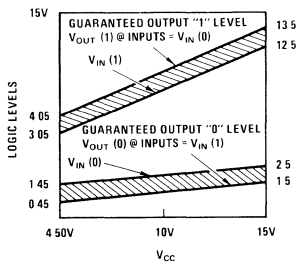


truth table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed noise Margin as a Function of V_{CC}



8

Interface Circuits

REFERENCE

The following table references all Physical Dimension Drawings for the devices in this section. For Order Numbers, see below.* Refer to the alpha-numerical index at the front of this catalog for complete device title and function. Packages (pages I thru VI) are in the back of the catalog.

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
		Fig.	Pg.	Fig.	Pg.	Type	Fig.	Pg.	Type	Fig.	Pg.	Type		Fig.	Pg.	Fig.	Pg.
DH0006	9-1									21	V	H					
DH0006C	9-1	2	II							21	V	H					
DH0008	9-4									21	V	H					
DH0008C	9-4	2	II							21	V	H					
DH0011	9-7									21	V	H					
DH0011C	9-7	2	II							21	V	H					
DH0011CN	9-7	2	II							21	V	H					
DH0016CN	9-10	2	II														
DH0017CN	9-10	2	II														
DH0018CN	9-10	2	II														
DH0028C	9-13	2	II							21	V	H					
DH0028CN	9-13	2	II							21	V	H					
DH0034	9-15			11	IV	J				21	V	H					
DH0034C	9-15			11	IV	J				21	V	H					
DH0035	9-18									24	VI	G					
DH0035C	9-18									24	VI	G					
DH3467C	9-20	3	II														
DH3725C	9-22	3	II														
LH2111	9-24			9	III	D	16	V	F								
LH2211	9-24			9	III	D	16	V	F								
LH2311	9-24			9	III	D	16	V	F								
LM106	9-26						15	IV	F	20	V	H					
LM206	9-26									20	V	H					
LM306	9-28									20	V	H					
LM111	9-30			8	III	D	14	IV	F	20	V	H					
LM211	9-30			8	III	D	14	IV	F	20	V	H					
LM311	9-35	3	II	8	III	D	14	IV	F	20	V	H					
LM350	9-40	3	II														
LM710	9-42	1	II							20	V	H					
LM710C	9-44	3	II							23	VI	H					
LM711	9-46									22	V	H					
LM711C	9-48	3	II							23	VI	H					
LM1414	9-55	3	II	11	IV	J											
LM1514	9-55			11	IV	J											
LM1488	9-50			11	IV	J											
LM1489, A	9-53			11	IV	J											
LM5520	9-58			12	IV	J											
LM7520	9-58	5	II	12	IV	J											
LM5521	9-58			12	IV	J											
LM7521	9-58	5	II	12	IV	J											
LM5522	9-61			12	IV	J											
LM7522	9-61	5	II	12	IV	J											
LM5523	9-61			12	IV	J											
LM7523	9-61	5	II	12	IV	J											
LM5524	9-63			12	IV	J											
LM7524	9-63	5	II	12	IV	J											
LM5525	9-63			12	IV	J											
LM7525	9-63	5	II	12	IV	J											
LM5528	9-65			12	IV	J											
LM7528	9-65	5	II	12	IV	J											
LM5529	9-65			12	IV	J											
LM7529	9-65	5	II	12	IV	J											
LM5534	9-67			12	IV	J											
LM7534	9-67	5	II	12	IV	J											

*Order Numbers: use Device No. suffixed with package letter, i.e. DH0006H.

DATA SHEETS		PACKAGES												WAVE-FORMS		TEST CIRCUITS	
Devices	Pg.	Molded DIP (N)		Cavity DIP (D)(J)			Flat Pack (F)(W)			Metal Can (G)(H)							
		Fig.	Pg.	Fig	Pg	Type	Fig.	Pg.	Type	Fig.	Pg.	Type		Fig.	Pg.	Fig.	Pg.
LM5535	9-67			12	IV	J											
LM7535	9-67	5	II	12	IV	J											
LM5538	9-69			12	IV	J											
LM7538	9-69	5	II	12	IV	J											
LM5539	9-69			12	IV	J											
LM7539	9-69	5	II	12	IV	J											
LM75450A	9-40	3	II														
LM75451A	9-71	1	II														
LM75452	9-71	1	II														
LM75453	9-71	1	II														
LM75454	9-73	1	II														
MH0007	9-75									22	V	H					
MH0007C	9-75									22	V	H					
MH0009	9-77									24	V	G					
MH0009C	9-77									24	V	G					
MH0012	9-79									24	VI	G					
MH0012C	9-79									24	VI	G					
MH0013	9-81									24	VI	G					
MH0013C	9-81									24	VI	G					
MH0025	9-85									20	VI	H					
MH0025C	9-85	1	II							20	V	H					
MH0026	9-88									24	VI	G					
MH0026C	9-88	1	II							20	V	H					
MH0027C	9-97	1	II														
MH8808	9-99	5	II														

Interface Circuits

DH0006/DH0006C*current driver

general description

The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28 volts. AND inputs are provided along with an Expander connection, should additional gating be required The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven

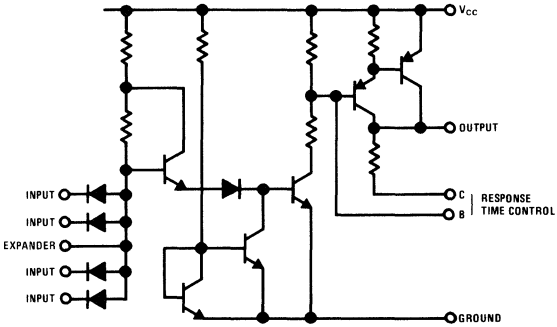
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

*Previously called NH0006/NH0006C

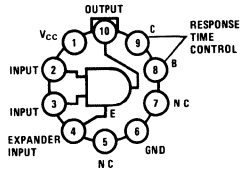
features

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply
- 1.5A, 50 ms, Pulse Current Capability.

schematic and connection diagrams

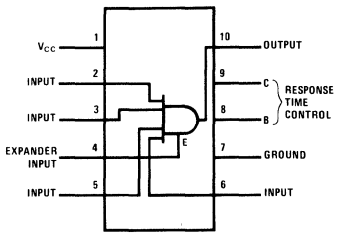


Metal Can Package



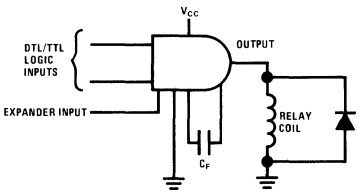
TOP VIEW

Dual-In-Line Package

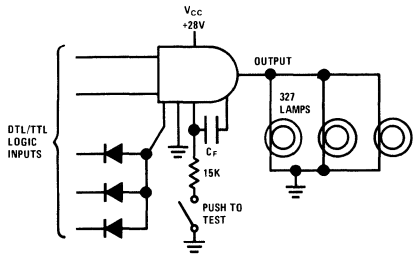


typical applications

Relay Driver



Lamp Driver with Expanded Inputs



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absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
DH0006	−55°C to +125°C
DH0006C, DH0006CN	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		.001	.01	V
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9 2		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = .4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2 0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		μs
Fall Time	V_{CC} = 28V, R_L = 82Ω		0.8		μs
T_{on}	V_{CC} = 28V, R_L = 82Ω		0.26		μs
T_{off}	V_{CC} = 28V, R_L = 82Ω		2.2		μs

Note 1: Unless otherwise specified, limits shown apply from −55°C to 125°C for DH0006 and 0°C to 70°C for DH0006C.

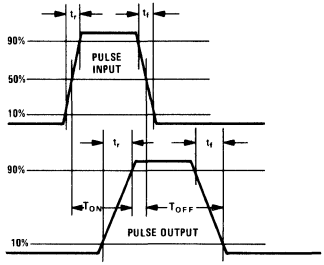
Note 2: Typical values are for 25°C ambient

Note 3. Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ_{JA} of 210°C/W

Note 4: Power rating for the DH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 175°C/W when mounted in a standard DIP socket

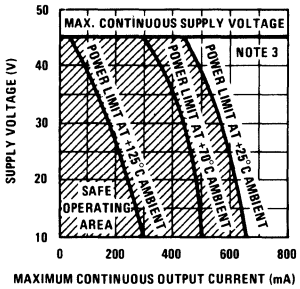
Note 5: Power rating for the DH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 150°C/W when mounted on a 1/16 inch thick, epoxy-glass board with ten 0 03 inch wide 2 ounce copper conductors

switching time waveforms

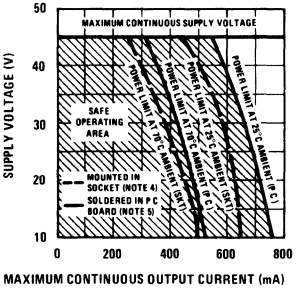


typical performance

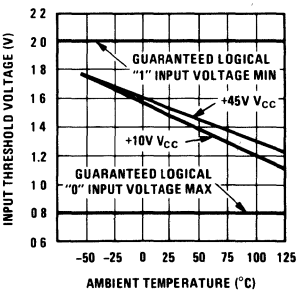
Maximum Continuous Output Current For TO-5



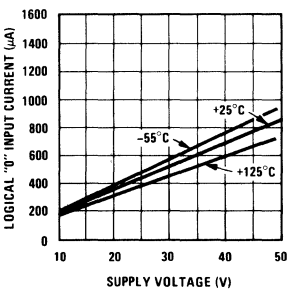
Maximum Continuous Output Current For Molded DIP



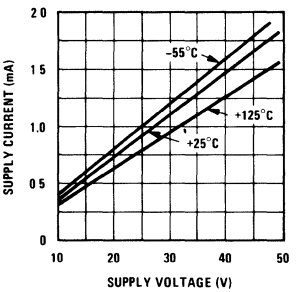
Input Threshold Voltage vs Temperature



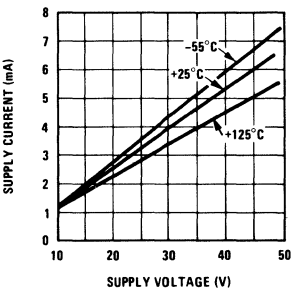
Logical "0" Input Current



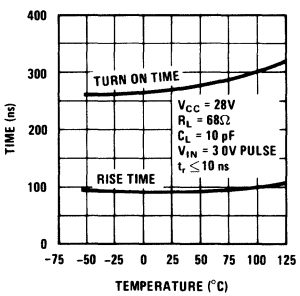
"OFF" Supply Current Drain



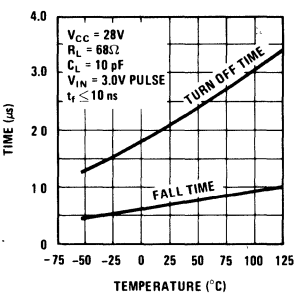
"ON" Supply Current Drain



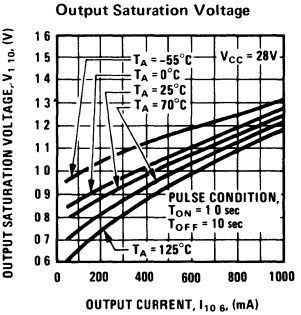
Turn On And Rise Time



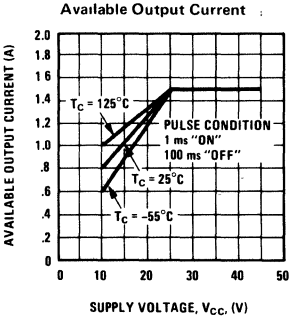
Turn Off and Fall Time



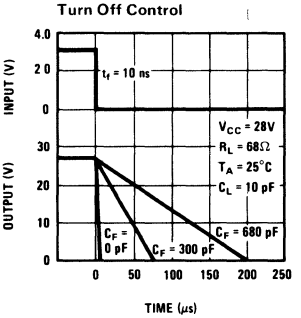
Output Saturation Voltage



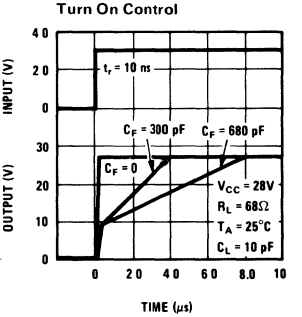
Available Output Current



Turn Off Control



Turn On Control



9

Interface Circuits

DH0008/DH0008C*
high voltage, high current driver

general description

The DH0008/DH0008C is an integrated high voltage, high current driver, designed to accept standard DTL or TTL input levels and provide a pulsed load of up to 3A from a continuous supply voltage up to 45V. AND inputs are provided with an EXPANDER connection, should additional gating be required.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

The high pulse current capability makes the DH0008/DH0008C ideal for driving nonlinear resistive loads such as incandescent lamps. The *Previously called NH0008/NH0008C

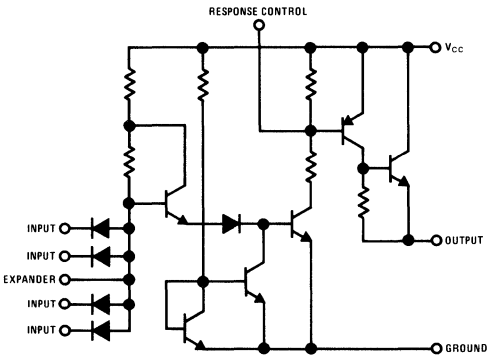
circuit also requires only one power supply for circuit functional operation.

The DH0008 is available in a 10-pin TO-5 package; the DH0008C is also available in a 10-pin TO-5, in addition to a 10-lead molded dual-in-line package.

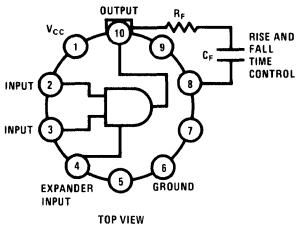
features

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 3.0A, 50 ms, Pulse Current Capability.

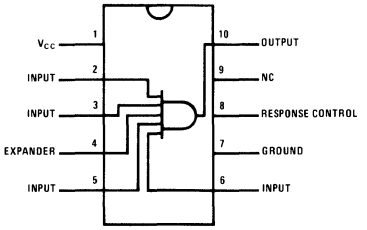
schematic and connection diagrams



Metal Can Package

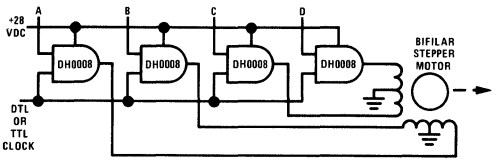


Dual-In-Line Package



typical application

Controller for Closed Loop Stepper Motor



Switching Sequence

Step	A	B	C	D
1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

To reverse the direction use a 4, 3, 2, 1 sequence

absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5 5V
Input Extender Current	5.0 mA
Peak Output Current	
(50 msec On/1 sec Off)	3 0 Amp
Continuous Output Current	
(See continuous operating curves.)	
Operating Temperature	
DH0008	−55°C to +125°C
DH0008C	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A 50 ms On/1 sec Off	43	43 5		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		0.02	0.1	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 0.8A 50 ms On/1 sec Off	26.5	27.1		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2 4V		0 5	5 0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0 V		1.6	2 0	mA
Rise Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.2		μs
Fall Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		3.0		μs
T_{ON}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5 0V		0.4		μs
T_{OFF}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		7.0		μs

Note 1: Unless otherwise specified limits shown apply from −55°C to 125°C for DH0008 and 0°C to 70°C for DH0008C.

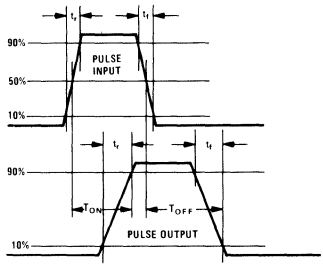
Note 2: Typical values are 25°C ambient

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ JA of 210°C/w

Note 4: Power ratings for the DH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 150°C/w when mounted in a standard DIP socket

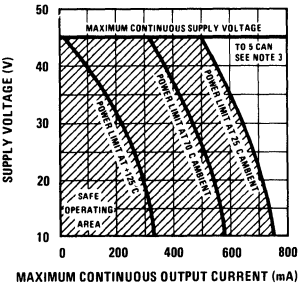
Note 5: Power ratings for the DH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 115°C/w when mounted on a 1/16 inch thick, epoxy-glass board with ten 0 03 inch wide 2 ounce copper conductors.

switching time waveforms

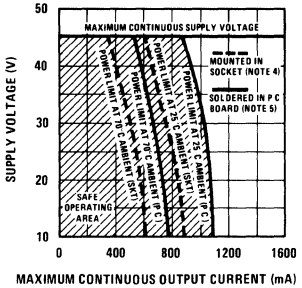


typical performance

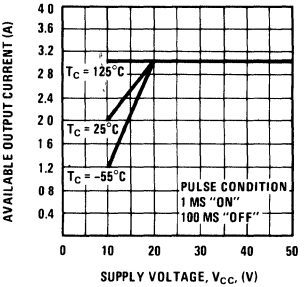
Maximum Continuous Output Current for TO-5 Package



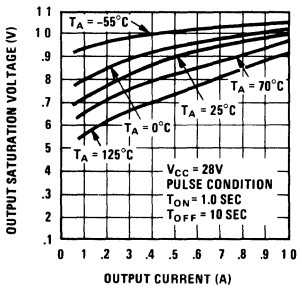
Maximum Continuous Output Current for Molded DIP



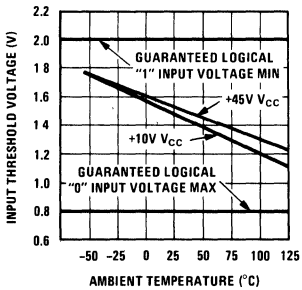
Available Output Current



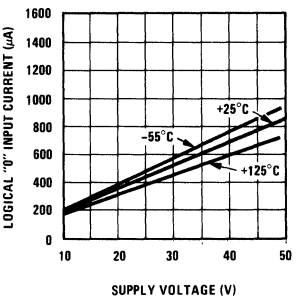
Output Saturation Voltage



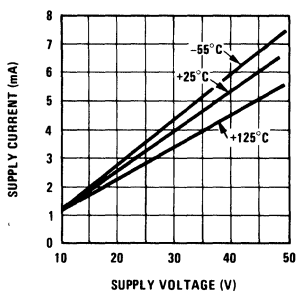
Input Threshold Voltage vs Temperature



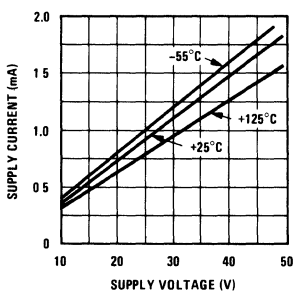
Logical "0" Input Current



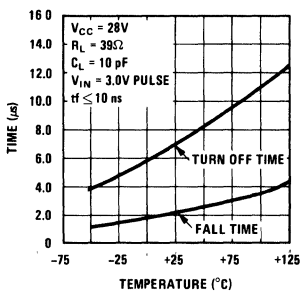
ON Supply Current Drain



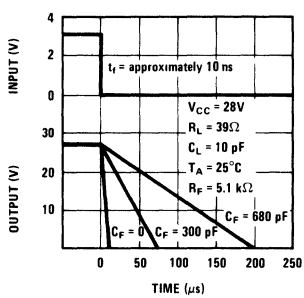
OFF Supply Current Drain



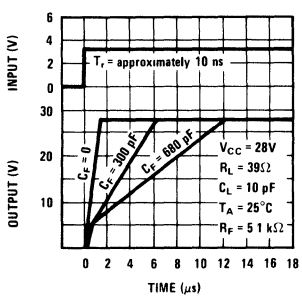
Turn OFF and Fall Times



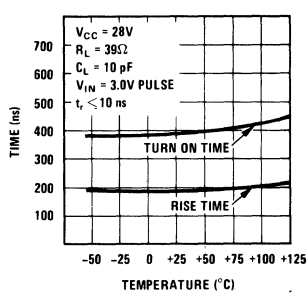
Turn ON Control



Turn OFF Control



Turn ON and Rise Time



Interface Circuits

DH0011*(SH2001)
DH0011C*(SH2002)
DH0011CN*(SH2002P)

high voltage high current drivers

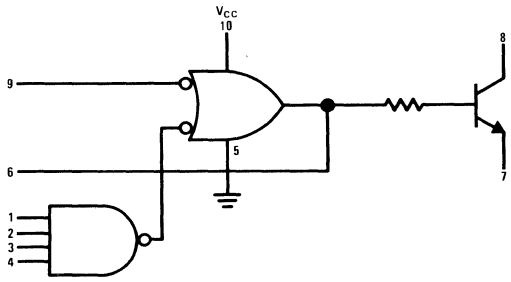
general description

The DH0011 high voltage, high current driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability. A summary of the variations is listed below.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 40V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects the base of the output transistor.

*Previously called NH0011, NH0011C, NH0011CN

logic diagram



ordering information

NSC DESIGNATION	SH DESIGNATION	PACKAGE	TEMPERATURE RANGE	OUTPUT CURRENT CAPABILITY
DH0011H	SH2001	TO 100	-55°C to +125°C	250 mA
DH0011CH	SH2002	TO 100	0°C to +70°C	150 mA
DH0011CN	SH2002 P	Epoxy "B" DIP	0°C to +70°C	150 mA

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absolute maximum ratings

V_{CC}		8V
Collector Voltage (Output)		40V
Input Reverse Current		1.0 mA
Power Dissipation		800 mW
Operating Temperature Range	DH0011	−55°C to +125°C
	DH0011C/DH0011CN	0°C to +70°C
Storage Temperature		−65°C to 150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12					GND				V_R	V_{CCH}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18					GND		GND			V_{CCL}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms on Page 4

forcing functions (Note 1) DH0011

PARAMETER	−55°C	+25°C	+125°C	UNITS
V_{CCL}	4.5	4.5	4.5	V
V_{CCH}	5.5	5.5	5.5	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.4	1.1	0.8	V
V_{IH}	2.1	1.9	1.7	V
V_R	4.0	4.0	4.0	V
V_F	0.0	0.0	0.0	V
I_{OL1}	250	250	250	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.0	40.0	40.0	V

Note 1: Temperature Range −55°C to +125°C

forcing functions (Note 2) DH0011C, DH0011CN

PARAMETER	0°C	+25°C	+70°C	UNITS
V_{CCL}	5.00	5.0	5.0	V
V_{CCH}	5.00	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.20	1.1	.95	V
V_{IH}	2.00	1.9	1.8	V
V_R	4.00	4.0	4.0	V
V_F	0.45	0.45	0.5	V
I_{OL1}	150	150	150	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.00	40.0	40.0	V

test limits (Note 1) DH0011

PARAMETER	-55°C		+25°C		+125°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.4		0.45	V
V_{OL2}		0.45		0.4		0.45	V
V_{OH}	2.20		2.00		1.80		V
I_R				2.0		5.0	μA
$-I_F$		1.60		1.6		1.5	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				29.6			mA
t_{ON}				160			ns
t_{OFF}				220			ns

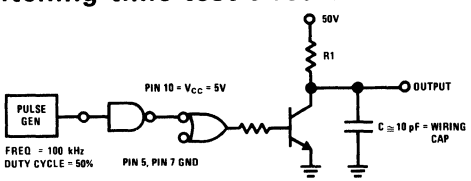
test limits (Note 2) DH0011C, DH0011CN

PARAMETER	0°C		+25°C		+70°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.45		0.5	V
V_{OL2}		0.45		0.45		0.5	V
V_{OH}	2.05		1.95		1.85		V
I_R				5.0		10.0	μA
$-I_F$		1.40		1.4		1.35	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				34.0			mA

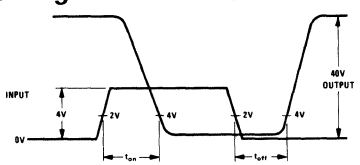
Note 1: Temperature Range -55°C to +125°C

Note 2: Temperature Range 0°C to +70°C

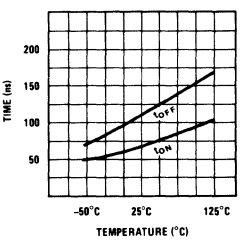
switching time test circuit



switching time waveforms



Typical Switching Times



9

Interface Circuits

DH0016CN*
DH0017CN*(SH2200P)
DH0018CN*

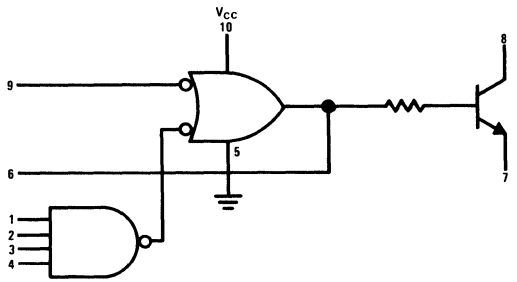
high voltage high current drivers

general description

This high-voltage, high-current driver family consists of hybrid integrated circuits which provide a wide range of output currents and output voltages. Applications include driving lamps, relays, cores, and other devices requiring up to 500 mA and withstanding voltages up to 100V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

*Previously called NH0016CN, NH0017CN, NH0018CN

logic diagram



ordering information

NSC DESIGNATION	SH DESIGNATION	PACKAGE	OUTPUT CHARACTERISTICS	
			Maximum Standoff Voltage	Current
DH0016CN	N/A	Epoxy "B" DIP	70V	250 mA
DH0017CN	SH2200P	Epoxy "B" DIP	50V	500 mA
DH0018CN	N/A	Epoxy "B" DIP	100V	500 mA

absolute maximum ratings

V_{CC}		8V
Input Voltage		8V
Collector Voltage	DH0016CN	70V
	DH0017CN	50V
	DH0018CN	100V
Output Surge Current	DH0016CN	1.0A
	DH0017CN & DH0018CN	2.0A
Power Dissipation		455mW
Operating Temperature Range		0°C to +70°C
Storage Temperature		−65°C to +150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMITS MIN	LIMITS MAX
2	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16					GND				V_R	V_{CC}	I_9		I_R
17	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22					GND		GND			V_{CC}	V_6	V_{OH1}	
23	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24					GND					V_{PD}	I_{10}		I_{PD}
25	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}

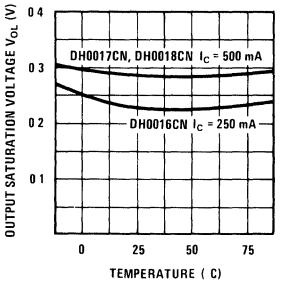
forcing functions

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{CC}	5.0	5.0	5 0	V
V_{PD}		5 0		V
V_{MAX}		8 0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4 5	4.5	4.5	V
V_F	0.45	0.45	0 45	V
V_{OX} (DH0016CN)		70	70	V
V_{OX} (DH0017CN)		50	50	V
V_{OX} (DH0018CN)		100	100	V
I_{OL1} (DH0017CN, DH0018CN)	500	500	500	mA
I_{OL1} (DH0016CN)	250	250	250	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

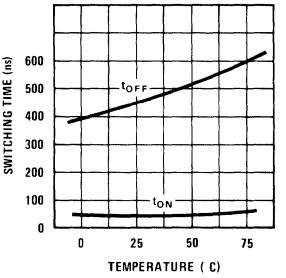
test limits

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{OL1}	0.6	0.6	0.6	V
V_{OL2}	0.45	0.45	0.45	V
V_{OHI}	1.95	1 85	1.65	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		10		mA

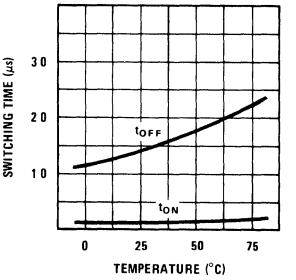
Typical Output Voltages vs Temperature



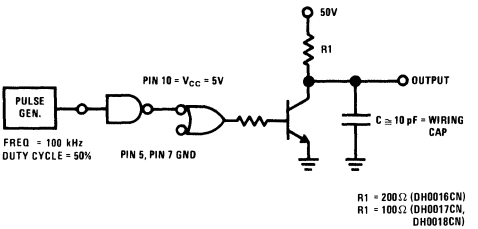
Typical Switching Times I_C = 250 mA
DH0016CN



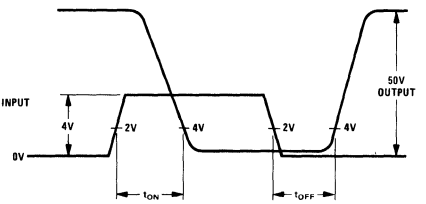
Typical Switching Times I_C = 500 mA
DH0017CN, DH0018CN



switching time test circuit



switching time waveforms



Interface Circuits

DH0028C/DH0028CN*hammer driver

general description

The DH0028C/DH0028CN is a high current hammer driver designed for utilization in a wide variety of printer applications. The device is capable of driving 6 amp pulsed loads at duty cycles up to 10% (1 ms ON/10 ms OFF). The input is DTL/TTL compatible and requires only a single voltage supply in the range of 10V to 45V.

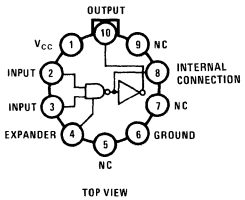
features

- Low standby power 45 mW at V_{CC} = 36V, 35 mW at V_{CC} = 28V.
- AND input with expander affords logic flexibility.
- Fast turn-on, typically 200 ns.

*Previously called NH0028C/NH0028CN

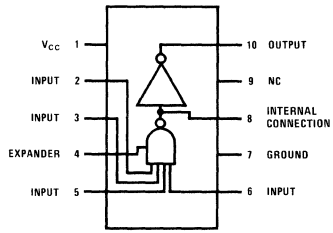
connection diagrams

Metal Can Package

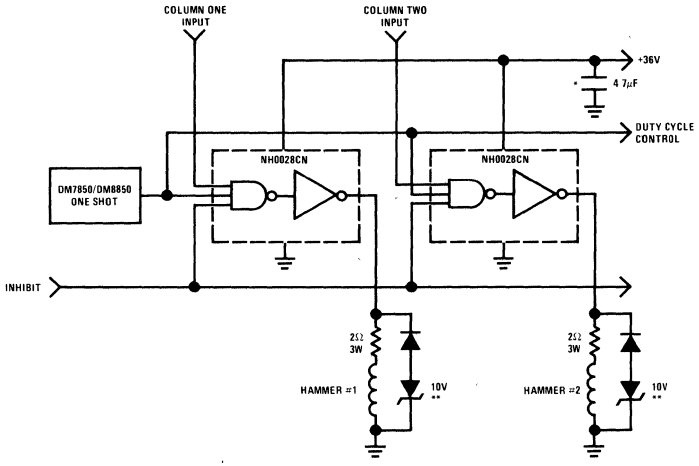


TOP VIEW

Molded Dual-In-Line Package



typical application



*Use one decoupling capacitor per six hammer drivers for improved AC noise immunity

**Zener is used to control the dynamics of the hammer

absolute maximum ratings

Continuous Supply Voltage	45V
Instantaneous Peak Supply Voltage (Pin 1 to Ground for 0.1 sec)	60V
Input Voltage	5.5V
Expander Input Current	5.0 mA
Peak Otuput Current (1 ms ON/10 ms OFF)	6.5A
Continuous Output Current DH0028C at 25°C	750 mA
DH0028CN at 25°C	1000 mA
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +175°C
Lead Soldering Temperature (10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 10V to 45V	2 0			V
Logical "0" Input Voltage	V_{CC} = 10V to 45V			0 8	V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0 4V		0 8	1 0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2 4V		0 5	5 0	μA
	V_{CC} = 45V, V_{IN} = 5 5V			100 0	μA
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2 0V, I_{OUT} = 1 6A	43 0	43 5		V
	V_{CC} = 36V, V_{IN} = 2 0V, I_{OUT} = 5A (Note 2)	33 5	34 0		V
Logical "0" Output Voltage	V_{CC} = 45V, R_L = 1k, V_{IN} = 0 8V		020	100	V
OFF Power Supply Current	V_{CC} = 45V, V_{IN} = 0 0V		1 6	2 0	mA
Rise Time (10% to 90%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		0 2		μs
Fall Time (90% to 10%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		3 0		μs
T_{ON}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		0 4		μs
T_{OFF}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		7 0		μs

Note 1 These specifications apply for ambient temperatures from 0°C to 70°C unless otherwise specified All typical values are for 25°C ambient

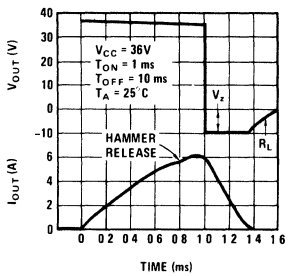
Note 2 Measurement made at 1 ms ON and 10 ms OFF

Note 3 Power ratings for the DH0028C are based on a maximum junction temperature of 175°C and a thermal resistance of 210°C/W

Note 4 Power ratings for the DH0028CN are based on a maximum junction temperature of 175°C and a thermal resistance of 150°C/W

typical performance characteristics

Waveforms for Typical Drum Printer Hammer



Interface Circuits

DH0034/DH0034C high speed dual level translator

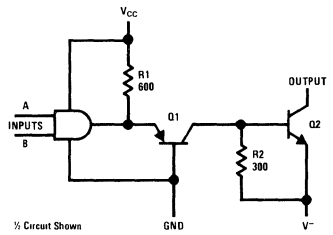
general description

The DH0034/DH0034C is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

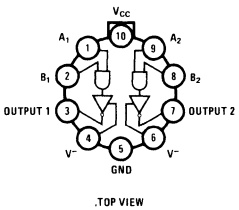
features

- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA
- High output currents: up to ±100 mA

schematic and connection diagrams

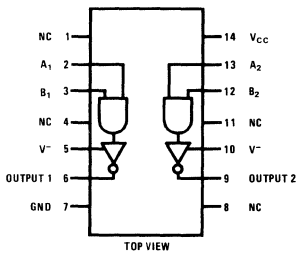


Metal Can Package



TOP VIEW

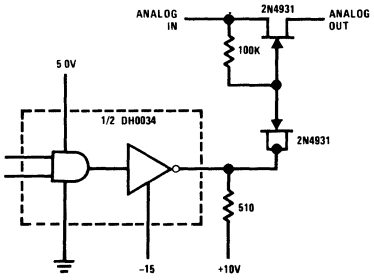
Dual-in-Line Package



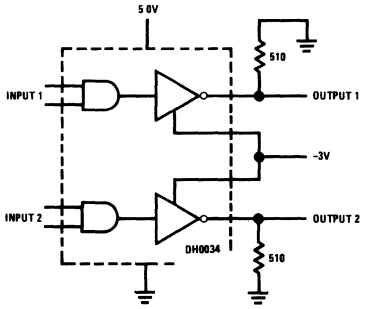
TOP VIEW

typical applications

5 MHz Analog Switch



TTL to IBM (SLT) Logic Levels



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absolute maximum ratings

V_{CC} Supply Voltage		7.0V
Negative Supply Voltage		-30V
Positive Supply Voltage		+25V
Differential Supply Voltage		25V
Maximum Output Current		100 mA
Input Voltage		+5.5V
Operating Temperature Range:	DH0034	-55°C to +125°C
	DH0034C	0°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (See Notes 1 & 2)

PARAMETER	CONDITIONS	DH0034			DH0034C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Logical "1" Input Voltage	V_{CC} = 4.5V V_{CC} = 4 75V	2.0			2.0			V
Logical "0" Input Voltage	V_{CC} = 5.5V V_{CC} = 4.75V			0.8			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V V_{CC} = 5.25V, V_{IN} = 2.4V			40			40	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V V_{CC} = 5.25V, V_{IN} = 5.5V			1 0			1 0	mA
Logical "0" Input Current	V_{CC} = 5 5V, V_{IN} = 0.4V V_{CC} = 5.25V, V_{IN} = 0 4V			1.6			1.6	mA
Power Supply Current Logic "0"	(Note 3) V_{CC} = 5.5V, V_{IN} = 4 5V V_{CC} = 5.25V, V_{IN} = 4.5V		30	38		30	38	mA
Power Supply Current Logic "1"	(Note 3) V_{CC} = 5.5V, V_{IN} = 0V V_{CC} = 5 25V, V_{IN} = 0V		37	48		37	48	mA
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 100 mA V_{CC} = 4.5V, I_{OUT} = 50 mA		V^- + .50 V^- + .3	V^- + .75 V^- + .50		V^- + .50 V^- + .3	V^- + .80 V^- + .65	V V
Output Leakage Current	V_{CC} = 5.5V, V_{IN} = 0.8V $V^+ \cdot V^-$ = 25V		0 1	5		0.1	5	μA
Transition Time to Logical "0"	V_{CC} = 5.0V, V_3 = 0V, T_A = 25°C V^- = -25V, R_L = 510Ω		15	25		15	35	ns
Transition Time to Logical "1"	V_{CC} = 5 0V, T_A = 25°C V^- = -25V, R_L = 510Ω		35	60		35	65	ns

Note 1: These specifications apply over the temperature range -55°C to +125°C for the DH0034 and 0°C to +85°C for the DH0034C with a 510 ohm resistor connected between output and ground, and V^- connected to -25V, unless otherwise specified.

Note 2: All typical values are for T_A = 25°C.

Note 3: Current measured is total drawn from V_{CC} supply.

theory of operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by $\frac{V_{CC} - V_{BE}}{R1}$ Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0," the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

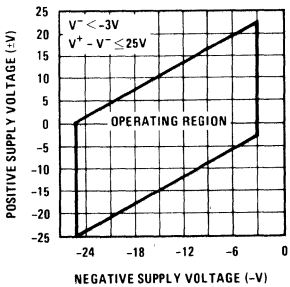
applications information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2 ohms/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. The range of operation for the negative supply is shown on the X axis and must be between −3V and −25V. The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to −6V would dictate values of



V^+ between −5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.

9

Interface Circuits

DH0035/DH0035C PIN diode switch driver

general description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

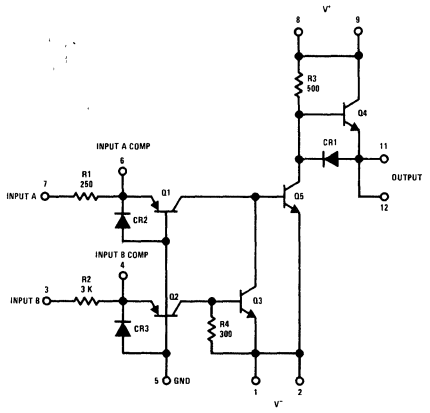
features

- Large output voltage swing – 30V
- Peak output current in excess of 1 Amp
- Inputs TTL/DTL compatible
- Short propogation delay – 10 ns
- High repetition rate – 5 MHz

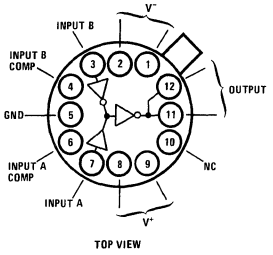
The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers*.

The DH0035 is guaranteed over the temperature range −55°C to +125°C whereas the DH0035C is guaranteed from 0°C to 85°C.

schematic and connection diagrams



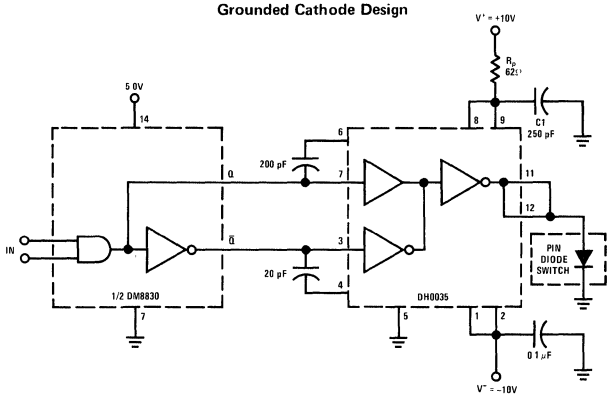
Metal Can Package



TOP VIEW

typical applications

Grounded Cathode Design



Note Cathode grounded PIN diode R_P = 62Ω limits diode forward current to 100 mA Typical switching for HP33604A RF turn on 25 ns, turn off 5 ns C2 = 250 pF, R_P = 062, C1 = 0 1F

absolute maximum ratings

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V	Storage Temperature Range	−65°C to +150°C
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V	Operating Temperature Range DH0035	−55°C to +125°C
Input Current (Pin 3 or 7)	±75 mA	DH0035C	0°C to +85°C
Peak Output Current	±1 0 Amps	Lead Temperature (Soldering, 10 sec)	300°C
Power Dissipation (Note 3)	1 5W		

electrical characteristics (Notes 1, 2)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Logic "1" Threshold	V_{OUT} = −8V, R_L = 100Ω	1 5			V
Input Logic "0" Threshold	V_{OUT} = +8V, R_L = 100Ω			0 4	V
Positive Output Swing	I_{OUT} = 100 mA	7 0	+8 0		V
Negative Output Swing	I_{OUT} = 100 mA		−8 0	−7 0	V
Positive Short Circuit Current	V_{IN} = 0V, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	400	800		mA
Negative Short Circuit Current	V_{IN} = 1 5V, I_{IN} = 50 mA, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	800	−1000		mA
Turn-On Delay	V_{IN} = 1 5V, V_{OUT} = −3V		10	15	ns
Turn-Off Delay	V_{IN} = 1 5V, V_{OUT} = +3V		15	30	ns
On Supply Current	V_{IN} = 1 5V		45	60	mA

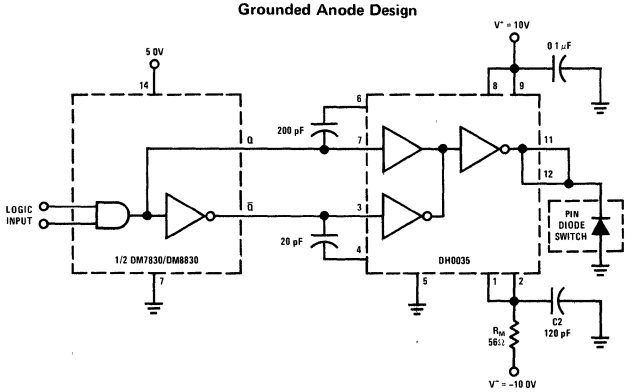
Note 1: Unless otherwise specified, these specifications apply for V^+ = 10.0V, V^- = −10.0V, pin 5 grounded, over the temperature range −55°C to +125°C for the DH0035, and 0°C to 85°C for the DH0035C.

Note 2: All typical values are for T_A = 25°C

Note 3: Derate linearly at 10 mW/°C for ambient temperatures above 25°C

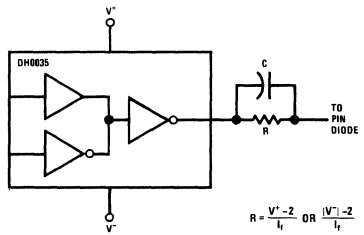
typical applications (cont.)

Grounded Anode Design



Note: Anode Grounded PIN diode, R_M = 56Ω limits diode forward current to 100 mA. Typical switching for HP33622A, RF turn on 5 ns, turn off 4 ns. C1 = 470 pF, C2 = 0 1 µF, R_M = 0Ω.

Alternate Current Limiting



9

Interface Circuits

DH3467C quad PNP core driver

general description

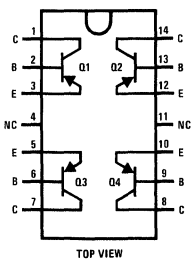
The DH3467C consists of four 2N3467 type PNP transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0 55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

connection diagram

Dual-In-Line Package



TOP VIEW

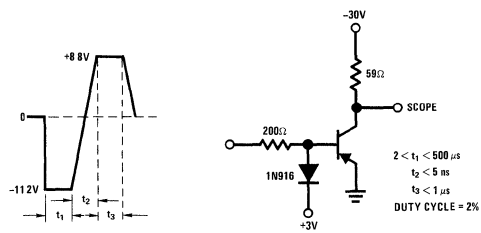


FIGURE 1. Turn-On Equivalent Test Circuit

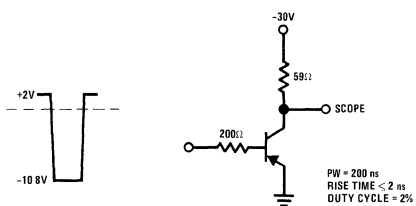


FIGURE 2. Turn-Off Equivalent Test Circuit

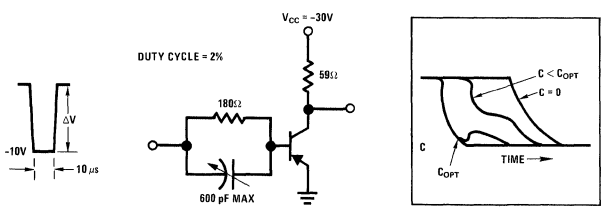


FIGURE 3. Q_T Test Circuit

absolute maximum ratings

Collector to Base Voltage	40V
Collector to Emitter Voltage	40V
Collector to Emitter Voltage (Note 1)	40V
Emitter to Base Voltage	5V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C) (each device)	0.85W
Power Dissipation (T_A = 25°C) (total package)	2.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA I_E = 0	−40		V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_E = 10 μA I_C = 0	−5 0		V
Collector to Emitter Breakdown Voltage (Note 1) (BV_{CEO})	I_C = 10 mA I_B = 0	−40		V
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 150 mA V_{CE} = −1 0V	40		
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 500 mA V_{CE} = −1 0V	40	120	
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 1 0A V_{CE} = −5 0V	40		
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 150 mA I_B = 15 mA		−0 30	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 500 mA I_B = 50 mA		−0.50	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 1.0A I_B = 100 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 150 mA I_B = 15 mA		−1 0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 500 mA I_B = 50 mA	−0 8	−1 2	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 1.0A I_B = 100 mA		−1 6	V
Collector Cutoff Current (I_{CBO})	V_{CB} = −30V I_B = 0		100	nA
Collector Cutoff Current ($I_{CBO(100°C)}$)	V_{CB} = −30V I_B = 0		15	μA
Collector Cutoff Current (I_{CEX})	V_{CB} = −30V V_{EB} = −3 0V		100	nA
Base Cutoff Current (I_{BL})	V_{CB} = −30V V_{EB} = −3 0V		120	nA
Total Control Charge (Figure 3) (Q_T)	I_C = 500 mA I_B = 50 mA		6 0	nC
Turn On Delay Time (Figure 1) (t_d)	I_C = 500 mA I_{B1} = 50 mA		10	ns
Rise Time (Figure 1) (t_r)	I_C = 500 mA I_{B1} = 50 mA		30	ns
Storage Time (Figure 2) (t_s)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		60	ns
Fall Time (Figure 2) (t_f)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		30	ns
Output Capacitance (f = 100 kHz) (C_{ob})	I_E = 0 V_{CB} = −10V		25	pF
Input Capacitance (f = 100 kHz) (C_{ib})	I_C = 0 V_{CB} = −0 5V		100	pF
High Frequency Current Gain (f = 100 MHz) (h_{fe})	I_C = 50 mA V_{CE} = 10V	1 75		

Note 1: Pulsed test, PW = 300μs, duty cycle = 1%

Interface Circuits

DH3725C quad NPN core driver

general description

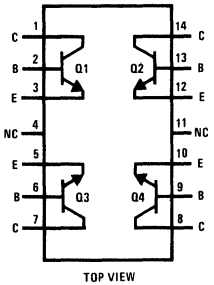
The DH3725C consists of four 2N3725 type NPN transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0.55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

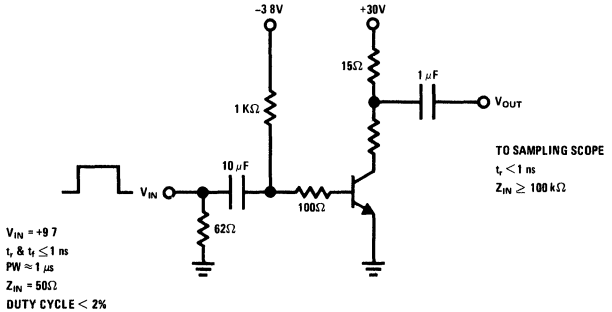
connection diagram

Dual-In-Line Package



TOP VIEW

switching time test circuit



$I_C \approx 500$ mA, $I_{B1} \approx 50$ mA, $I_{B2} \approx -50$ mA

absolute maximum ratings

Collector to Base Voltage	80V
Collector to Emitter Voltage	80V
Collector to Emitter Voltage (Note 1)	50V
Emitter to Base Voltage	6V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C)	0.6W
Power Dissipation (T_C = 25°C)	1.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics – Each transistor (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector to Emitter Sustaining Voltage (V_{CEO} (sust)	I_C = 10 mA, I_B = 0	50			V
Collector to Emitter Breakdown Voltage (BV_{CES})	I_C = 10 μA, V_{BE} = 0	80			V
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA, I_E = 0	80			V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_C = 0, I_E = 10 μA	6.0			V
Collector Saturation Voltage ($V_{CE\ (Sat)}$) (Note 2)	I_C = 1A, I_B = 100 mA		0 55	0.95	V
	I_C = 0.5A, I_B = 50 mA		0.31	0.52	V
	I_C = 0.1A, I_B = 10 mA		0.19	0.26	V
DC Pulse Current Gain (h_{FE}) (Note 2)	I_C = 1A, V_{CE} = 5V	25	65		
	I_C = 0.5A, V_{CE} = 1V	35	45		
	I_C = 0.1A, V_{CE} = 1V	60	90	150	
Base Saturation Voltage (V_{BE} (Sat) (Note 2)	I_C = 1A, I_B = 100 mA		1 10	1.70	V
	I_C = 0.5A, I_B = 50 mA		0.95	1.20	V
	I_C = 0.1A, I_B = 10 mA		0.75	0.86	V
Collector Cutoff Current (I_{CBO})	I_E = 0, V_{CB} = 60V		0.33	1.70	μA
Turn-ON Time	I_C = 0.5A, I_{B1} = 50 mA (See test circuit)		18	30	ns
Turn-OFF Time	I_C = 0.5A, I_{B1} = 50 mA I_{B2} = 50 mA (See test circuit)		45	60	ns
High Frequency Current Gain	f = 100 MHz, I_C = 50 mA, V_{CE} = 10V	2.5	4.5		
Common Base, Open Circuit, Output Capacitance	I_E = 0, V_{CB} = 10V		4.8	10	pF
Common Base, Open Circuit, Input Capacitance	I_C = 0, V_{BE} = 0.5V		40	55	pF

Note 1: Ratings refer to a high-current point where collector-to-emitter voltage is lowest

Note 2: Pulse conditions Length = 300 μs, duty cycle = 1%.

Interface Circuits

LH2111/LH2211/LH2311 dual voltage comparator

general description

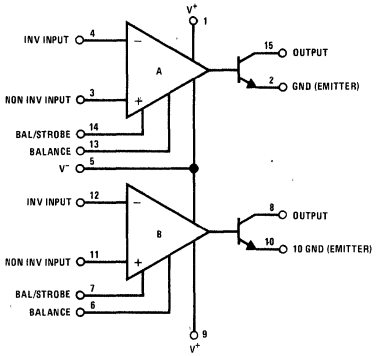
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook

The LH2111 is specified for operation over the -55°C to +125°C military temperature range. The LH2211 is specified for operation over the -25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

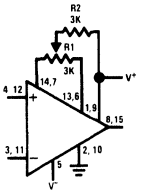
features

- Wide operating supply range — ±15V to a single +5V
- Low input currents — 6 nA
- High sensitivity — 10 μV
- Wide differential input range — ±30V
- High output drive — 50 mA, 50V

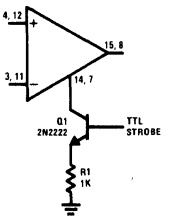
connection diagram



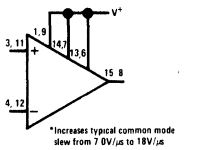
auxiliary circuits



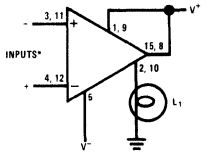
Offset Balancing



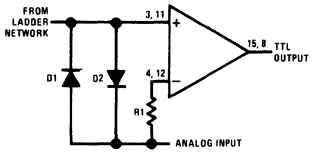
Strobing



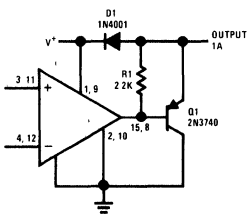
Increasing Input Stage Current*



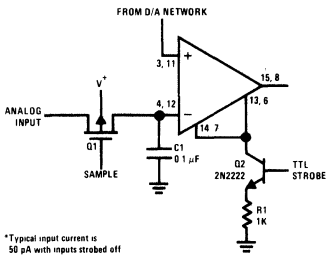
Driving Ground-Referred Load



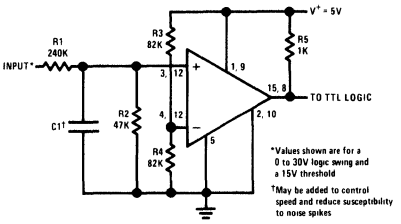
Using Clamp Diodes to Improve Responses



Comparator and Solenoid Driver



Strobing off Both Input* and Output Stages



TTL Interface with High Level Logic

absolute maximum ratings

Total Supply Voltage ($V^+ - V^-$)		36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)		50V
Ground to Negative Supply Voltage (GND – V^-)		30V
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Power Dissipation (Note 2)		500 mW
Output Short Circuit Duration		10 sec
Operating Temperature Range	LH2111	–55°C to 125°C
	LH2211	–25°C to 85°C
	LH2311	0°C to 70°C
Storage Temperature Range		–65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics – each side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3 0	3 0	7 5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$	1 5	1 5	1 5	V Max
Strobe On Current	$T_A = 25°C$	3 0	3 0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	4 0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4$ 5V, $V^- = 0$ $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6 0	6 0	7 5	mA Max
Negative Supply Current	$T_A = 25°C$	5 0	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, $-25°C \leq T_A \leq 85°C$ for the LH2211, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive

Interface Circuits

LM106/LM206 voltage comparator/buffer

general description

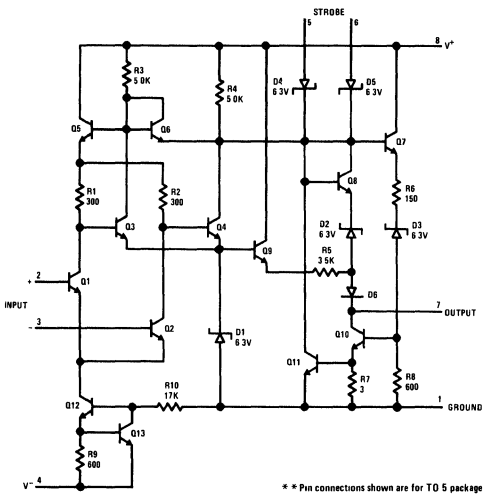
The LM106 and LM206 are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 100 mA. Other features include:

- Improved accuracy: 2 mV maximum worst case offset.
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710.
- 40 ns maximum response time

The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 and LM206. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

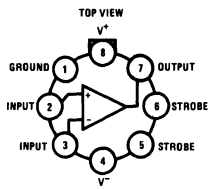
The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM206 is specified for operation over the −25°C to +85°C temperature range.

schematic and connection diagrams * *



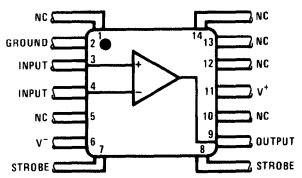
* * Pin connections shown are for TO 5 package

Metal Can



Note: Pin 4 connected to case

Flat Package

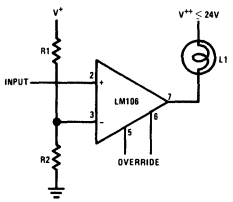


Note: Pin 6 connected to bottom of package

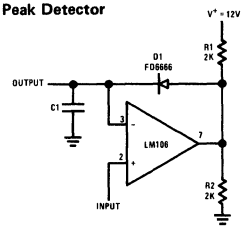
TOP VIEW

typical applications * *

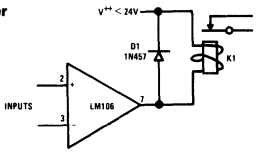
Level Detector and Lamp Driver



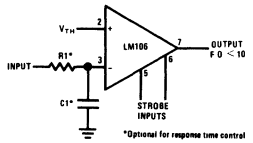
Fast Response Peak Detector



Relay Driver



Adjustable Threshold Line Receiver



*Optional for response time control

absolute maximum ratings

Positive Supply Voltage	15V	Power Dissipation (Note 1)	600 mW
Negative Supply Voltage	−15V	Output Short Circuit Duration	10 sec
Output Voltage	24V	Operating Temperature Range LM106	−55°C to 125°C
Output to Negative Supply Voltage	30V	LM206	−25°C to 85°C
Differential Input Voltage	±5V	Storage Temperature Range	−65°C to 150°C
Input Voltage	±7V	Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3		0.5	2 0	mV
Input Offset Current	Note 3		0 7	3.0	μA
Input Bias Current			10	20	μA
Response Time	Note 4, R_L = 390Ω to +5V, C_L = 15 pF		28	40	ns
Saturation Voltage	$V_{IN} \leq$ -5 mV, I_{OUT} = 100 mA		1 0	1 5	V
Output Leakage Current	$V_{IN} \geq$ 5 mV, 8V $\leq V_{OUT} \leq$ 24V		0 02	1 0	μA

electrical characteristics

The following specifications apply for $T_L \leq T_A \leq T_H$ (Note 5)

Input Offset Voltage	Note 3			3 0	mV
Average Temperature Coefficient of Input Offset Voltage			3 0	10	μV/°C
Input Offset Current	Note 3, $T_L \leq T_A \leq 25°C$		1 8	7 0	μA
	$25°C \leq T_A \leq T_H$		0 25	3 0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_H$		5 0	25	nA/°C
	$T_L \leq T_A \leq 25°C$		15	75	nA/°C
Input Bias Current	$T_L \leq T_A \leq 25°C$			45	μA
	$25°C \leq T_A \leq T_H$			20	μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5 0			V
Differential Input Voltage Range		±5 0			V
Saturation Voltage	$V_{IN} \leq$ -5 mV, I_{OUT} = 50 mA			1 0	V
Saturation Voltage	$V_{IN} \leq$ -5 mV, I_{OUT} = 16 mA			0 4	V
Positive Output Level	$V_{IN} \geq$ 5 mV, I_{OUT} = -400 μA	2 5		5 5	V
Output Leakage Current	$V_{IN} \geq$ 5 mV, 8V $\leq V_{OUT} \leq$ 24V, $T_L \leq T_A \leq 25°C$			1 0	μA
	$25°C < T_A \leq T_H$			100	μA
Strobe Current	V_{strobe} = 0 4V		-1 7	-3 2	mA
Strobe ON Voltage		0 9	1 4		V
Strobe OFF Voltage	$I_{sink} \leq$ 16 mA		1 4	2 2	V
Positive Supply Current	V_{IN} = -5 mV		5 5	10	mA
Negative Supply Current			-1 5	-3 6	mA

Note 1. The maximum junction temperature of the LM106 is 150°C, while that of the LM206 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0 03-inch-wide, 2-ounce copper conductors.

Note 2. These specifications apply for −3V > V^- > −12V, V^+ = 12V and T_A = 25°C unless otherwise specified. All currents into device pins are considered positive.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0 5V or up to 5 0V. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

Note 4. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 5: All currents into device pins are considered positive.

Interface Circuits

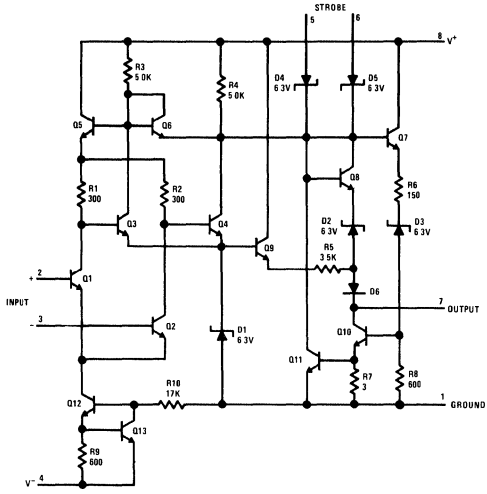
LM306 voltage comparator/buffer general description

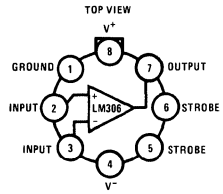
The LM306 is a high-speed voltage comparator designed to accurately detect low-level analog signals and drive a digital load. It is equivalent to an LM710C, combined with a two input NAND gate and an output buffer. The circuit can drive RTL, DTL or TTL integrated circuits directly. Furthermore, the output can switch voltages up to 24V at currents as high as 100 mA. Other features include.

- Improved accuracy. 5 mV (max) offset, 25,000 gain
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710C.

The device has short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts. The speed is equivalent to that of an LM710C. However, it is even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM306. It can also be operated from any negative supply voltage between −3V and −12V with little effect on performance. The LM306 is identical to the LM106, except that it is specified over a 0°C to 70°C temperature range.

schematic and connection diagrams

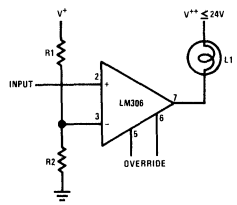




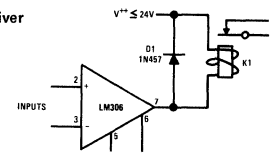
Note Pin 4 connected to case

typical applications

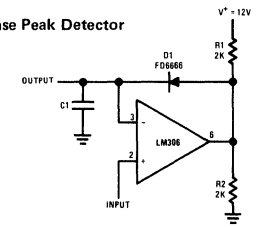
Level Detector and Lamp Driver



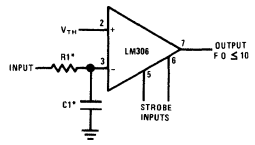
Relay Driver



Fast Response Peak Detector



Adjustable Threshold Line Receiver



*Optional for response time control

absolute maximum ratings

Positive Supply Voltage	15V
Negative Supply Voltage	−15V
Output Voltage	24V
Output to Negative Supply Voltage	30V
Differential Input Voltage	±5V
Input Voltage	±7V
Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3		1.6	5.0	mV
Input Offset Current	Note 3		1.8	5 0	μA
Input Bias Current			16	25	μA
Voltage Gain			40		V/mV
Response Time	Note 4		40		ns
Saturation Voltage	$V_{IN} \leq -7$ mV, I_{sink} = 100 mA		0.8	2.0	V
Output Leakage Current	$V_{IN} \geq 7$ mV, $8V \leq V_{OUT} \leq 24V$		0.02	2.0	μA

electrical characteristics

The following specifications apply for $0°C \leq T_A \leq 70°C$

Input Offset Voltage	Note 3			6.5	mV
Average Temperature Coefficient of Input Offset Voltage			5	20	μV/°C
Input Offset Current	Note 3, $T_A = 0°C$		2.4	7.5	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current			25	40	μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			V
Differential Input Voltage Range		±5.0			V
Saturation Voltage	$V_{IN} \leq -8$ mV, I_{sink} = 50 mA			1.0	V
Saturation Voltage	$V_{IN} \leq -8$ mV, $I_{sink} \leq 16$ mA			0.4	V
Positive Output Level	$V_{IN} \geq 8$ mV, I_{OUT} = 400 μA	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 8$ mV, $8V \leq V_{OUT} \leq 24V$			100	μA
Strobe Current	V_{strobe} = 0.4V		1.7	3.3	mA
Strobe ON Voltage		0.9	1.4		V
Strobe OFF Voltage	$I_{sink} \leq 16$ mA		1.4	2.5	V
Positive Supply Current	V_{IN} = −8 mV		5.5	10	mA
Negative Supply Current			1.5	3.6	mA

Note 1: For operating at elevated temperatures, the device must be derated based on a 85°C maximum junction temperature and a thermal resistance of 45°C/W junction to case or 150°C/W junction to ambient

Note 2. These specifications apply for $-3V \geq V^- \geq -12V$, V^+ = 12V and T_A = 25°C unless otherwise specified.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 5 0V. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Interface Circuits

LM111/LM211 voltage comparator

general description

The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

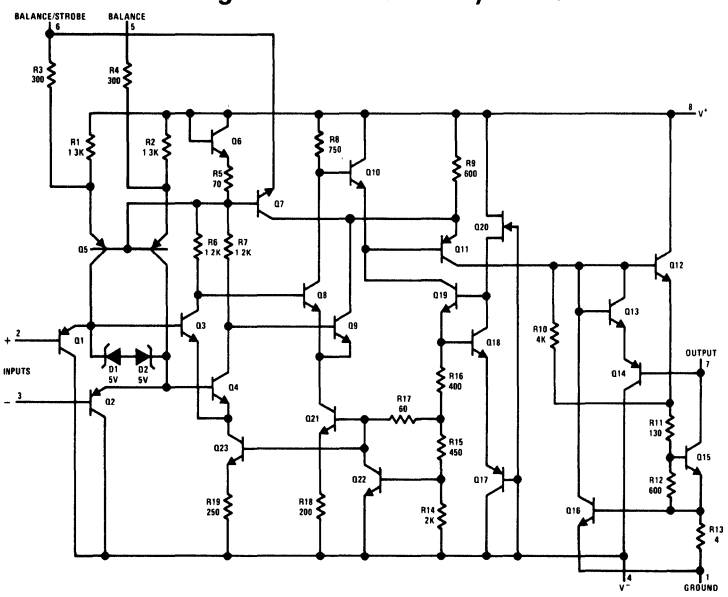
features

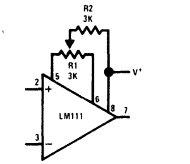
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

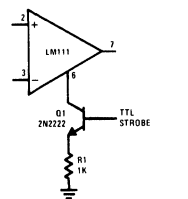
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

schematic diagram and auxiliary circuits

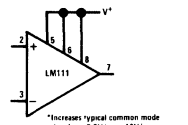




Offset Balancing



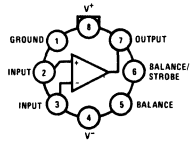
Strobing



Increasing Input Stage Current*

connection diagrams *

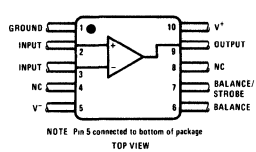
Metal Can



NOTE Pin 4 connected to case

TOP VIEW

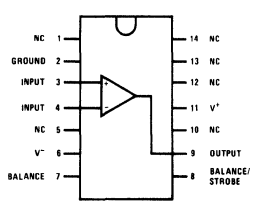
Flat Package



NOTE Pin 5 connected to bottom of package

TOP VIEW

Dual-In-Line Package



NOTE Pin 6 connected to bottom of package

TOP VIEW

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0 7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4 0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0 23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0 1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1. This rating applies for ±15V supplies The positive input voltage limit is 30V above the negative supply The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less

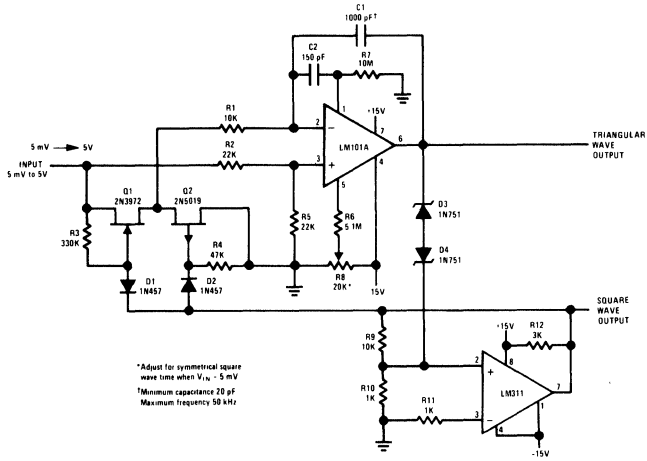
Note 2. The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0 03-inch-wide, 2-ounce copper conductors The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient

Note 3. These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise stated With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$ The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies

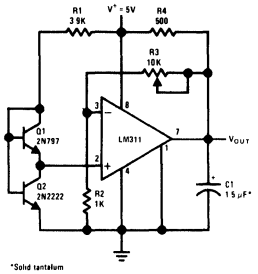
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive

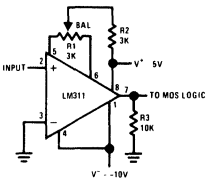
typical applications



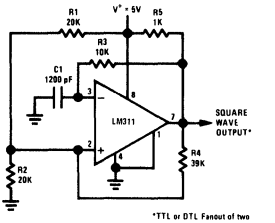
10 Hz to 10 kHz Voltage Controlled Oscillator



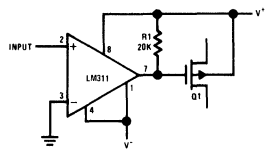
Low Voltage Adjustable Reference Supply



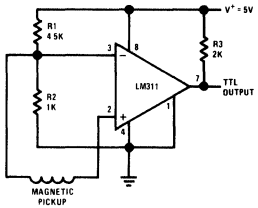
Zero Crossing Detector driving MOS logic



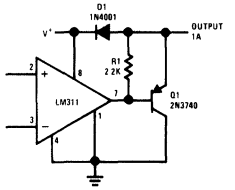
100 kHz Free Running Multivibrator



Zero Crossing Detector Driving MOS Switch

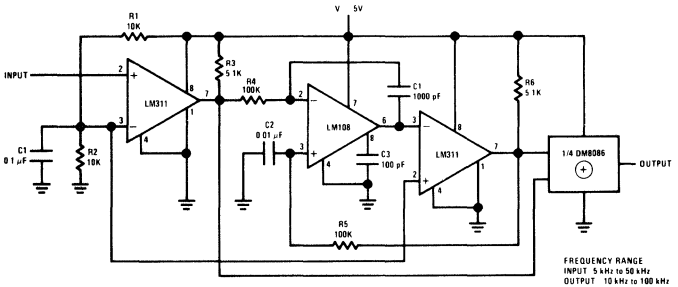


Detector for Magnetic Transducer

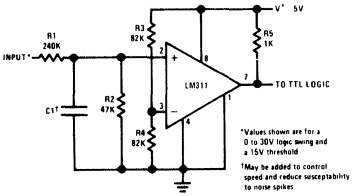


Comparator and Solenoid Driver

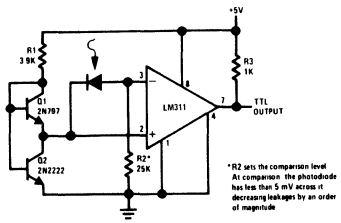
typical applications (con't)



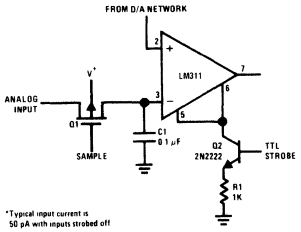
Frequency Doubler



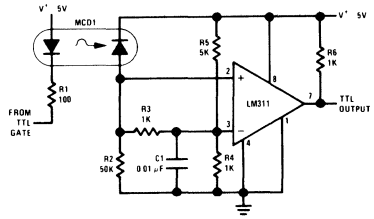
TTL Interface with High Level Logic



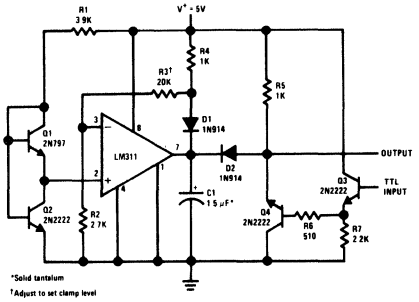
Precision Photodiode Comparator



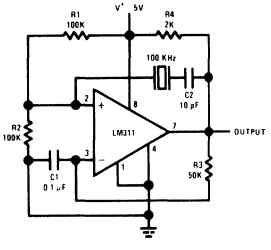
Strobing off Both Input* and Output Stages



Digital Transmission Isolator

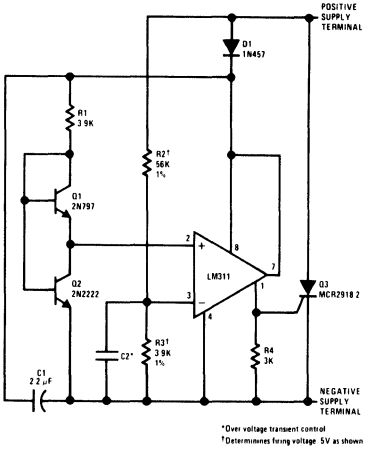


Precision Squarer

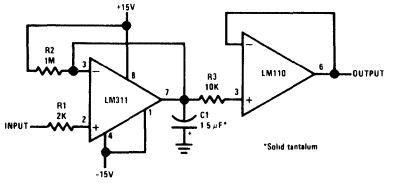


Crystal Oscillator

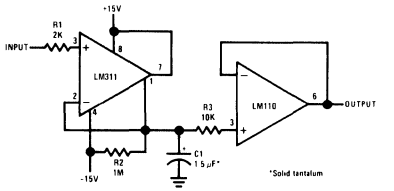
typical applications (con't)



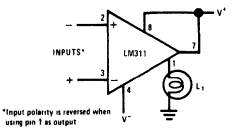
Crowbar Over-Voltage Protector



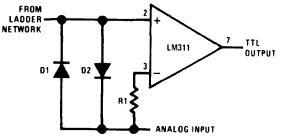
Negative Peak Dectector



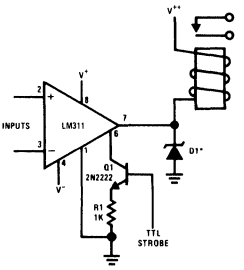
Positive Peak Detector



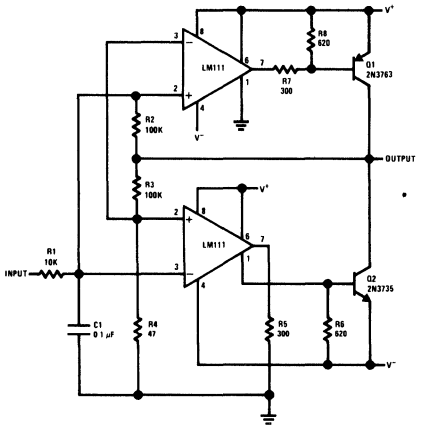
Driving Ground-Referred Load



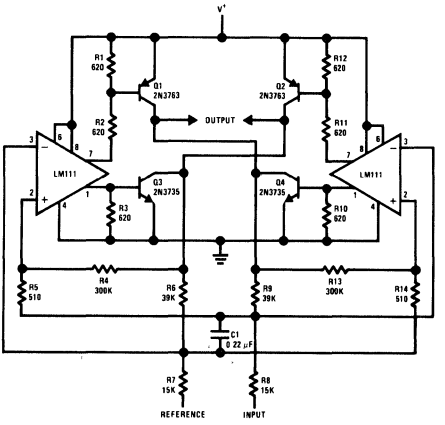
Using Clamp Diodes to Improve Response



Relay Driver with Strobe



Switching Power Amplifier



Switching Power Amplifier

Interface Circuits

LM311 voltage comparator

general description

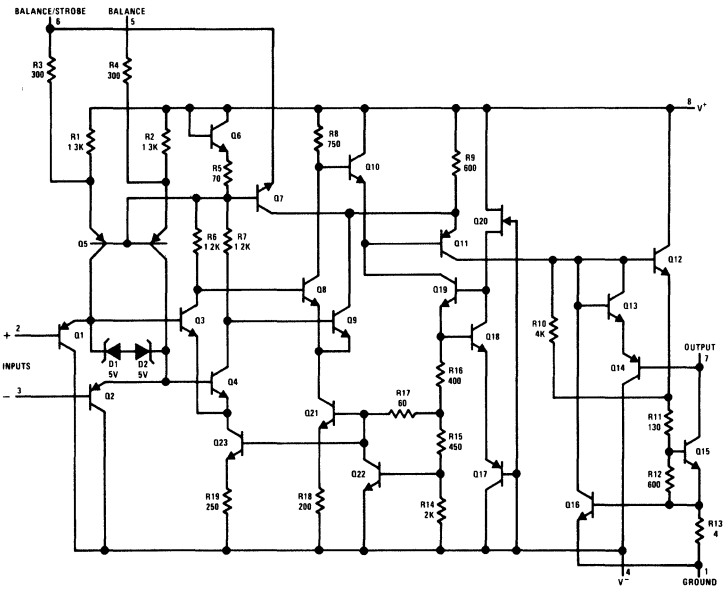
The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

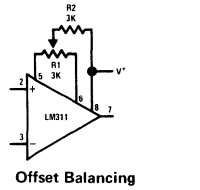
features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

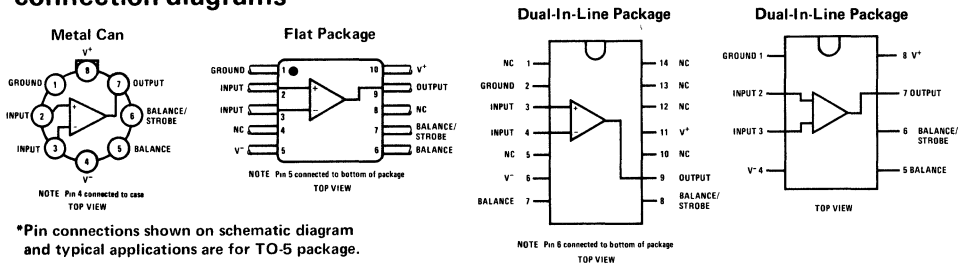
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C.

schematic diagram and auxiliary circuits





connection diagrams *



*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50K$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0 23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7 5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5 0	mA

Note 1: This rating applies for ±15V supplies The positive input voltage limit is 30V above the negative supply The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less

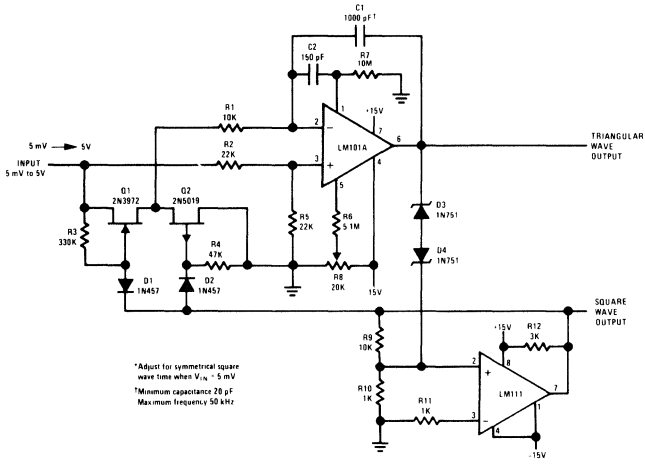
Note 2. The maximum junction temperature of the LM311 is 85°C For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$, unless otherwise specified The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies

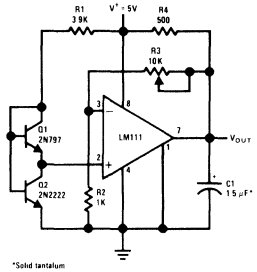
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive

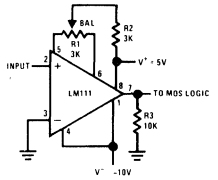
typical applications



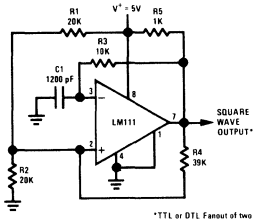
10 Hz to 10 kHz Voltage Controlled Oscillator



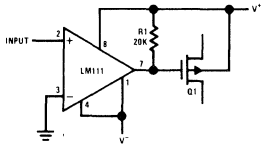
Low Voltage Adjustable Reference Supply



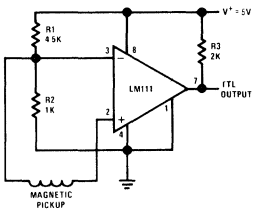
Zero Crossing Detector driving MOS logic



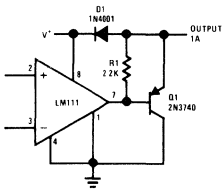
100 kHz Free Running Multivibrator



Zero Crossing Detector Driving MOS Switch

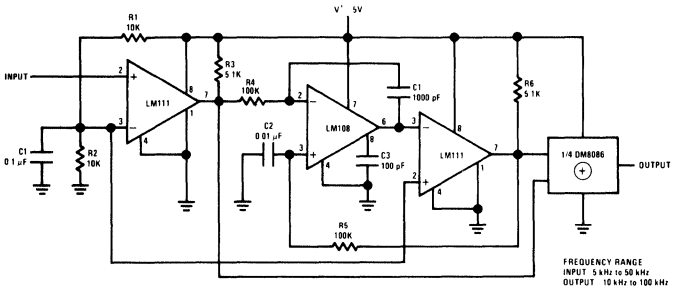


Detector for Magnetic Transducer

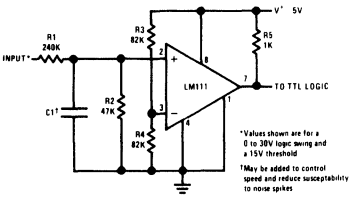


Comparator and Solenoid Driver

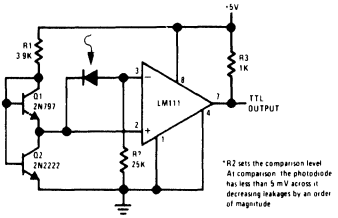
typical applications (con't)



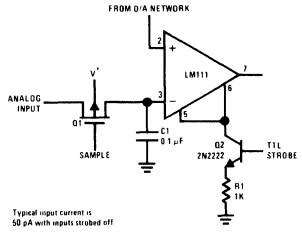
Frequency Doubler



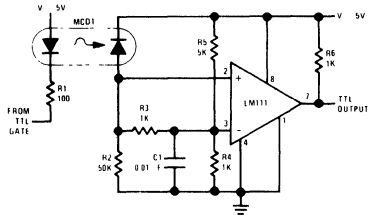
TTL Interface with High Level Logic



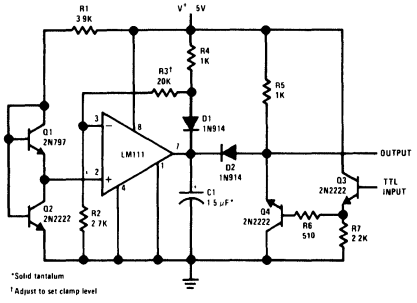
Precision Photodiode Comparator



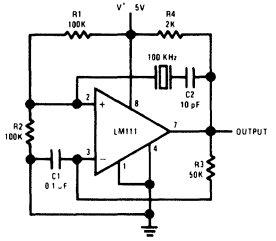
Strobing off Both Input* and Output Stages



Digital Transmission Isolator

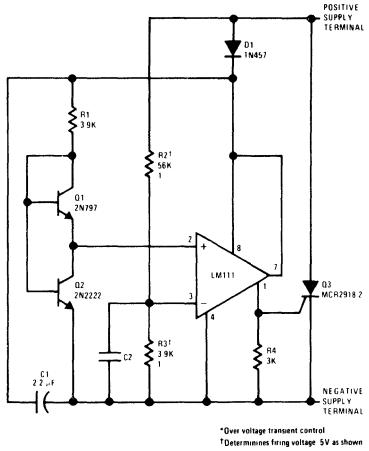


Precision Squarer

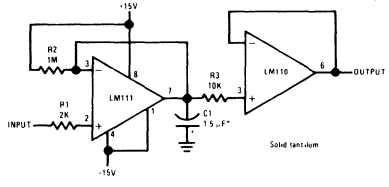


Crystal Oscillator

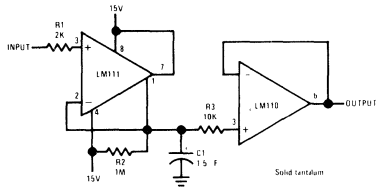
typical applications (con't)



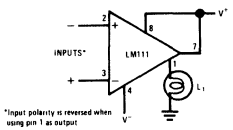
Crowbar Over-Voltage Protector



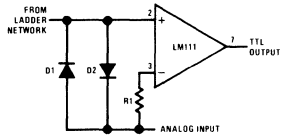
Negative Peak Dectector



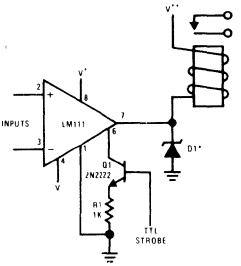
Positive Peak Detector



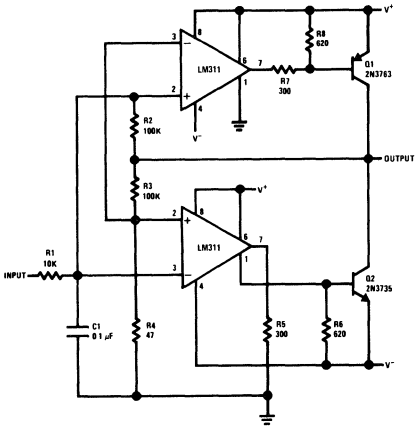
Driving Ground-Referred Load



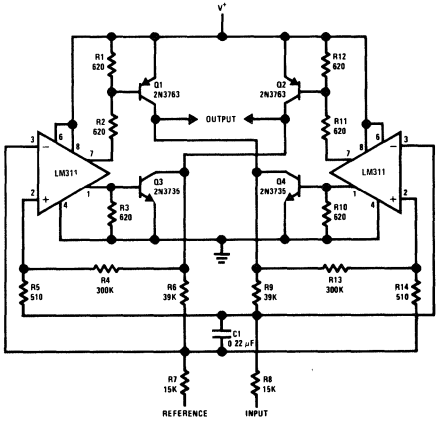
Using Clamp Diodes to Improve Response



Relay Driver with Strobe



Switching Power Amplifier



Switching Power Amplifier

Interface Circuits

LM350,LM75450A dual peripheral drivers

general description

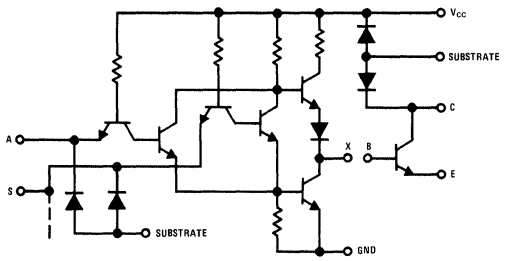
The LM350 and LM75450A are general purpose dual peripheral drivers. The design employs two standard TTL gates (NOR in LM350, NAND in LM75450A) and two totally uncommitted, high-voltage, high-current n-p-n transistors. These transistors are capable of sinking 300 mA and will withstand 30V in the OFF state. Inputs are fully DTL/TTL compatible. The LM75450A meets or exceeds the specifications for both the SN75450 and the SN75450A and is a pin-for-pin replacement.

features

- High speed
- High sink current 300 mA
- Separate gates and transistors
- Both transistors can sink 300 mA simultaneously
- Transistors withstand 30V collector to emitter in the OFF state
- Input clamp diodes

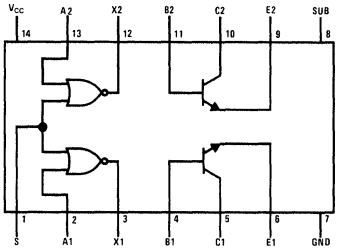
schematic and connection diagrams

LM350



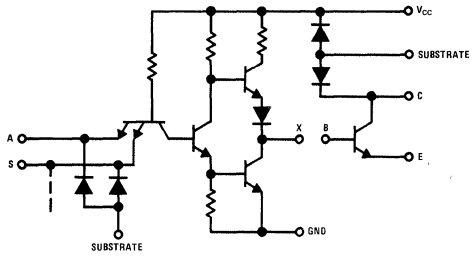
Note 1/2 of unit shown

Dual-In-Line Package
LM350



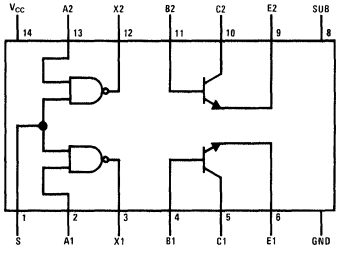
Positive Logic: $\overline{A+S} = X$

LM75450A



Note 1/2 of unit shown

Dual-In-Line Package
LM75450A



Positive Logic: $\overline{A \cdot S} = X$

absolute maximum ratings (Note 1)

Supply Voltage V_{CC}	7V	Emitter-Base Voltage	5V
Input Voltage	5 5V	Continuous Collector Current	300 mA
V_{CC} -to-Substrate Voltage	35V	Continuous Total Power Dissipation (Note 3)	800 mW
Collector-to-Substrate Voltage	35V	Operating Free-Air Temperature Range	0°C to 70°C
Collector-Base Voltage	35V	Storage Temperature Range	−65°C to 150°C
Collector-Emitter Voltage (Note 2)	30V		

electrical characteristics

The following apply for $0°C \leq T_A \leq 70°C$, V_{CC} = 5V ±5%, for LM350 and LM75450A unless otherwise specified.

TTL GATES

PARAMETER	COMMENTS	LOGIC INPUT	LOGIC OUTPUT	SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	Logic Output ≤ 0 4V	V_{IN}	16 mA	4 75V	2			V
Logical "0" Input Voltage	Logic Output ≥ 2 4V	V_{IN}	−400 mA	4 75V			0 8	V
Logical "1" Output Voltage		0 8V	−400 mA	4 75V	2 4			V
Logical "0" Output Voltage		2V	16 mA	4 75V			0 4	V
Logical "1" Input Current	A Input	2 4V		5 25V			40	μA
	S Input	2 4V		5 25V			80	μA
	A Input	5 5V		5 25V			1	mA
	S Input	5 5V		5 25V			2	mA
Logical "0" Input Current	A Input	0 4V		5 25V			−1 6	mA
	S Input	0 4V		5 25V			−3 2	mA
Output Short Circuit Current	Note 4	0V	0V	5 25V	−18		−55	mA
Supply Current								
Output Low								
LM350	Per Package	5V		5 25V		8	14	mA
LM75450A	Per Package	5V		5 25V		6	11	mA
Output High								
LM350	Per Package	0V		5 25V		4	7	mA
LM75450A	Per Package	0V		5 25V		2	4	mA
Input Diode Clamp Voltage	T_A = 25°C, V_{SUB} = 0V	−12 mA		5V			−1 5	V

TRANSISTORS

PARAMETER	COMMENTS	BASE	EMITTER	COLLECTOR	MIN	TYP	MAX	UNIT
BV_{CBO}		0V		100 μA	35			V
BV_{CER}	$R_{BE} \leq 500\Omega$		0V	100 μA	30			V
BV_{EBO}		0V	100 μA		5			V
V_{BE}		10 mA	0V	100 mA		0 85	1	V
		30 mA	0V	300 mA		1 05	1 2	V
$V_{CE(sat)}$		10 mA	0V	100 mA		0 25	0 4	V
		30 mA	0V	300 mA		0 5	0 7	V
h_{FE}	V_{CE} = 3V, T_A = 0°C, Note 5	I_B	0V	100 mA	20			
	V_{CE} = 3V, T_A = 0°C, Note 5	I_B	0V	300 mA	25			
	V_{CE} = 3V, T_A = 25°C, Note 5	I_B	0V	100 mA	25			
	V_{CE} = 3V, T_A = 25°C, Note 5	I_B	0V	300 mA	30			

The following apply for V_{CC} = 5V, T_A = 25°C

TTL GATES (Note 6)

PARAMETER	TYP	MAX
t_{pd1}	10 ns	22 ns
t_{pd0}	5 ns	15 ns

TRANSISTORS

PARAMETER	TYP	MAX
t_d	6 ns	15 ns
t_r	12 ns	20 ns
t_s	6 ns	15 ns
t_f	8 ns	15 ns

GATES AND TRANSISTORS (Note 7)

PARAMETER	TYP
t_{pd1}	14 ns
t_{pd0}	18 ns
t_r	5 ns
t_f	10 ns

Note 1: All voltage values are with respect to ground terminal. Positive current is defined to be current into referenced pin.

Note 2: With base-emitter resistance ≤ 500Ω.

Note 3: The maximum junction temperature is 150°C. For operating at elevated temperatures the package must be derated based on a thermal resistance of 150°C/W θ_{JA}.

Note 4: Only one output should be shorted at a time.

Note 5: These parameters are to be measured with less than 2% duty cycle.

Note 6: Delays measured with fanout of 10, 15 pF total load capacitance, measured from 1.5V input to 1.5V output.

Note 7: Delays measured with 50Ω load to 10V, 15 pF total load capacitance, measured from 1.5V input to 50% of output.

Interface Circuits

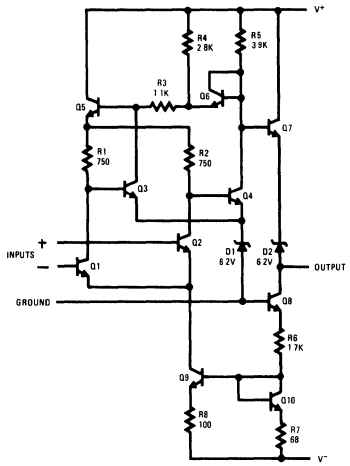
LM710 voltage comparator general description

The LM710 is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

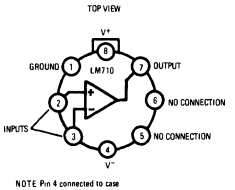
The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

schematic* and connection diagrams

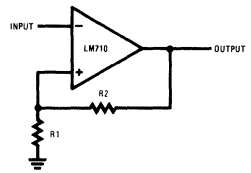


Metal Can Package

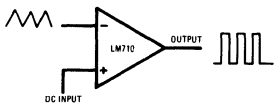


typical applications*

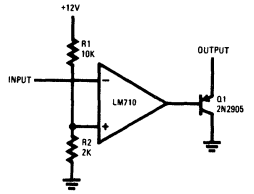
Schmidt Trigger



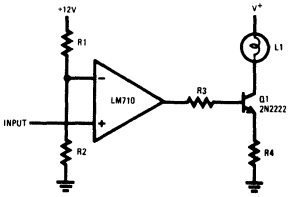
Pulse Width Modulator



Line Receiver With Increased Output Sink Current



Level Detector With Lamp Driver



*Pin connections shown are for metal can.

absolute maximum ratings

Positive Supply Voltage	14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation	
TO-99 (Note 1)	300 mW
Flat Package (Note 2)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 200\Omega$ $V_{CM} = 0V$		0 6	2 0	mV
Input Offset Current	$T_A = 25°C$, $V_{OUT} = 1\ 4V$		0 75	3 0	μA
Input Bias Current	$T_A = 25°C$		13	20	μA
Voltage Gain	$T_A = 25°C$	1250	1700		
Output Resistance	$T_A = 25°C$		200		Ω
Output Sink Current	$T_A = 25°C$ $V_{OUT} = 0$	2 0	2.5		mA
Response Time (Note 4)	$T_A = 25°C$		40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3 0	mV
Average Temperature Coefficient of Input Offset Voltage	$-55°C \leq T_A \leq 125°C$ $R_S \leq 50\Omega$		3 0	10	μV/°C
Input Offset Current	$T_A = 125°C$		0 25	3 0	μA
	$T_A = -55°C$		1 8	7 0	μA
Average Temperature	$25°C \leq T_A \leq 125°C$		5 0	25	nA/°C
Coefficient of Input Offset Current	$-55°C \leq T_A \leq 25°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7\ 0V$	±5 0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5 0V			V
Voltage Gain		1000			
Positive Output Level	$V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq -5$ mA	2 5	3 2	4 0	V
Negative Output Level	$V_{IN} \leq -5$ mV	−1 0	−0 5	0	V
Output Sink Current	$T_A = 125°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0$	0 5	1 7		mA
	$T_A = -55°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0$	1 0	2 3		mA
Positive Supply Current	$V_{IN} \leq -5$ mV		5 2	9 0	mA
Negative Supply Current			4.6	7 0	mA
Power Consumption	$V_{IN} \leq -5$ mV $I_{OUT} = 0$		90	150	mW

Note 1: Rating applies for case temperatures to +125°C, derate linearly at 5 6 mW/°C for ambient temperatures above +105°C

Note 2: Derate linearly at 4 4 mW/°C for ambient temperatures above +100°C

Note 3: These specifications apply for $V^+ = 12\ 0V$, $V^- = -6.0V$, $-55°C \leq T_A \leq +125°C$ unless otherwise specified The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1 8V at −55°C, 1 4V at +25°C, and 1 0V at +125°C

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive

Interface Circuits

LM710C voltage comparator

general description

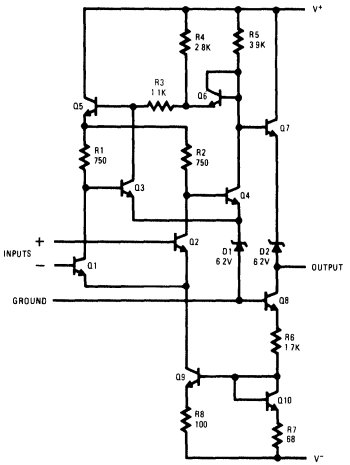
The LM710C is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

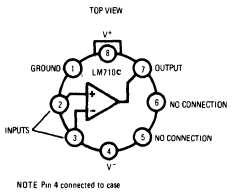
The LM710C is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

The LM710C is the commercial/industrial version of the LM710. It is identical to the LM710 except that operation is specified over a 0°C to 70°C temperature range.

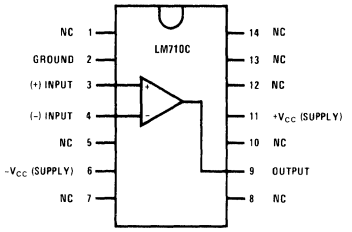
schematic and connection diagrams



Metal Can Package

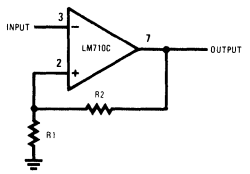


Dual-In-Line Package

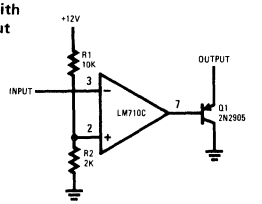


typical applications

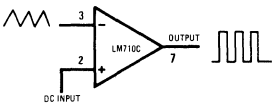
Schmidt Trigger



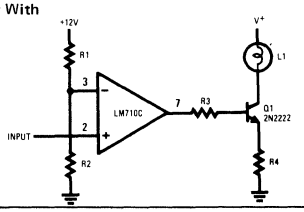
Line Receiver With Increased Output Sink Current



Pulse Width Modulator



Level Detector With Lamp Driver



absolute maximum ratings

Positive Supply Voltage	14.0V
Negative Supply Voltage	−7.0V
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation (Note 1)	300 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S < 200\Omega$ $V_{OUT} = 1.4V$		1.6	5.0	mV
Input Offset Current	$T_A = 25°C$, $V_{OUT} = 1.4V$		1.8	5.0	μA
Input Bias Current	$T_A = 25°C$		16	25	μA
Voltage Gain	$T_A = 25°C$	1000	1500		
Output Resistance	$T_A = 25°C$		200		Ω
Output Sink Current	$T_A = 25°C$, $\Delta V_{IN} \geq 5$ mV $V_{OUT} = 0$	1.7	2.5		mA
Response Time (Note 3)			40		ns
Input Offset Voltage	$R_S \leq 200\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$0°C \leq T_A \leq 70°C$ $R_S \leq 50\Omega$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		15 24	50 100	nA/°C nA/°C
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	70	98		
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq -5$ mA	2.5	3.2	4.0	V
Negative Output Level	$V_{IN} \leq -10$ mV	−1.0	−0.5	0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{IN} \leq -10$ mV		5.2	9	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption				150	mW

Note 1 Ratings apply for ambient temperatures to 70°C
Note 2 These specifications apply for $V^+ = 12.0V$, $V^- = 6.0V$, $0°C \leq T_A \leq 70°C$ and for a logic threshold voltage of 1.5V at 0°C, 1.4V at 25°C and 1.2V at 70°C unless otherwise specified
Note 3 The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Interface Circuits

LM711 dual comparator

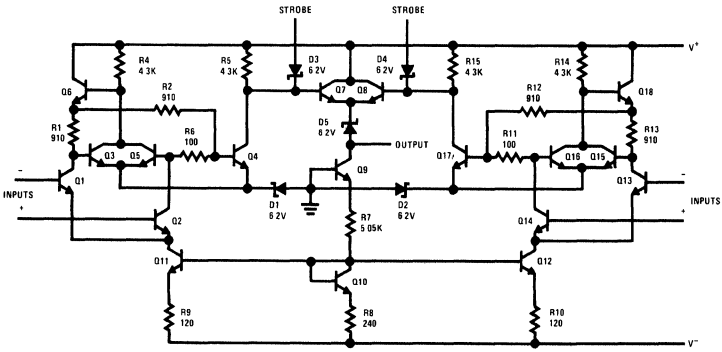
general description

The LM711 contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

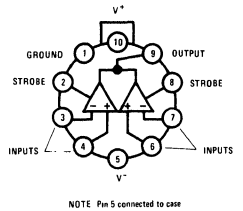
With the addition of an external resistor network, the LM711 can be used as a sense amplifier for core memories The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711 is also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711 is available in either an 10-lead low profile TO-5 header or a 1/4" by 1/4" metal flat package.

schematic and connection diagrams



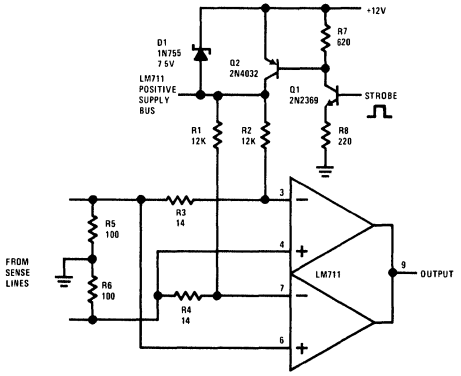
Metal Can Package



NOTE Pin 5 connected to case

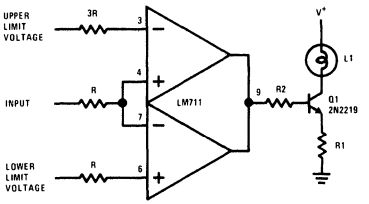
typical applications

Sense Amplifier With Supply Strobing for Reduced Power Consumption*



*Standby dissipation is about 40 mW

Double-Ended Limit Detector With Lamp Driver



absolute maximum ratings

Positive Supply Voltage	+14 0V
Negative Supply Voltage	-7.0V
Peak Output Current	25 mA
Differential Input Voltage	±5.0V
Input Voltage	±7 0V
Strobe Voltage	0 to +6.0V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

(These specifications apply for $T_A = 25°C$, $V^+ = 12V$, $V^- = -6V$)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$		1 0	3.5	mV
	$R_S \leq 200\Omega$		1 0	5.0	mV
Input Offset Current			0 5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0V$	±5 0			V
Differential Input Voltage Range		±5 0			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_O = -5$ mA	2 5	3.5		V
Negative Output Level	$V_{IN} \leq -10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3V$	-1 0		0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} \geq 0$	0 5	0 8		mA
Strobe Current	$V_{STROBE} = 0$		1 2	2.5	mA
Positive Supply Current	$V_{IN} \leq -10$ mV		8 6		mA
Negative Supply Current			3 9		mA
Power Consumption			130	200	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage (Note 3)	$R_S \leq 200\Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Average Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

Note 1: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

Note 2: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1 8V at -55°C, 1.4V at +25°C, and 1.0V at +125°C.

Note 3: The response time specified is for a 100 mV input step with 5 mV overdrive (see definitions).

Interface Circuits

LM711C dual comparator

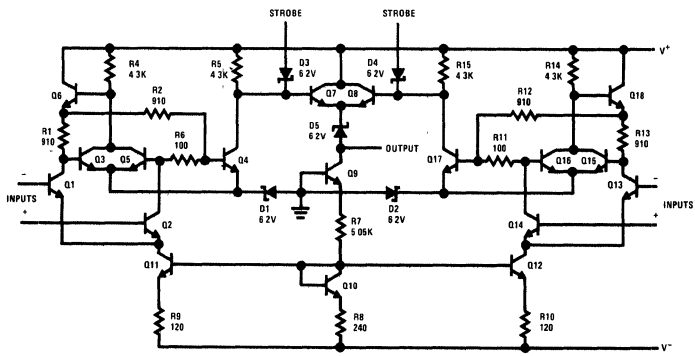
general description

The LM711C contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710C, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

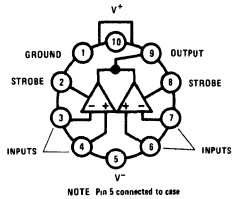
With the addition of an external resistor network, the LM711C can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711C is also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711C is the commercial/industrial version of the LM711. It is identical to the LM711, except that operation is specified over a 0°C to 70°C temperature range.

schematic and connection diagrams

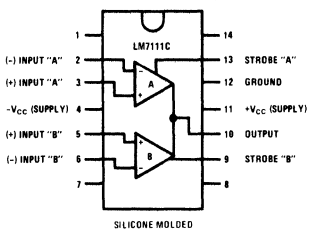


Metal Can Package



NOTE Pin 5 connected to case

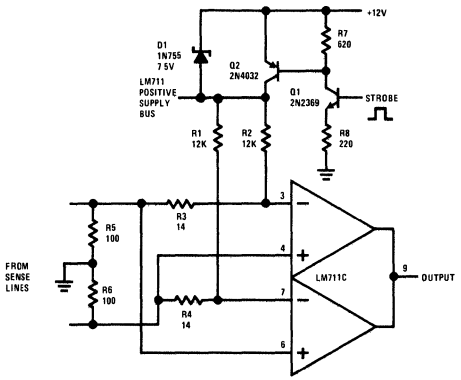
Dual-In-Line Package



SILICONE MOLDED

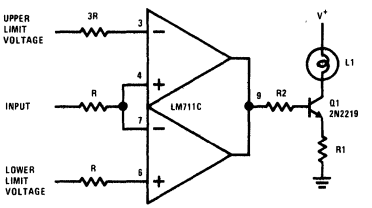
typical applications

Sense Amplifier With Supply Strobing for Reduced Power Consumption*



*Standby dissipation is about 40 mW

Double-Ended Limit Detector With Lamp Driver



absolute maximum ratings

Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	25 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Strobe Voltage	0 to +6.0V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

(These specifications apply for $T_A = 25°C$, $V^+ = 12V$, $V^- = -6V$)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$		1.0	5.0	mV
	$R_S \leq 200\Omega$		1.0	7.5	mV
Input Offset Current			0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^-=-7.0V	±5 0			V
Differential Input Voltage Range		±5 0			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_O = -5$ mA	2.5	3.5		V
Negative Output Level	$V_{IN} \leq -10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0$ 3V	-1 0		0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 0$		1.2	2.5	mA
Positive Supply Current	$V_{IN} \leq -10$ mV		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage (Note 3)	$R_S \leq 200\Omega$, $V_{CM} = 0$			6.0	mV
	$R_S \leq 200\Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Average Temperature Coefficient of input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

Note 1: Ratings apply for ambient temperatures to 70°C

Note 2: These specifications apply for $V^+ = 12.0V$, $V^- = 6.0V$, $0°C < T_A < 70°C$ and for a logic threshold voltage of 1.5V at 0°C, 1.4V at 25°C and 1.2V at 70°C unless otherwise specified

Note 3: The response time specified is for a 100 mV input step with 5 mV overdrive (see definitions).

Interface Circuits

LM1488 quad line driver

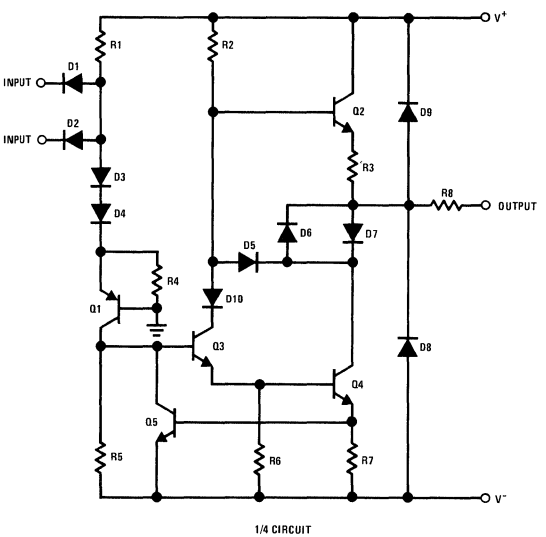
general description

The LM1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

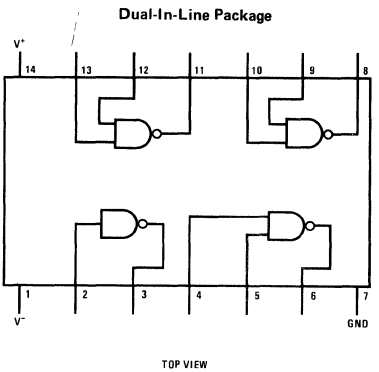
features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

schematic and connection diagrams



1/4 CIRCUIT



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Power Derating (Note 2)	
(Package Limitation, J Package)	1000 mW
Derating above $T_A = +25°C$ ($1/\theta_{JA}$)	6.7 mW/°C
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "0" Input Current	$V_{IN} = 0V$		−1 0	−1.3	mA
Logic "1" Input Current	$V_{IN} = +5\ 0V$		.005	10.0	μA
High Level Output Voltage	$R_L = 3\ 0k\Omega$, $V_{IN} = 0\ 8V$, $V^+ = 9\ 0V$, $V^- = -9.0V$	6.0	7 0		V
	$R_L = 3\ 0k\Omega$, $V_{IN} = 0\ 8V$, $V^+ = 13.2V$, $V^- = -13\ 2V$	9.0	10 5		V
Low Level Output Voltage	$R_L = 3\ 0k\Omega$, $V_{IN} = 1\ 9V$, $V^+ = 9.0V$, $V^- = -9.0V$	−6.0	−6.8		V
	$R_L = 3\ 0k\Omega$, $V_{IN} = 1\ 9V$, $V^+ = 13.2V$, $V^- = -13\ 2V$	−9.0	−10 5		V
High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$	−6 0	−10 0	−12 0	mA
Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1\ 9V$	6 0	10 0	12.0	mA
Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$	300			Ω
Positive Supply Current (Output Open)	$V_{IN} = 1\ 9V$, $V^+ = 9.0V$, $V^- = -9\ 0V$		15 0	20 0	mA
	$V_{IN} = 1\ 9V$, $V^+ = 12V$, $V^- = -12V$		19 0	25.0	mA
	$V_{IN} = 1\ 9V$, $V^+ = 15V$, $V^- = -15V$		25.0	34.0	mA
	$V_{IN} = 0.8V$, $V^+ = 9.0V$, $V^- = -9.0V$		4 5	6.0	mA
	$V_{IN} = 0.8V$, $V^+ = 12V$, $V^- = -12V$		5.5	7.0	mA
	$V_{IN} = 0.8V$, $V^+ = 15V$, $V^- = -15V$		8.0	12.0	mA
Negative Supply Current (Output Open)	$V_{IN} = 1.9V$, $V^+ = 9\ 0V$, $V^- = -9\ 0V$		−13.0	−17 0	mA
	$V_{IN} = 1.9V$, $V^+ = 12V$, $V^- = -12V$		−18 0	−23 0	mA
	$V_{IN} = 1.9V$, $V^+ = 15V$, $V^- = -15V$		−25.0	−34 0	mA
	$V_{IN} = 0.8V$, $V^+ = 9\ 0V$, $V^- = -9\ 0V$		−.001	−1.0	mA
	$V_{IN} = 0.8V$, $V^+ = 12V$, $V^- = -12V$		−.001	−1 0	mA
	$V_{IN} = 0.8V$, $V^+ = 15V$, $V^- = -15V$		−.01	−2.5	mA
Power Dissipation	$V^+ = 9.0V$, $V^- = -9.0V$		252	333	mW
	$V^+ = 12V$, $V^- = -12V$		444	576	mW
Propagation Delay to "1" (t_{pd1})	$R_L = 3.0\ k\Omega$ $C_L = 15\ pF$, $T_A = 25°C$		230	300	ns
Propagation Delay to "0" (t_{pd0})	$R_L = 3.0\ k\Omega$ $C_L = 15\ pF$, $T_A = 25°C$		70	175	ns
Rise Time (t_r)	$R_L = 3.0\ k\Omega$ $C_L = 15\ pF$, $T_A = 25°C$		75	100	ns
Fall Time (t_f)	$R_L = 3.0\ k\Omega$ $C_L = 15\ pF$, $T_A = 25°C$		40	75	ns

Note 1: Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: The maximum junction temperature of the LM1488 is 150°C. For operating at elevated temperatures the cavity Dual-In-Line Package (J) must be derated based on a thermal resistance of 85°C/W, junction to ambient.

Note 3: These specifications apply for $V^+ = +9.0V \pm 1\%$, $V^- = -9.0V \pm 1\%$, $T_A = 0°C$ to +75°C unless otherwise noted. All typicals are for $V^+ = 9.0V$, $V^- = -9.0V$, and $T_A = 25°C$.

applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the LM1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

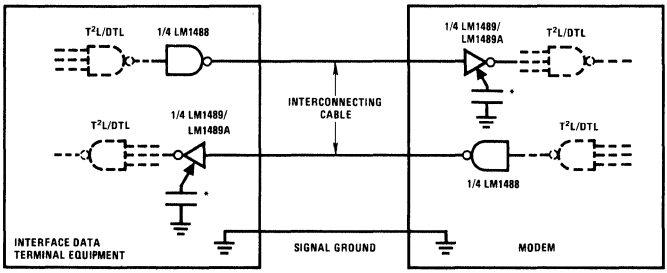
$$C = I_{SC} (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

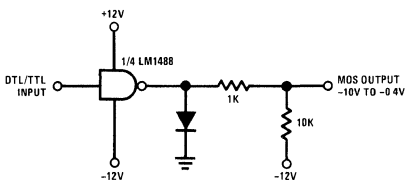
typical applications

RS232C Data Transmission

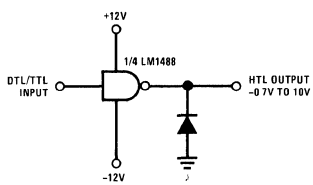


*OPTIONAL FOR NOISE FILTERING

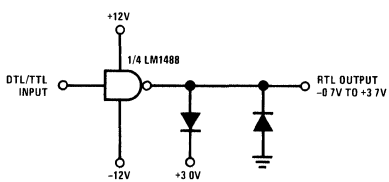
DTL/TTL-to-MOS Translator



DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator



Interface Circuits

LM1489/LM1489A quad line receiver

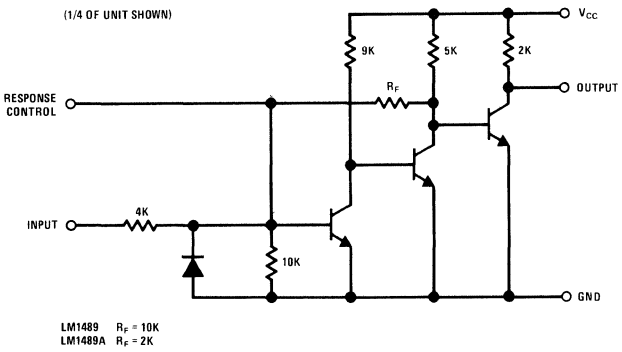
general description

The LM1489/LM1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The LM1489/LM1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The LM1489/LM1489A are available in 14 lead ceramic dual-in-line package.

features

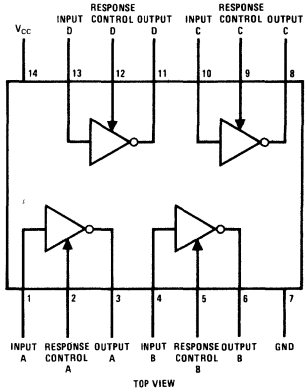
- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

schematic and connection diagrams



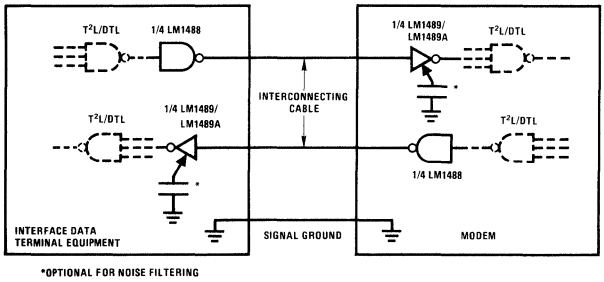
LM1489 R_F = 10K
LM1489A R_F = 2K

Dual-In-Line Package



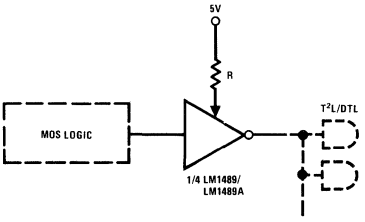
TOP VIEW

typical applications



*OPTIONAL FOR NOISE FILTERING

RS232C Data Transmission



MOS to T^2L/DTL Translator

absolute maximum ratings (Note 1)

The following apply for $T_A = 25°C$ unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C

electrical characteristics (Note 3)

LM1489/LM1489A The following apply for $V_{CC} = 5.0V \pm 1\%$, $0°C \leq T_A \leq +75°C$ unless otherwise specified

PARAMETER	CONDITIONS	LM1489			LM1489A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input High Threshold Voltage	$T_A = 25°C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10$ mA	1.0		1.5	1.75		2.25	V
Input Low Threshold Voltage	$T_A = 25°C$, $V_{OUT} \geq 2.5V$, $I_{OUT} = -0.5$ mA	0.75		1.25	0.75		1.25	V
Input Current	$V_{IN} = +25V$	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	$V_{IN} = -25V$	−3.6	−5.6	−8.3	−3.6	−5.6	−8.3	
	$V_{IN} = +3V$	+0.43	+0.53		+0.43	+0.53		mA
	$V_{IN} = -3V$	−0.43	−0.53		−0.43	−0.53		
Output High Voltage	$V_{IN} = 0.75V$, $I_{OUT} = -0.5$ mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, $I_{OUT} = -0.5$ mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output Low Voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10$ mA		0.33	0.45		0.33	0.45	V
Output Short Circuit Current	$V_{IN} = 0.75V$		3.0			3.0		mA
Supply Current	$V_{IN} = 5.0V$		14	26		14	26	mA
Power Dissipation	$V_{IN} = 5.0V$		70	130		70	130	mW
LM1489/LM1489A. The following apply for $V_{CC} = 5.0V \pm 1\%$, $T_A = 25°C$								
Input to Output "High" Propagation Delay (t_{pd1})	$R_L = 3.9k$ (Figure 1) (AC Test Circuit)		28	85		28	85	ns
Input to Output "Low" Propagation Delay (t_{pd0})	$R_L = 390\Omega$ (Figure 1) (AC Test Circuit)		20	50		20	50	ns
Output Rise Time	$R_L = 3.9k$ (Figure 1) (AC Test Circuit)		110	175		110	175	ns
Output Fall Time	$R_L = 390\Omega$ (Figure 1) (AC Test Circuit)		9	20		9	20	ns

Note 1: Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: For operation at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 85°C/W junction to case

Note 3: These specifications apply for response control pin = open.

Interface Circuits

LM1514/LM1414 dual differential voltage comparator

general description

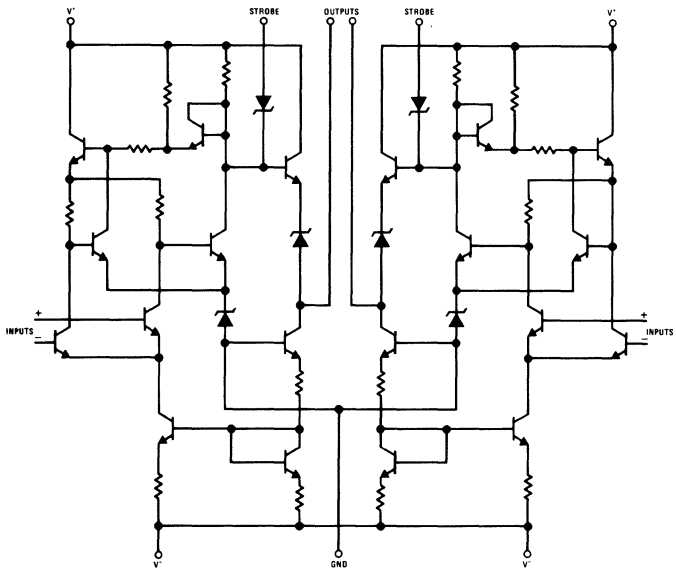
The LM1514/LM1414 is a dual differential voltage comparator intended for applications requiring high accuracy and fast response times. The device is constructed on a single monolithic silicon chip.

The LM1514/LM1414 is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. The LM1514/LM1414 meet or exceed the specifications for the MC1514/MC1414 and are pin-for-pin replacements. The LM1514 is available in the ceramic dual-in-line package. The LM1414 is available in either the ceramic or molded dual-in-line package.

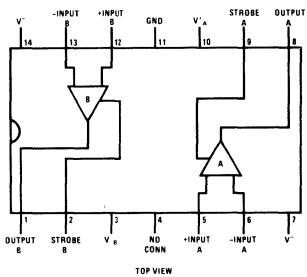
features

- Two totally separate comparators per package
- Independent strobe capability
- High speed 30 ns typ
- Low input offset voltage and current
- High output sink current over temperature
- Output compatible with TTL/DTL logic
- Molded or ceramic dual-in-line package

schematic and connection diagram



Dual-In-Line Package



9

absolute maximum ratings (Note 1)

Positive supply voltage	+14 0V	Power dissipation (Note 2)	600 mW
Negative supply voltage	−7 0V	Operating temperature Range LM1514	−55°C to +125°C
Peak output current	10 mA	LM1414	0°C to +70°C
Differential input voltage	±5.0V	Storage temperature range	−65°C to +150°C
Input voltage	±7 0V	Lead temperature (Soldering, 10 sec)	300°C

electrical characteristics for $T_A = 25°C$, $V^+ = +12V$, $V^- = -6V$, unless otherwise specified

PARAMETER	CONDITIONS	LM1514			LM1414			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $V_{OUT} = 1\ 4V$		0 6	2.0		1 0	5 0	mV
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1\ 4V$		0 8	3 0		1 2	5 0	μA
Input Bias Current				20			25	μA
Voltage Gain		1250			1000			
Output Resistance			200			200		Ω
Differential Input Voltage Range		±5 0			±5.0			V
Input Voltage Range	$V^- = -7.0V$	±5 0			±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$, $V^- = -7.0V$	80	100		70	100		dB
Positive Output Voltage	$V_{IN} \geq 7\ 0$ mV, $0 \leq I_{OUT} \leq -5\ 0$ mA	2 5	3 2	4 0	2 5	3 2	4 0	V
Negative Output Voltage	$V_{IN} \leq -7\ 0$ mV	−1 0	−0 5	0	−1 0	−0 5	0	V
Strobed Output Voltage	$V_{STROBE} \leq 0\ 3V$	−1 0	−0 5	0	−1 0	−0 5	0	V
Strobe "0" Current	$V_{STROBE} = 100$ mV		−1 2	−2 5		−1 2	−2 5	mA
Positive Supply Current	$V_{IN} \leq -7$ mV			18			18	mA
Negative Supply Current	$V_{IN} \leq -7$ mV			−14			−14	mA
Power Consumption			180	300		180	300	mW
Response Time	(Note 3)		30			30		ns
LM1514/LM1414. The following apply for $T_L \leq T_A \leq T_H$ (Note 4) unless otherwise specified								
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{OUT} = 1\ 8V$ for $T_A = T_L$			3 0			6 5	mV
	$V_{CM} = 0V$, $V_{OUT} = 1\ 0V$ for $T_A = T_H$			3 0			6 5	mV
Input Bias Current				45			40	μA
Temperature Coefficient of Input Offset Voltage			3 0			5 0		μV/°C
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1.8V$, $T_A = T_L$			7 0			7.5	μA
	$V_{CM} = 0V$, $V_{OUT} = 1\ 0V$, $T_A = T_H$			3.0			7.5	μA
Voltage Gain		1000			800			
Output Sink Current	$V_{IN} \leq -9$ mV, $V_{OUT} \geq 0V$	2 8	4.0		1.6	2 5		mA

Note 1: Voltage values are with respect to network ground terminal Positive current is defined as current into the referenced pin

Note 2: LM1514 ceramic package: The maximum junction temperature is +150°C, for operating at elevated temperatures, devices must be derated linearly at 12 5 mW/°C LM1414 ceramic package The maximum junction temperature is +95°C for operating at elevated temperatures, devices must be derated linearly at 12 5 mW/°C LM1414 molded package The maximum junction temperature is +115°C, for operating at elevated temperatures, devices must be derated linearly at 6 7 mW/°C

Note 3. The response time specified (see Definitions) for a 100 mV input step with 5 mV overdrive

Note 4: For LM1514, $T_L = -55°C$, $T_H = +125°C$ For LM1414, $T_L = 0°C$, $T_H = +70°C$

Interface Circuits

LM5520/LM7520 series
dual core memory sense amplifiers
general description

The devices in this series of dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible. All devices of the series have identical preamplifier configurations, while various logic connections are provided to suit the specific application.

The LM5520/LM7520 has output latch capability and provides sense, strobe, and memory function for two sense lines. The LM5522/LM7522 contains a single open collector output which may be used to expand the number of inputs of the LM5520/LM7520, or to drive an external Memory Data Register (MDR). Intended for small memories, the two channels of the LM5524/LM7524 are independent with two separate outputs. The LM5534/LM7534 is similar to the LM5524/LM7524 but has uncommitted, wire-ORable outputs. The LM5528/LM7528 has the same logic configuration of the LM5524/LM7524 and in addition provides separate low impedance Test Points at each preamplifier output. A similar device having uncommitted, wire-ORable outputs is the LM5538/LM7538.

features

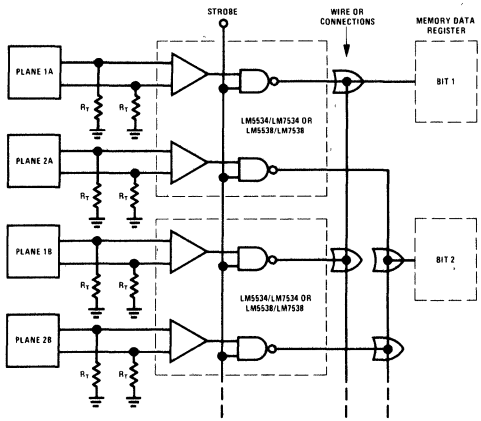
- High speed
- Guaranteed narrow threshold uncertainty over temperature.
- Adjustable input threshold voltage
- Fast overload recovery times
- Two amplifiers per package
- Molded or cavity dual-in-line package
- Six logic configurations

The part number ending with an even number (e.g., LM5520) designates a tighter guaranteed input threshold uncertainty than the subsequent odd number ending (e.g., LM5521). The remaining specifications for the two are identical. All devices meet or exceed the specifications for the corresponding device (where applicable) in the SN5520/SN7520 series and are pin-for-pin replacements.

absolute maximum ratings

Supply Voltage	±7V
Differential or Reference Input Voltage	±5V
Logic Input Voltage	+5.5V
Operating Temperature Range	
LM55XX	-55°C to +125°C
LM75XX	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

typical application



Expanded Small Memory System

LM5520/LM7520 and LM5521/LM7521 electrical characteristics

LM5520/LM5521: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF INPUT	REF. INPUT	STROBE INPUT	GATE Q INPUT	GATE $\bar{Q}$ INPUT	LOGIC OUTPUT (NOTE 3)	SUPPLY VOLT	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V	+5 25V	+5 25V		±5 25V	
LM7520/LM7521: The following apply for $0°C \leq T_A \leq 70°C$												
Differential Input Threshold Voltage (V_{TH}) (Note 4)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V	+5 25V	+5 25V		±5 25V	
LM5520/LM5521: The following apply for $-55°C \leq T_A \leq 125°C$ LM7520/LM7521: The following apply for $0°C \leq T_A \leq 70°C$												
Differential Input Offset Current		0 5		μA	0V	0V	+5 25V	+5 25V	+5 25V		±5 25V	
Logic "1" Input Voltage												
(Strobes)	2			V	40 mV	20 mV	+2V	+4 75V		−400 μA(Q)	±5V	Logic Output >2 4V
(Gate Q)	2			V	40 mV	20 mV	0V	+2V		+16 mA(Q)	±5V	Logic Output <0 4V
(Gate $\bar{Q}$)	2			V	40 mV	20 mV	0V	0V	+2V	+16 mA($\bar{Q}$)	±5V	Logic Output <0 4V
Logic "0" Input Voltage												
(Strobes)			0 8	V	40 mV	20 mV	+0 8V	+4 75V		+16 mA(Q)	±5V	Logic Output <0 4V
(Gate Q)			0 8	V	40 mV	20 mV	0V	+0 8V		−400 μA(Q)	±5V	Logic Output >2 4V
(Gate $\bar{Q}$)			0 8	V	40 mV	20 mV	0V	0V	+0 8V	−400 μA($\bar{Q}$)	±5V	Logic Output >2 4V
Logic "0" Input Current		−1	−1.6	mA	40 mV	20 mV	+0 4V	+0 4V	+0 4V		±5 25V	Each Input
Logic "1" Input Current		5	40	μA	0V	20 mV	+2 4V	+5 25V	+2 4V		±5 25V	Each Input
(Strobe & Gate $\bar{Q}$)		02	1	mA	0V	20 mV	+5 25V	+5 25V	+5 25V		±5 25V	Each Input
(Gate Q)		5	40	μA	40 mV	20 mV	+5 25V	+2 4V			±5 25V	
		02	1	mA	40 mV	20 mV	+5 25V	+5 25V			±5 25V	
Logic "1" Output Voltage												
(Strobe)	2 4	3 9		V	40 mV	20 mV	+2 0V	+5 25V		−400 μA(Q)	±4 75V	
(Gate Q)	2 4	3 9		V	40 mV	20 mV	0V	+0 8V		−400 μA(Q)	±4 75V	
(Gate $\bar{Q}$)	2 4	3 9		V	40 mV	20 mV	+4 75V	0V	+0 8V	−400 μA($\bar{Q}$)	±4 75V	
Logic "0" Output Voltage												
(Strobe)		0 25	0 40	V	40 mV	20 mV	+0 8V	+4 75V		+16 mA(Q)	±4 75V	
(Gate Q)		0 25	0 40	V	0V	20 mV	0V	+2V		+16 mA(Q)	±4 75V	
(Gate $\bar{Q}$)		0 25	0 40	V	0V	20 mV	0V	0V	+2V	+16 mA($\bar{Q}$)	±4 75V	
Q Output Short Circuit Current	−3	−4	−5	mA	0V	20 mV	0V	0V		0 V(Q)	±5 25V	
$\bar{Q}$ Output Short Circuit Current	−2 1	−2 8	−3 5	mA	0V	20 mV	0V	0V	0V	0 V($\bar{Q}$)	±5 25V	
V+ Supply Current		21	35	mA	0V	20 mV	0V	0V	0V		±5 25V	
V− Supply Current		−13	−18	mA	0V	20 mV	0V	0V	0V		±5 25V	

Note 1 For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5520 and LM5521 are guaranteed the same as LM7520 and LM7521, respectively

Note 2 Limits in parentheses pertain to LM5521, other limits pertain to LM5520

Note 3 Q or $\bar{Q}$ in parentheses indicate Q or $\bar{Q}$ logic output, respectively

Note 4 Limits in parentheses pertain to LM7521, other limits pertain to LM7520

Note 5 Positive current is defined as current into the referenced pin

Note 6 Pin 1 to have $\geq$100 pF capacitor connected to ground

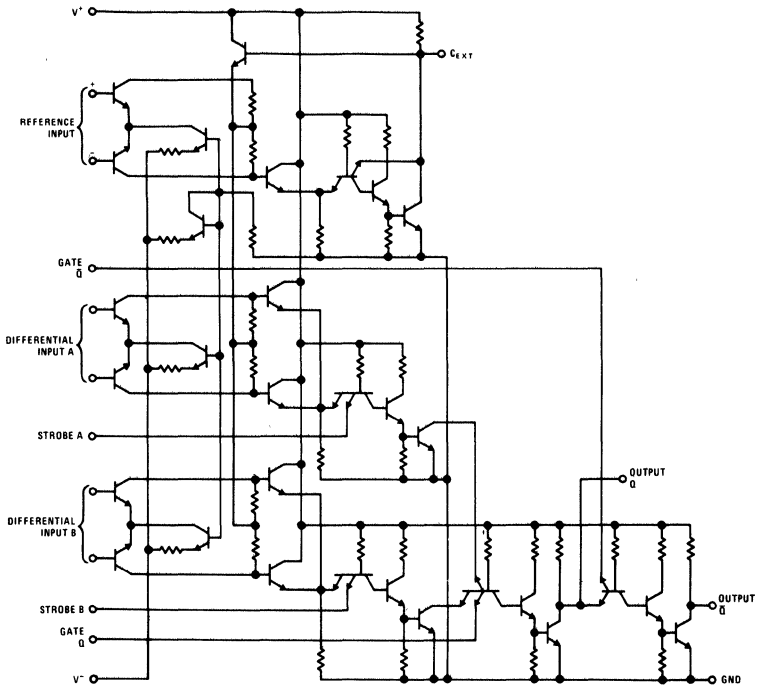
LM5520/LM7520 and LM5521/LM7521 electrical characteristics

LM5520/LM5521 and LM7520/LM7521: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS				
					DIFF INPUT	REF INPUT	STROBE AND GATE INPUTS	Q LOGIC OUTPUT	AC TEST CIRCUIT
AC Common Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE	
Propagation Delays									
Differential Input to Logical "1" Q Output		20	40	ns		20 mV			1
Differential Input to Logical "0" Q Output		28		ns		20 mV			1
Differential Input to Logical "1" $\bar{Q}$ Output		36		ns		20 mV			1
Differential Input to Logical "0" $\bar{Q}$ Output		28	55	ns		20 mV			1
Strobe Input to Logical "1" Q Output		10	30	ns		20 mV			1
Strobe Input to Logical "0" Q Output		20		ns		20 mV			1
Strobe Input to Logical "1" $\bar{Q}$ Output		33		ns		20 mV			1
Strobe Input to Logical "0" $\bar{Q}$ Output		16	55	ns		20 mV			1
Gate Q Input to Logical "1" Q Output		12	20	ns		20 mV			2
Gate Q Input to Logical "0" Q Output		6		ns		20 mV			2
Gate Q Input to Logical "1" $\bar{Q}$ Output		17		ns		20 mV			2
Gate Q Input to Logical "0" $\bar{Q}$ Output		19	30	ns		20 mV			2
Gate $\bar{Q}$ Input to Logical "1" $\bar{Q}$ Output		12		ns		20 mV			2
Gate $\bar{Q}$ Input to Logical "0" $\bar{Q}$ Output		6	20	ns		20 mV			2
Diff Input Overload Recovery Time		10		ns					
Common Mode Input Overload Recovery Time		5		ns					
Min Cycle Time		200		ns					

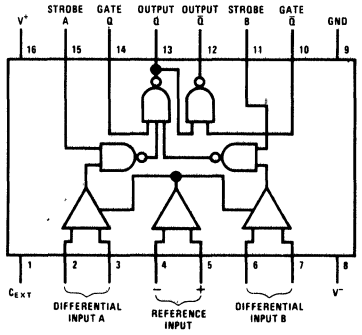
LM5520/LM7520 and LM5521/LM7521

schematic diagram



connection diagram

Dual-In-Line Package



LM5522/LM7522 and LM5523/LM7523
electrical characteristics

LM5522/LM5523: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF INPUT	REF INPUT	STROBE INPUT	GATE INPUT	LOGIC OUTPUT	SUPPLY VOLT	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V	-400 µA	±5V	Logic Output >2 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V	+16 mA	±5V	Logic Output <0 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V	-400 µA	±5V	Logic Output >2 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V	+16 mA	±5V	Logic Output <0.4V
Differential & Reference Input Bias Current		30	100	µA	0V	0V	+5 25V	+5 25V		±5 25V	
LM7522/LM7523: The following apply for $0°C \leq T_A \leq 70°C$											
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V	-400 µA	±5V	Logic Output >2 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V	+16 mA	±5V	Logic Output <0 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V	-400 µA	±5V	Logic Output >2 4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V	+16 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	75	µA	0V	0V	+5 25V	+5 25V		±5 25V	
LM5522/LM5523: The following apply for $-55°C \leq T_A \leq 125°C$ **LM7522/LM7523: The following apply for $0°C \leq T_A \leq 70°C$**											
Diff Input Offset Current		0 5		µA	0V	0V	+5 25V	+5 25V		±5 25V	
Logic "1" Input Voltage (Strobes)	2			V	40 mV	20 mV	+2V	+4 75V	+16 mA	±5V	Logic Output <0 4V
(Gate)	2			V	40 mV	20 mV	0V	+2V	-400 µA	±5V	Logic Output >2 4V
Logic "0" Input Voltage (Strobes)			0 8	V	40 mV	20 mV	+0 8V	+4 75V	-400 µA	±5V	Logic Output >2 4V
(Gate)			0 8	V	40 mV	20 mV	0V	+0 8V	+16 mA	±5V	Logic Output <0 4V
Logic "0" Input Current		-1	-1 6	mA	40 mV	20 mV	+0 4V	+0 4V		±5 25V	Each Input
Logic "1" Input Current (Strobes)			40	µA	0V	20 mV	+2 4V	+5 25V		±5 25V	
			1	mA	0V	20 mV	+5 25V	+5 25V		±5 25V	
(Gate)			40	µA	40 mV	20 mV	+5 25V	+2 4V		±5 25V	
			1	mA	40 mV	20 mV	+5 25V	+5 25V		±5 25V	
Logic "1" Output Voltage	2 4	3 9		V	40 mV	20 mV	+0 8V	+2V	-400 µA	±4 75V	
Logic "0" Output Voltage (Strobes)		0 25	0 40	V	40 mV	20 mV	+2V	+4.75V	+16 mA	±4 75V	Tie Pins 10 and 12
(Gate)		0 25	0 40	V	40 mV	20 mV	0V	+0 8V	+16 mA	±4 75V	Tie Pins 10 and 12
Output Short Circuit Current	-2 1	-2 8	-3 5	mA	40 mV	20 mV	0V	+5 25V	0V	±5 25V	Tie Pins 10 and 12
Output Leakage Current		0 01	250	µA	0V	20 mV	0V	+2V	+5 25V	±4 75V	
V^+ Supply Current		23	36	mA	0V	20 mV	0V	0V		±5 25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V	0V		±5 25V	
LM5522/LM5523 and LM7522/LM7523. The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$											
AC Common Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	+5V	SCOPE		
Propagation Delays Differential Input to Logical "1" Output		26		ns		20 mV					AC Test Circuit
Differential Input to Logical "0" Output		21	45	ns		20 mV					AC Test Circuit
Strobe Input to Logical "1" Output		22		ns		20 mV					AC Test Circuit
Strobe Input to Logical "0" Output		12	40	ns		20 mV					AC Test Circuit
Gate Input to Logical "1" Output		4		ns		20 mV					AC Test Circuit
Gate Input to Logical "0" Output		15	25	ns		20 mV					AC Test Circuit
Differential Input Over load Recovery Time		10		ns							
Common Mode Input Overload Recovery Time		5		ns							
Min Cycle Time		200		ns							

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5522 and LM5523 are guaranteed the same as LM7522 and LM7523, respectively

Note 2 Limits in parentheses pertain to LM5523, other limits pertain to LM5522

Note 3. Limits in parentheses pertain to LM7523, other limits pertain to LM7522

Note 4 Positive current is defined as current into the referenced pin

Note 5: Pin 1 to have $\geq$100 pF capacitor connected to ground

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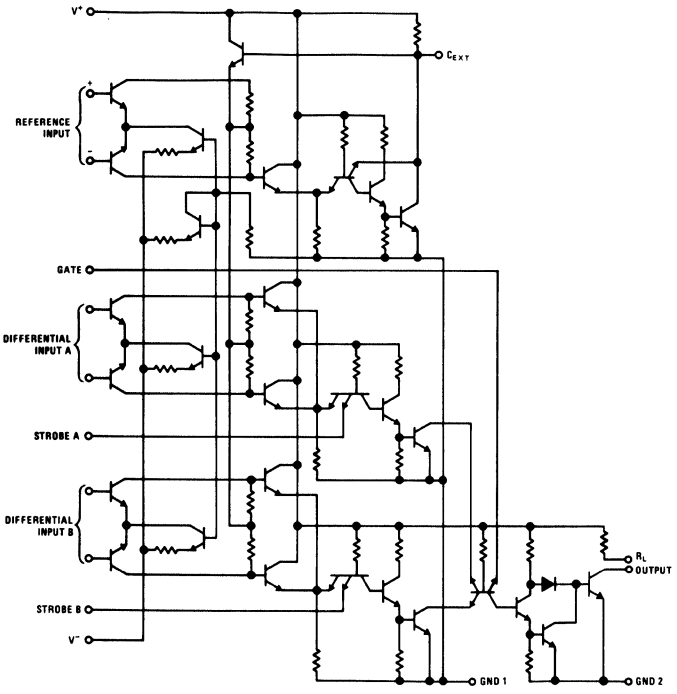
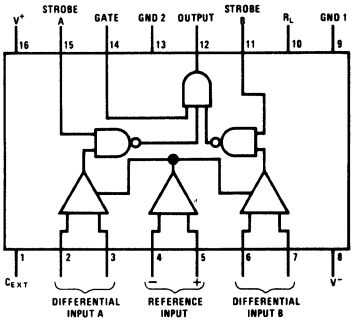
LM5522/LM7522 and LM5523/LM7523

schematic diagram



connection diagram

Dual-In-Line Package



LM5524/LM7524 and LM5525/LM7525 electrical characteristics

LM5524/LM5525: The following apply for $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	−400 μA	±5V	Logic Output >2 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	−400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5 25V	
LM7524/LM7525: The following apply for $0^{\circ}C \leq T_A \leq 70^{\circ}C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	−400 μA	±5V	Logic Output >2 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	−400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5524/LM5525: The following apply for $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ LM7524/LM7525: The following apply for $0^{\circ}C \leq T_A \leq 70^{\circ}C$										
Diff Input Offset Current		0 5		μA	0V	0V	+5 25V		±5 25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	−400 μA	±5V	Logic Output >2 4V
Logic "0" Input Voltage			0 8	V	40 mV	20 mV	+0 8V	+16 mA	±5V	Logic Output <0 4V
Logic "0" Input Current		−1	−1 6	mA	40 mV	20 mV	+0 4V		±5 25V	
Logic "1" Input Current		5	40	μA	0V	20 mV	+2 4V		±5 25V	
		0 02	1	mA	0V	20 mV	+5 25V		±5 25V	
Logic "1" Output Voltage	2 4	3 9		V	40 mV	20 mV	+2 0V	−400 μA	±4 75V	
Logic "0" Output Voltage		0 25	0 40	V	40 mV	20 mV	+0 8V	+16 mA	±4 75V	
Output Short Circuit Current	−2 1	−2 8	−3 5	mA	40 mV	20 mV	+5 25V	0V	±5 25V	
V^+ Supply Current		29	40	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		−13	−18	mA	0V	20 mV	0V		±5 25V	
LM5524/LM5525 and LM7524/LM7525: The following apply for $T_A = 25^{\circ}C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		20	40	ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		28		ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		10	30	ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		20		ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min Cycle Time		200		ns						

Note 1 For $0^{\circ}C \leq T_A \leq 70^{\circ}C$ operation, electrical characteristics for LM5524 and LM5525 are guaranteed the same as LM7524 and LM7525 respectively

Note 2 Limits in parentheses pertain to LM5525, other limits pertain to LM5524

Note 3. Limits in parentheses pertain to LM7525, other limits pertain to LM7524

Note 4 Positive current is defined as current into the referenced pin

Note 5: Pin 1 to have $\geq$100 pF capacitor connected to ground

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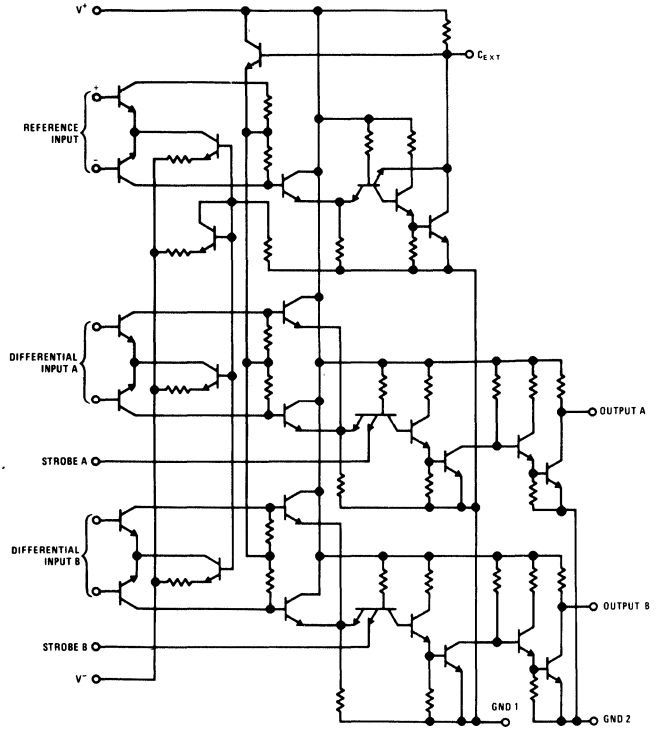
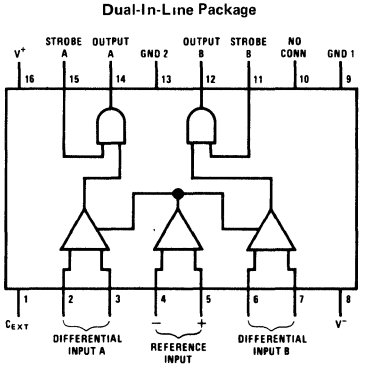
LM5524/LM7524 and LM5525/LM7525

schematic diagram



connection diagram

Dual-In-Line Package



LM5528/LM7528 and LM5529/LM7529 electrical characteristics

LM5528/LM5529: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	−400 μA	±5V	Logic Output >2 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	−400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5 25V	
LM7528/LM7529: The following apply for $0°C \leq T_A \leq 70°C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	−400 μA	±5V	Logic Output >2 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	−400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5528/LM5529: The following apply for $-55°C \leq T_A \leq 125°C$ LM7528/LM7529: The following apply for $0°C \leq T_A \leq 70°C$										
Diff Input Offset Current		0 5		μA	0V	0V	+5 25V		±5 25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	−400 μA	±5V	Logic Output >2 4V
Logic "0" Input Voltage			0 8	V	40 mV	20 mV	+0 8V	+16 mA	±5V	Logic Output <0 4V
Logic "0" Input Current		−1	−1 6	mA	40 mV	20 mV	+0 4V		±5 25V	
Logic "1" Input		5	40	μA	0V	20 mV	+2 4V		±5 25V	
Current		0 02	1	mA	0V	20 mV	+5 25V		±5 25V	
Logic "1" Output Voltage	2 4	3 9		V	40 mV	20 mV	+2 0V	−400 μA	±4 75V	
Logic "0" Output Voltage		0 25	0 40	V	40 mV	20 mV	+0 8V	+16 mA	±4 75V	
Output Short Circuit Current	−2 1	−2 8	−3 5	mA	40 mV	20 mV	+5 25V	0V	±5 25V	
V^+ Supply Current		29	40	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		−13	−18	mA	0V	20 mV	0V		±5 25V	
LM5528/LM5529 and LM7528/LM7529: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		20	40	ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		28		ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		10	30	ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		20		ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min Cycle Time		200		ns						

Note 1 For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5528 and LM5529 are guaranteed the same as LM7528 and LM7529 respectively

Note 2 Limits in parentheses pertain to LM5529, other limits pertain to LM5528

Note 3. Limits in parentheses pertain to LM7529, other limits pertain to LM7528

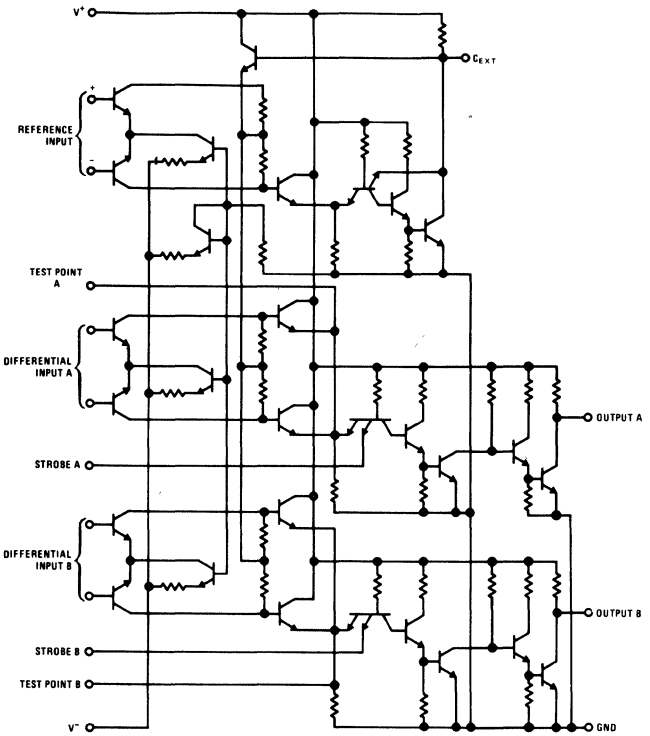
Note 4: Positive current is defined as current into the referenced pin

Note 5. Pin 1 to have $\geq$100 pF capacitor connected to ground

Note 6: Each test point to have $\leq$15 pF capacitive load to ground

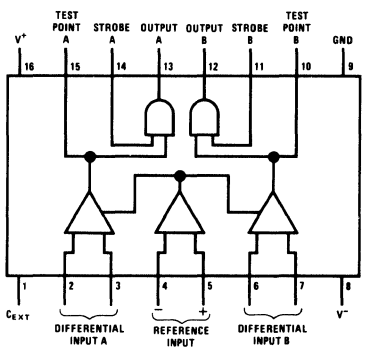
LM5528/LM7528 and LM5529/LM7529

schematic diagram



connection diagram

Dual-In-Line Package



LM5534/LM7534 and LM5535/LM7535 electrical characteristics

LM5534/LM5535: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF INPUT	REF INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5 25V	
LM7534/LM7535: The following apply for $0°C \leq T_A \leq 70°C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5534/LM5535: The following apply for $-55°C \leq T_A \leq 125°C$ LM7534/LM7535: The following apply for $0°C \leq T_A \leq 70°C$										
Diff Input Offset Current		0 5		μA	0V	0V	+5 25V		±5 25V	
Logic "0" Input Voltage			0 8	V	40 mV	20 mV	+0 8V	+5 25V	±5V	Logic Output <250 μA
Logic "1" Input Voltage	2 0			V	40 mV	20 mV	+2 0V	+20 mA	±5V	Logic Output <0 4V
Logic "0" Input Current		-1	-1 6	mA	40 mV	20 mV	+0 4V		±5 25V	
Logic "1" Input Current		5	40	μA	0V	20 mV	+2 4V		±5 25V	
		0 02	1	mA	0V	20 mV	+5 25V		±5 25V	
Logic "0" Output Voltage		0 25	0 40	V	40 mV	20 mV	+2V	+20 mA	±4 75V	
Output Leakage Current		0 01	250	μA	40 mV	20 mV	+0 8V	+5 25V	±4 75V	
V^+ Supply Current		28	38	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V		±5 25V	
LM5534/LM5535 and LM7534/LM7535: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		24		ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		20	40	ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		16		ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		10	30	ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min Cycle Time		200		ns						

Note 1 For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5534 and LM5535 are guaranteed the same as LM7534 and LM7535 respectively

Note 2: Limits in parentheses pertain to LM5535, other limits pertain to LM5534

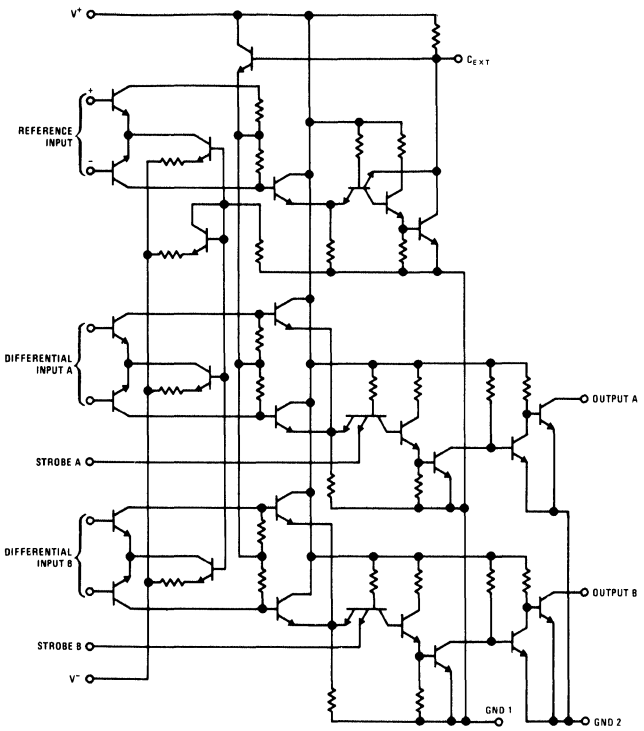
Note 3: Limits in parentheses pertain to LM7535, other limits pertain to LM7534

Note 4: Positive current is defined as current into the referenced pin

Note 5: Pin 1 to have $\geq$ 100 pF capacitor connected to ground

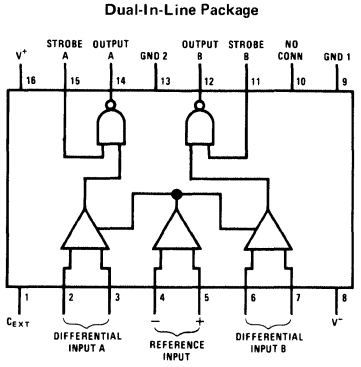
LM5534/LM7534 and LM5535/LM7535

schematic diagram



connection diagram

Dual-In-Line Package



LM5538/LM7538 and LM5539/LM7539 electrical characteristics

LM5538/LM5539: The following apply for $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF INPUT	REF INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	-20 mA	±5V	Logic Output <0 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5 25V	
LM7538/LM7539 The following apply for $0^{\circ}C \leq T_A \leq 70^{\circ}C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5538/LM5539. The following apply for $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ LM7538/LM7539: The following apply for $0^{\circ}C \leq T_A \leq 70^{\circ}C$										
Diff Input Offset Current		0 5		μA	0V	0V	+5 25V		±5 25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	+20 mA	±5V	Logic Output <0 4V
Logic "0" Input Voltage			0 8	V	40 mV	20 mV	+0 8V	+5 25V	±5V	Logic Output <250 μA
Logic "0" Input Current		-1	-1 6	mA	40 mV	20 mV	+0 4V		±5 25V	
Logic "1" Input		5	40	μA	0V	20 mV	+2 4V		±5 25V	
Current		0 02	1	mA	0V	20 mV	+5 25V		±5 25V	
Logic "0" Output Voltage		0 25	0 40	V	40 mV	20 mV	+2 0V	+20 mA	±4 75V	
Output Leakage Current		0 01	250	μA	40 mV	20 mV	+0 8V	+5 25V	±4 75V	
V^+ Supply Current		28	38	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V		±5 25V	
LM5538/LM5539 and LM7538/LM7539: The following apply for $T_A = 25^{\circ}C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		24		ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		20	40	ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		16		ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		10	30	ns		20 mV				AC Test Circuit
Differential Input Over load Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min Cycle Time		200		ns						

Note 1 For $0^{\circ}C \leq T_A \leq 70^{\circ}C$ operation, electrical characteristics for LM5538 and LM5539 are guaranteed the same as LM7538 and LM7539 respectively

Note 2 Limits in parentheses pertain to LM5539, other limits pertain to LM5538

Note 3. Limits in parentheses pertain to LM7539, other limits pertain to LM7538

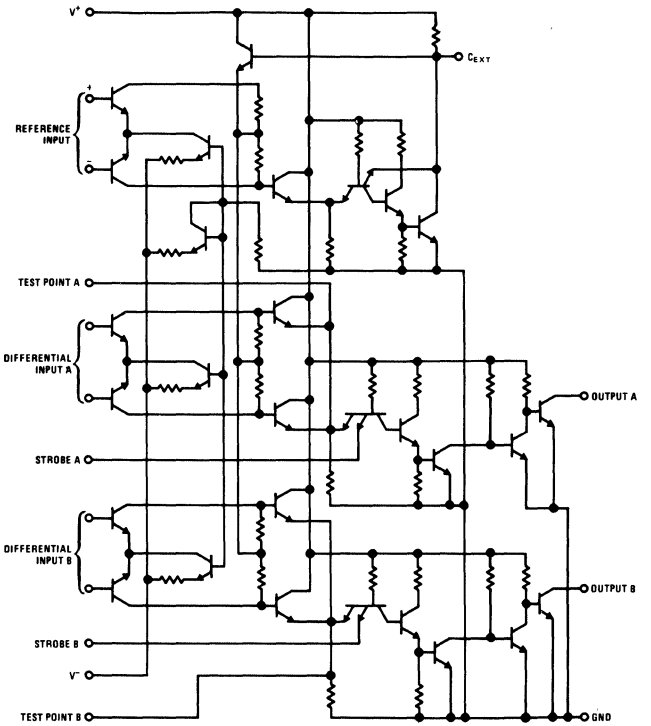
Note 4. Positive current is defined as current into the referenced pin

Note 5 Pin 1 to have $\geq$100 pF capacitor connected to ground

Note 6. Each test point to have $\leq$15 pF capacitive load to ground

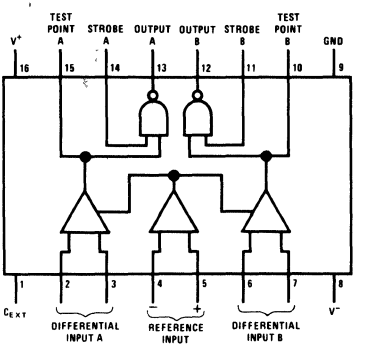
LM5538/LM7538 and LM5539/LM7539

schematic diagram



connection diagram

Dual-In-Line Package



Interface Circuits

LM75451A, LM75452, LM75453 dual peripheral drivers

general description

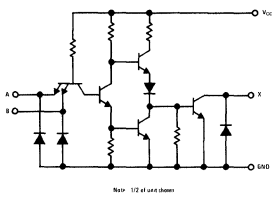
These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300 mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible. The LM75451A meets or exceeds the specifications for both the SN75451 and SN75451A and is a pin-for-pin replacement. The LM75452 and LM75453 meet or exceed the specifications for SN75452 and SN75453, respectively, and are pin-for-pin replacements.

features

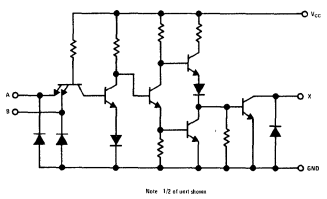
- High speed – 20 ns max (LM75451A, LM75453)
  25 ns max (LM75452)
- Both outputs can sink 300 mA simultaneously
- Withstands 30V on output with V_{CC} = 0V for power strobing applications
- Input clamp diodes
- Two separate drivers per package

schematic diagrams

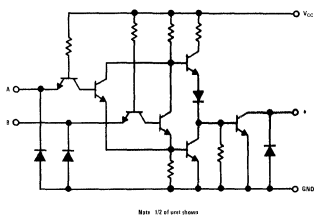
LM75451A



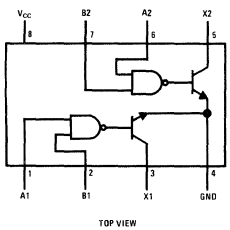
LM75452



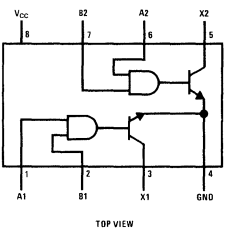
LM75453



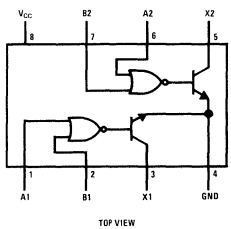
connection diagrams



TOP VIEW



TOP VIEW



TOP VIEW

truth tables

Positive logic AB=X

A	B	OUTPUT X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output ≤ 0.7V
"1" Output ≤ 100 μA

Positive logic $\overline{AB}$=X

A	B	OUTPUT X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output ≤ 0.7V
"1" Output ≤ 100 μA

Positive logic A + B = X

A	B	OUTPUT X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output ≤ 0.7V
"1" Output ≤ 100 μA

absolute maximum ratings (Note 1)

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Output Voltage (Note 2)	30V
Continuous Output Current	300 mA
Continuous Total Power Dissipation (Note 3)	800 mW
Operating Free Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics

The following apply for $0°C \leq T_A \leq 70°C$, V_{CC} = 5V ±5%, unless otherwise specified (Note 4)

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNIT
Logic "1" Input Voltage	V_{IN}	30V (300 mA)	4 75V	Output $\leq$ 100 µA ($\leq$0 7V)	2			V
Logic "0" Input Voltage	V_{IN}	300 mA (30V)	4 75V	Output $\leq$ 0 7V ($\leq$100 µA)			0 8	V
Output Leakage Currents	2V (0 8V)	30V	4 75V				100	µA
		30V	0V				100	µA
Output LOW Voltages	0 8V (2V)	100 mA	4 75V			0 25	0 4	V
	0 8V (2V)	300 mA	4 75V			0 5	0 7	V
Logic "1" Input Currents	2 4V		5 25V				40	µA
	5 5V		5 25V				1	mA
Logic "0" Input Current	0 4V		5 25V			−1	−1 6	mA
Supply Currents								
Output Low								
LM75451A	0V		5 25V	Per Package		48	60	mA
LM75452	5V		5 25V	Per Package		51	65	mA
LM75453	0V		5 25V	Per Package		50	63	mA
Output High								
LM75451A	5V		5 25V	Per Package		7	11	mA
LM75452	0V		5 25V	Per Package		9	14	mA
LM75453	5V		5 25V	Per Package		9	14	mA
Input Diode Clamp Voltage	−12 mA		5V	T_A = 25°C			−1 5	V
The following apply for V_{CC} = 5V, T_A = 25°C								
Propagation Delay Times								
Input to Output HIGH								
LM75451A & LM75453			(Note 5)			11	20	ns
LM75452			(Note 5)			13	25	ns
Input to Output LOW								
LM75451A & LM75453			(Note 5)			16	20	ns
LM75452			(Note 5)			19	25	ns
Output Risetime						4		ns
Output Falltime						10		ns

Note 1: All voltage values are with respect to ground terminal Positive current is defined to be current into referenced pin

Note 2: Maximum voltage to be applied to either output in the off state

Note 3: The maximum junction temperature is 150°C For operating at elevated temperatures, the package must be derated based on a thermal resistance of 110°C/W θ_{JA}

Note 4: Test conditions in parentheses pertain to LM75452, other test conditions pertain to LM75451A and LM75453

Note 5: Delays measured with 50Ω load to 10V, 15 pF total load capacitance, measured from 1 5V input to 50% of output.

Interface Circuits

LM75454 dual NOR peripheral line driver

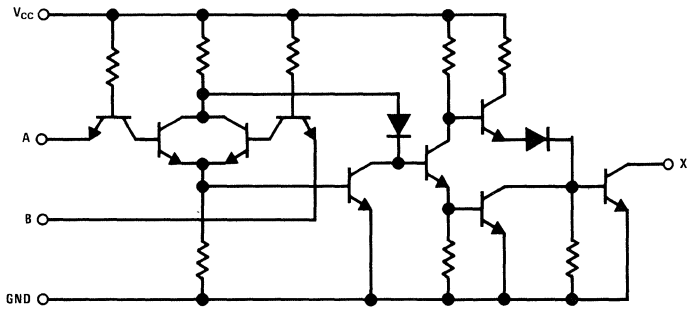
general description

The LM75454 is a dual NOR peripheral line driver with output transistors rated up to 300mA continuous current. Both output transistors can sink this current at the same time, bringing maximum chip power dissipation to 820mW. Switching speeds are compatible with standard TTL and logic levels interface directly with TTL, DTL, and LPTTL logic families. The overall input to output NOR function allows pin for pin replacement with TI's SN75454 positive logic NOR driver.

features

- High speed, 25 ns maximum
- Both outputs can sink 300 mA simultaneously
- Withstands 30V on outputs
- Input clamp diodes
- Maximum package power dissipation at maximum current rating $\leq$ 820 mW

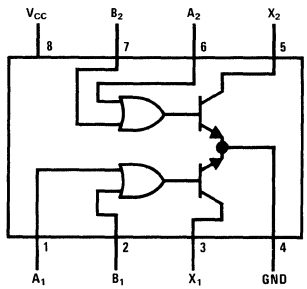
schematic diagram



NOTE 1/2 SCHEMATIC SHOWN

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage (Note 4)	30V
Continuous Output Current	300mA
Continuous Total Power Dissipation (Note 2)	820mW
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics The following apply at $0°C \leq T_A \leq +70°C$, V_{CC} = 5V + 5% unless otherwise noted

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IN}	300mA	4 75V	Output $\leq$ 0 7V	2 0			V
Logical "0" Input Voltage	V_{IN}	30V	4 75V	Output $\leq$ 100μA			0 8	V
Logical "1" Input Current	2 4V		5 25V				40	μA
	5 5V		5 25V				1	mA
Logical "0" Input Current	0 4V		5 25V			−1 0	−1 6	mA
Output Low Voltage	2 0V	100mA	4 75V			0 25	0 4	V
	2 0V	300mA	4 75V			0 5	0 7	V
Output Leakage Current	0 8V	30V	4 75V				100	μA
	0 8V	30V	0V				100	μA
Supply Currents								
Output Low	A_1 = 5V, B_1 = 0V		5 25V	Per Package		61	79	mA
Output High	$A_1 = B_1$ = 0V		5 25V	Per Package		13	17	mA
Input Clamp Diode Voltage	−12mA		5V	T_A = 25°C			−1 5	V
Propagation Delay Times The following Apply for V_{CC} = 5V, T_A = 25°C								
t_{pd1}, Input "0" to Output "1"			(Note 3)			13	25	ns
t_{pd1}, Input "1" to Output "0"			(Note 3)			19	25	ns
Output Risetime								ns
Output Falltime								ns

Note 1: All voltage values are with respect to ground Positive current is defined to be current into referenced pin.

Note 2: Maximum junction temperature is 150°C For operating at elevated temperatures, the package must be derated based on a thermal resistance, θ_{JA}, of 110°C/W.

Note 3: Delay is measured with a 50Ω load to 10V, 15pF load capacitance, measured from 1.5V input to 50% point on output. Unused inputs should be grounded for this test.

Note 4: Maximum voltage to be applied to either output in the off state

Interface Circuits

MH0007/MH0007C dc coupled MOS clock driver

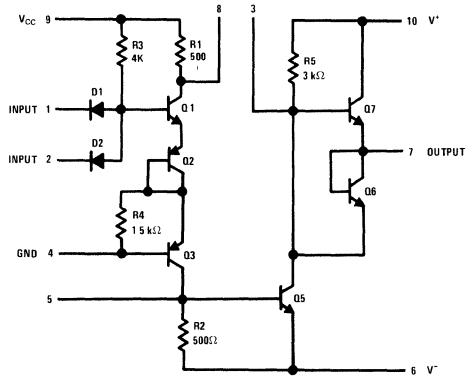
general description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

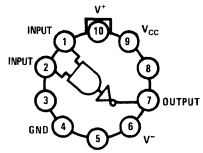
features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- High speed: 5 MHz with nominal load
- External trimming possible for increased performance

schematic and connection diagram



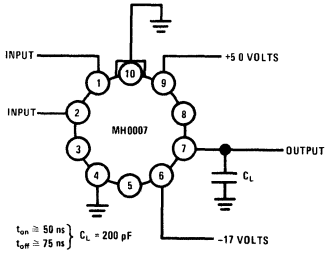
10 Pin TO-100 Package



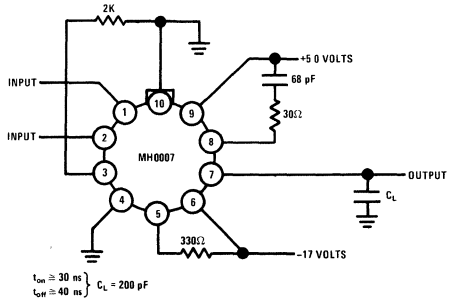
TOP VIEW

typical applications

Switching Time Test Configuration



High Speed Operation



absolute maximum ratings

V_{CC} Supply Voltage	8V
V^- Supply Voltage	-40V
V^+ Supply Voltage	+28V
($V^+ - V^-$) Voltage Differential	30V
Input Voltage	5.5V
Power Dissipation ($T_A = 25°C$)	800 mW
Peak Output Current	500 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range MH0007	-55°C to +125°C
MH0007C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

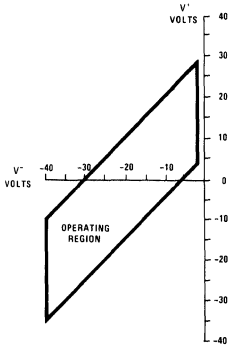
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	$V_{CC} = 4.5V$	2.2			V
Logical "0" Input Voltage	$V_{CC} = 4.5V$			0.8	V
Logical "1" Input Current	$V_{CC} = 5.5V$, $V_{IN} = 5.5V$			100	μA
Logical "0" Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$		1.0	1.5	mA
Logical "1" Output Voltage	$V_{CC} = 5.5V$, $I_{OUT} = 30$ mA, $V_{IN} = 0.8V$	$V^+ - 4.0$			V
	$V_{CC} = 5.5V$, $I_{OUT} = 1$ mA, $V_{IN} = 0.8V$	$V^+ - 2.0$			V
Logical "0" Output Voltage	$V_{CC} = 4.5V$, $I_{OUT} = 30$ mA, $V_{IN} = 2.2V$			$V^- + 2.0$	V
Transition Time to Logical "0" Output	$C_L = 200$ pF (Note 3)		50		ns
Transition Time to Logical "1" Output	$C_L = 200$ pF (Note 3)		75		ns

Note 1: Min/max limits apply across the guaranteed range of -55°C to +125°C for the MH0007, and from 0°C to +85°C for the MH0007C, for all allowable values of V^- and V^+

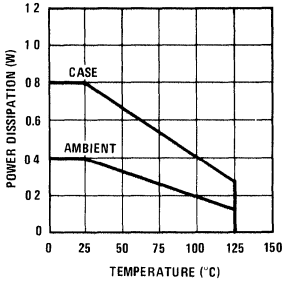
Note 2: All typical values measured at $T_A = 25°C$ with $V_{CC} = 5.0$ volts, $V^- = -25$ volts, $V^+ = 0$ volts.

Note 3: Transition time measured from time V_{IN} = 50% value until V_{OUT} has reached 80% of final value

Allowable Values for V^- and V^+



Maximum Power Dissipation



Interface Circuits

MH0009/MH0009C dc coupled two phase MOS clock driver

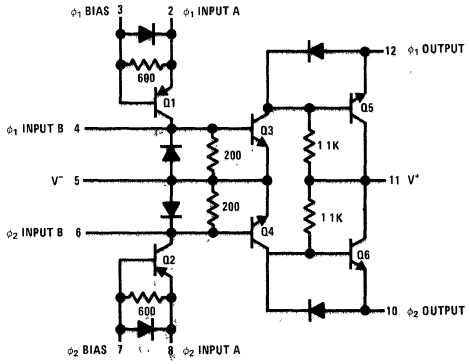
general description

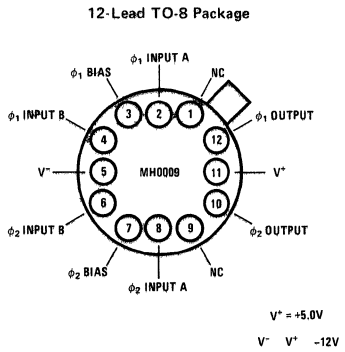
The MH0009/MH0009C is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM8830, DM7440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

features

- DC logically controlled operation
- Output Swings – to 30V
- Output Currents – in excess of ±500 nA
- High rep rate – in excess of 2 MHz
- Low standby power

schematic and connection diagrams





typical application

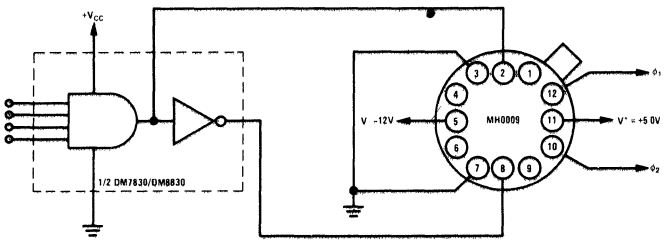


FIGURE 1

absolute maximum ratings

V^- Supply Voltage. Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	-40V
V^+ Supply Voltage: Differential (Pin 11 to Pin 5)	30V
Input Current: (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±500 mA
Power Dissipation (Note 2 and Figure 2)	1.5W
Storage Temperature	-65°C to +150°C
Operating Temperature: MH0009	-55°C to +125°C
MH0009C	0°C to 85°C
Lead Temperature (Soldering, 10 Sec.)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	C_{IN} = .0022 μF C_L = 001 μF		10	35	ns
t_{rise}	C_{IN} = 0022 μF C_L = 001 μF		40	50	ns
Pulse Width (50% to 50%)	C_{IN} = 0022 μF C_L = 001 μF	340	400	440	ns
t_{fall}	C_{IN} = 0022 μF C_L = 001 μF		80	120	ns
t_{delay}	C_{IN} = 600 pF C_L = 200 pF		10		ns
t_{rise}	C_{IN} = 600 pF C_L = 200 pF		15		ns
Pulse Width (50% to 50%)	C_{IN} = 600 pF C_L = 200 pF	40	70	120	ns
t_{fall}	C_{IN} = 600 pF C_L = 200 pF		40		ns

Note 1: Characteristics apply for circuit of Figure 1 With V^- = -20 volts, V^+ = 0 volts, V_{CC} = 5 0 volts Minimum and maximum limits apply from -55°C to +125°C for the MH0009 and from 0°C to +85°C for the MH0009C. Typical values are for T_A = 25°C

Note 2: Transient power is given by $P = fC_L (V^+ - V^-)^2$ watts, where f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing

Note 3: For typical performance data see the MH0013/MH0013C data sheet

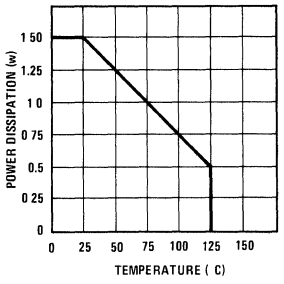


FIGURE 2. Maximum Power Dissipation

Interface Circuits

MH0012/MH0012C high speed MOS clock driver

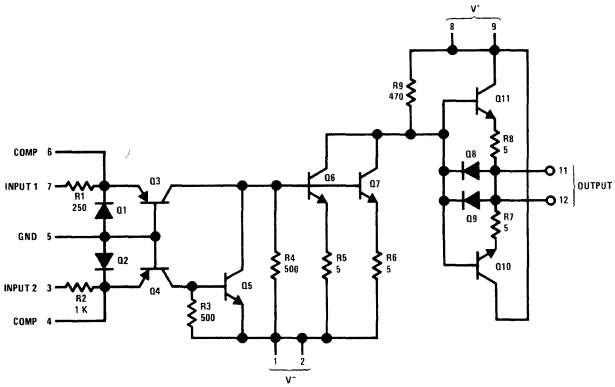
general description

The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

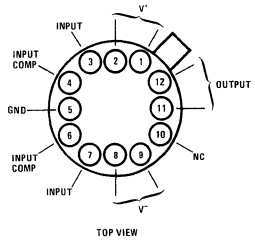
features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

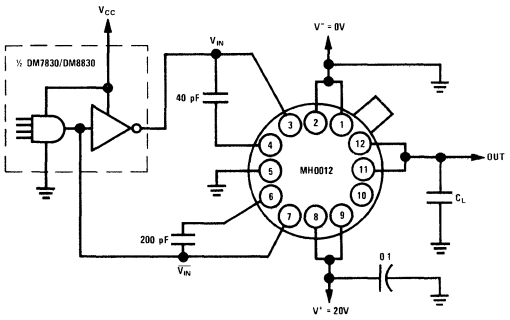
schematic and connection diagrams



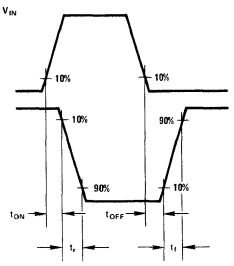
12-lead TO-8 Package



typical application (ac test circuit)



timing diagram



9

absolute maximum ratings

V^- Supply Voltage	Differential (Pin 1 or 2 to Pin 5)	-40V
V^+ Supply Voltage	Differential (Pin 8 or 9 to Pin 1 or 2)	30V
Input Current (Pin 3 or 7)		±75 mA
Peak Output Current		±1000 mA
Maximum Output Load–See Figure 2		
Power Dissipation–See Figure 1		1 5W
Storage Temperature		-65°C to +150°C
Operating Temperature	MH0012	-55°C to +125°C
	MH0012C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} < V^- + 2V$		1 0	2 0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} > V^+ - 1.5V$	0 4	0 6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2\ 0V$		V + 1 0	V^- + 2 0	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0\ 4V$	$V^+ - 1\ 5$	$V^+ - 0\ 7$		V
I_{DC} (V^- Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2\ 0V$		34	60	mA

ac electrical characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5\ 0V$ $C_L = 200$ pF, f = 1 0 MHz $T_A = 25°C$		10	15	ns
Rise Time (t_r)			5	10	ns
Turn-Off Delay (t_{OFF})			35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1 Min and max limits apply from -55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C Typical values are for $T_A = 25°C$

Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required

Note 3: All conditions apply for each parameter

Power Dissipation

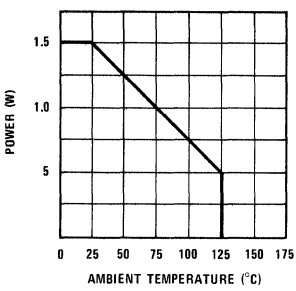


Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times

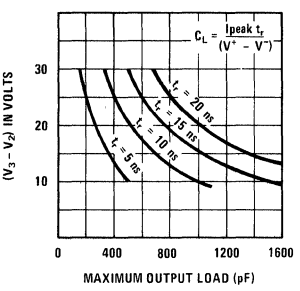
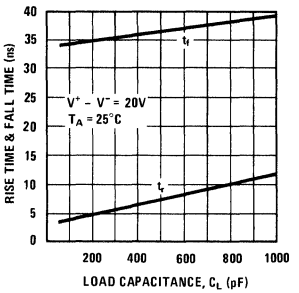


Figure 2.

Rise and Fall Times vs Load Capacitance



applications information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state The OFF power is neglible and will be ignored in the subsequent discussion The ON power is dissipated primarily by Q_3 and R_9 and is given by·

$$P_{ON} \cong [V^-|I_{IN} + \frac{(V^+ - V^-)^2}{R_9}] \ DC \qquad (1)$$

Where

$$DC = \text{Duty Cycle} = \frac{\text{ON Time}}{\text{ON Time \& OFF Time}}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9}\right] DC \qquad (2)$$

For $V_{IN} = 2\ 5V$, $V_{BE3} = 0\ 7V$, $V^+ = 0V$, $V^- = -20V$, and DC = 20%, $P_{ON} \cong 200$ mW

The transient power incurred during switching is given by

$$P_{AC} = (V^+ - V^-)^2\ C_L f \qquad (3)$$

For $V^+ = 0V$, $V^- = -20V$, $C_L = 200$ pF, and f = 5 0 MHz, $P_{AC} = 400$ mW

The total power is given by

$$P_T = P_{AC} + P_{ON} \qquad (4)$$

$$P_T \leq P_{MAX}$$

For the above example, $P_T = 600$ mW

Interface Circuits

MH0013/MH0013C two phase MOS clock driver

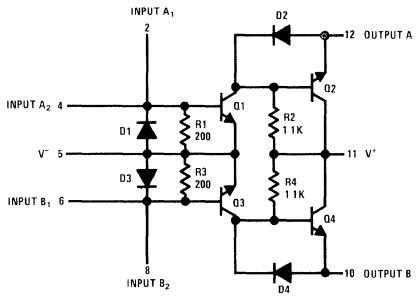
general description

The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

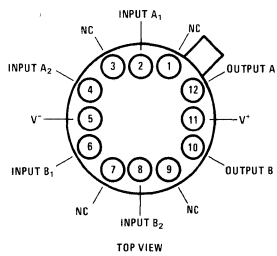
features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5 0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

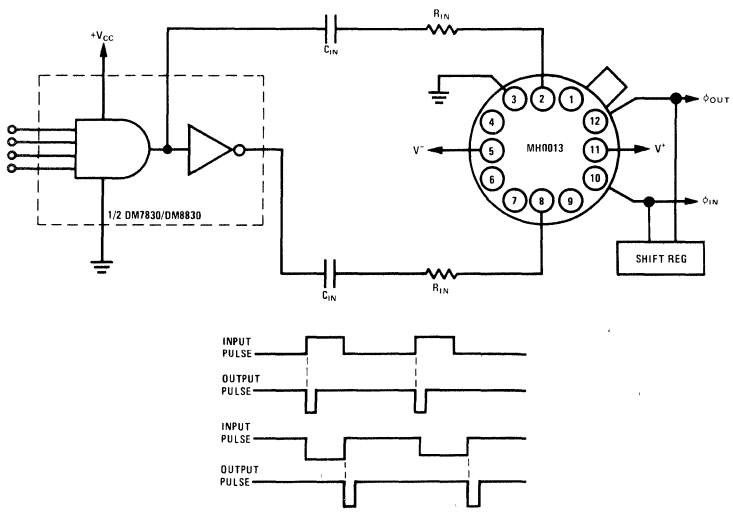
schematic and connection diagrams



12-Lead TO-8 Package



typical applications



absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±600 mA
Power Dissipation (Figure 7)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0013	−55°C to +125°C
MH0013C	0°C to +85°C
Lead Temperature (Soldering, 10 sec 1/16" from Case)	300°C

electrical characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^+ - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
					V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V		1.0	100	μA
	$I_{OUT} = I_{IN}$ = 0 mA				
Negative Input Voltage Clamp	I_{IN} = −10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}			35	50	ns
$t_{d\,OFF}$ (Note 2)	C_{IN} = 0.0022 μF		30	60	ns
t_{fall} (Note 2)	R_{IN} = 0Ω	40	50	80	ns
t_{fall} (Note 3)	C_L = 0.001 μF	40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/Max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with V^- = −20V and V^+ = 0V unless otherwise specified. Typical values are for 25°C

Note 2: Parameter values apply for clock pulse width determined by input pulse width

Note 3: Parameter values apply for input pulse width greater than output clock pulse width

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V_3 - V_2)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

circuit operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

typical performance characteristics

FIGURE 1. Output Load vs Voltage Swing

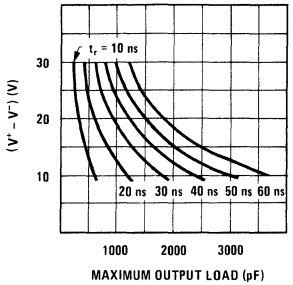


FIGURE 2. Transient Power vs Rep. Rate vs C_L

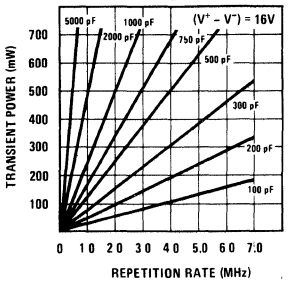


FIGURE 3. Transient Power vs Rep. Rate vs C_L

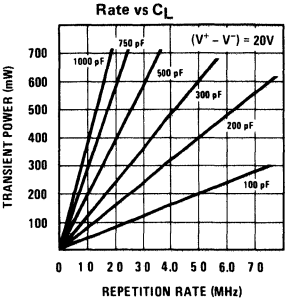


FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

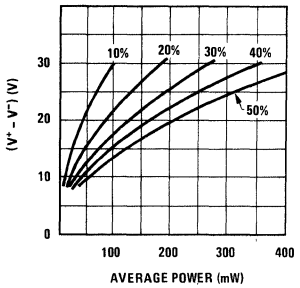


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

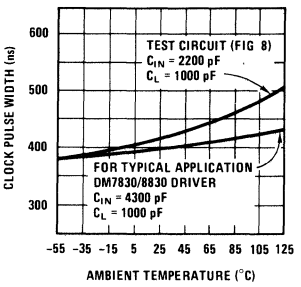


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

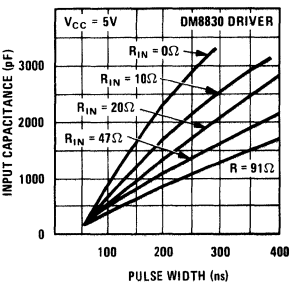
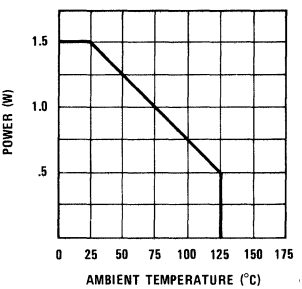
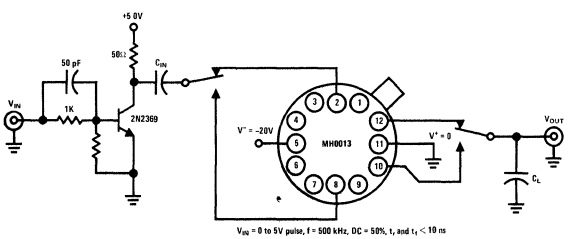


FIGURE 7. Package Power Derating



ac test circuit



timing diagram

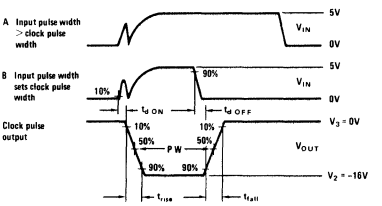


Figure 8

pulse width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall})$$

$$+ R_O C_{IN} \ln \frac{I_{IN}\ peak}{I_{IN}\ min} \cong 400 \text{ ns.}$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{d\,OFF} + t_{d\,ON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

fan-out calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times.

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of $(V^+ - V^-)$ versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3 *Input Power*

The average input power is a function of the input current and duty cycle Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25° C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width

4 *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70° C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink, therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW
+ transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved

Interface Circuits

MH0025/MH0025C two phase MOS clock driver

general description

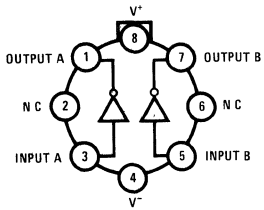
The MH0025/MH0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DM8830, or DM7440 Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1 5A
- Rep Rate 1 0 MHz into > 1000 pF
- Driven by DM932, DM8830, DM7440(SN7440)
- "Zero" Quiescent Power

connection diagrams

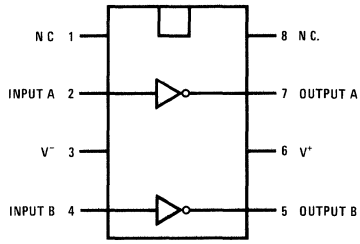
Metal Can Package



Note Pin 4 connected to case

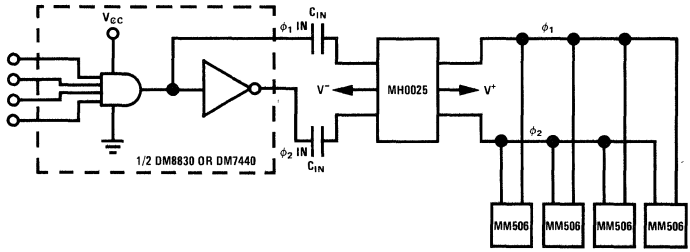
TOP VIEW

Dual-In-Line Package

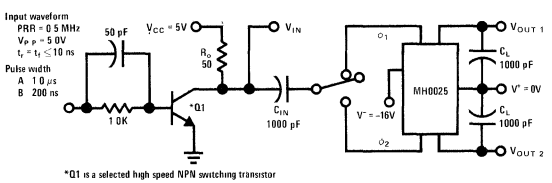


TOP VIEW

typical application

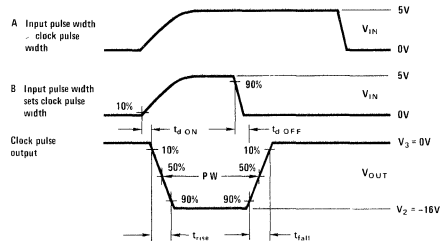


ac test circuit



*Q1 is a selected high speed NPN switching transistor

timing diagram



absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Power Dissipation	See Curves
Storage Temperature	−65°C to +150°C
Operating Temperature MH0025	−55°C to +125°C
MH0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1) See test circuit.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{d_{ON}}$			15	30	ns
T_{rise}	C_{IN} = .001 μF		25	50	ns
$T_{d_{OFF}}$ (Note 2)	R_{IN} = 0Ω		30	60	ns
T_{fall} (Note 2)	C_L = .001 μF	60	90	120	ns
T_{fall} (Note 3)		100	150	250	ns
P.W. (50% to 50%) (Note 3)			500		ns
Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA	$V^+ - 1.0$	$V^+ - 0.7V$		V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA		$V^- + 0.7V$	$V^- + 1.5V$	V

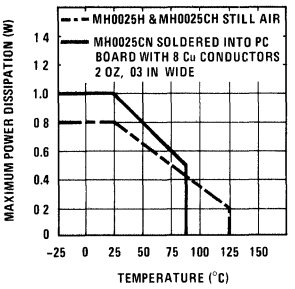
Note 1. Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for MH0025 and 0°C to 85°C for MH0025C. Typical values are for +25°C

Note 2. Parameter values apply for clock pulse width determined by input pulse width.

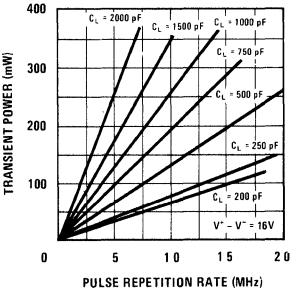
Note 3. Parameter values apply for input pulse width greater than output clock pulse width

typical performance

Package Power Derating

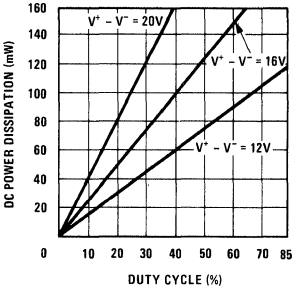


Transient Power vs Rep. Rate



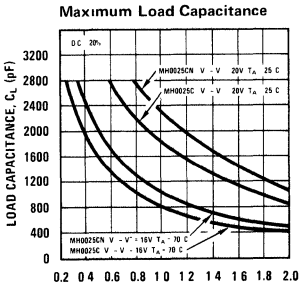
$P_{AC} = (V^+ - V^-)^2 f C_L$

DC Power (P_{DC}) vs Duty Cycle



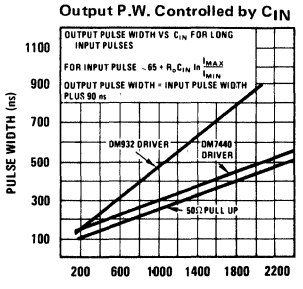
$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$

Maximum Load Capacitance



$$C_L \leq \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} \leq \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output P.W. Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$I_{MIN} \cong \frac{V_{BE}}{R_1} = \frac{0.6}{1k}$

applications information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents form V^- to V^+ cannot occur.

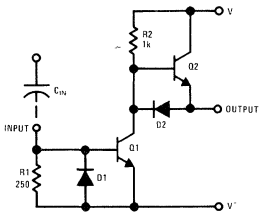


FIGURE 1. MH0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the MH0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition

Transient Current

The maximum peak output current of the MH0025 is given as 1.5A. Average transient current required from the driver can be calculated from

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

example calculation

How many MM506 shift registers can be driven by an MH0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the MH0025CN can dissipate 630 mW when soldered into printed circuit board

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one half of the MH0025C, 630 mW ÷ 2 can be dissipated.

315 mW = 50 mW + transient output power

265 mW = transient output power

Using equation (2) at 16V, 1 MHz and 250 mW, each half of the MH0025CN can drive a 975 pF load. This is, less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 975 pF would prevail

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{975}{80}$ or 12 registers.

9

Interface Circuits

MH0026/MH0026C 5 MHz two phase MOS clock driver

general description

The MH0026/MH0026C is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design along with advanced processing provide both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 series gates and flip-flops or from drivers such as the DM8830 or DM7440. The MH0026 is intended for applications in which the output pulse width is logically controlled· i.e., the output pulse width is equal to the input pulse width.

features

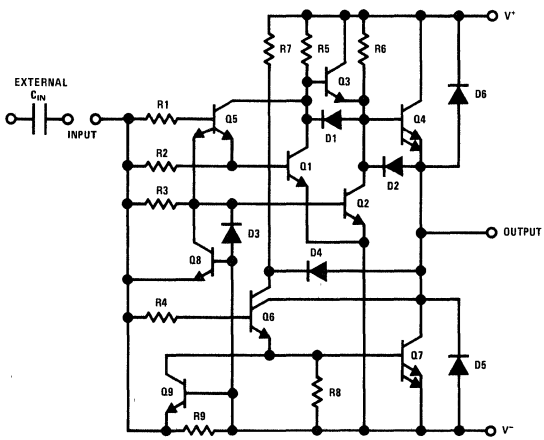
- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on load
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

The MH0026 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16 bit MM1103 RAM memory system. Information on the correct usage of the MH0026 in these as well as other systems is included in the application section starting on page 5. A thorough understanding of its usage will insure optimum performance of the device.

The device is available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt TO-8 packages.

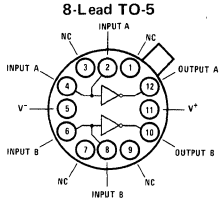
schematic diagram

(1/2 of Circuit Shown)



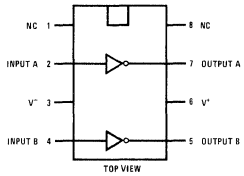
connection diagrams

8-Lead TO-5



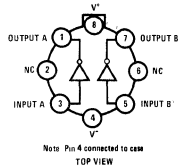
MH0026H/MH0026CH

8-Lead Dual-In-Line Package



MH0026CN

12-Lead TO-8



MH0026G/MH0026CG

absolute maximum ratings

$V^+ - V^-$ Differential Voltage		22V
Input Current		100 mA
Input Voltage ($V_{IN} - V^-$)		5.5V
Peak Output Current		1.5A
Power Dissipation		See curves
Operating Temperature Range	MH0026	−55°C to +125°C
	MH0026C	0°C to 85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Notes 1 & 2)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Logic "1" Input Voltage	$V_{OUT} = V^- + 1.0V$	2.5	1.5		V
Logic "1" Input Current	$V_{IN} - V^- = 2.5V$, $V_{OUT} = V^- + 1.0V$		10	15	mA
Logic "0" Input Voltage	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	V
Logic "0" Input Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$		-0.005	-10	μA
Logic "0" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -11.6$	4.0	4.3		V
Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$	$V^+ - 1.0$	$V^+ - 0.7$		V
Logic "1" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -9.5V$		-11.5	-11.0	V
Logic "1" Output Voltage	$V_{IN} - V^- = 2.5V$		$V^- + 0.5$	$V^- + 1.0$	V
"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.5V$		30	40	mA
"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$		10	100	μA

ac electrical characteristics (Notes 1 & 2, AC test circuit, $T_A = 25°C$)

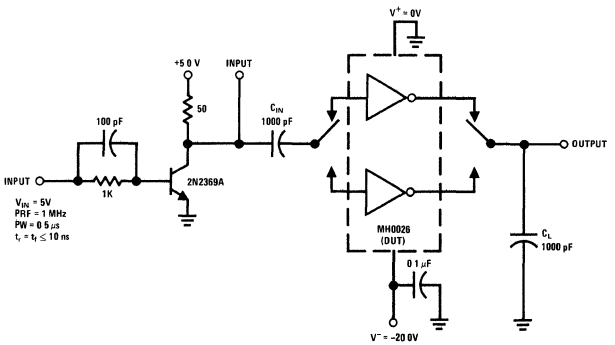
Turn-On Delay (t_{ON})		5.0	7.5	12	ns
Turn-Off Delay (t_{OFF})		5.0	12	15	ns
Rise time (t_r) — Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		12		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		15	18	ns
	$C_L = 1000$ pF		20	35	ns
Falltime (t_f) — Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		10		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		12	16	ns
	$C_L = 1000$ pF		17	25	ns

Note 1: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range −55°C to +125°C for the MH0026 and 0°C to +85°C for the MH0026C, unless otherwise specified.

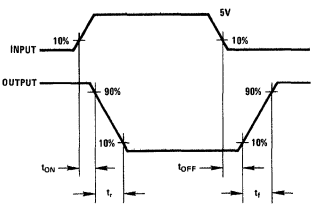
Note 2: All typical values for the $T_A = 25°C$

Note 3: Rise and fall time are given for MOS logic levels, i e , rise time is transistion from logic "0" to logic "1" which is voltage fall. See waveforms on the following pages.

ac test circuit

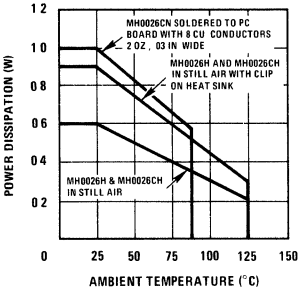


switching time waveforms

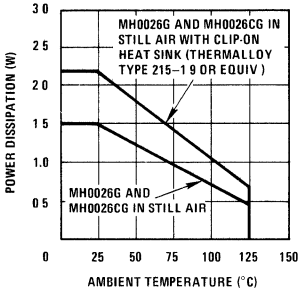


typical performance characteristics

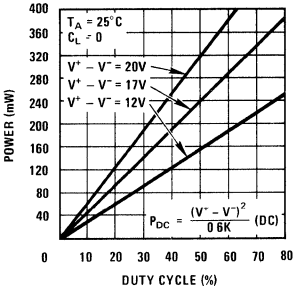
TO-5 & DIP Power Ratings



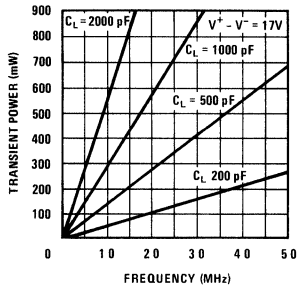
TO-8 Package Power Rating



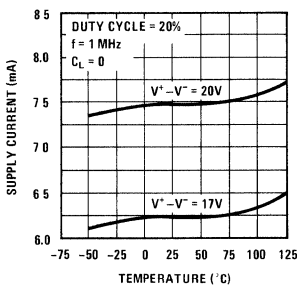
DC Power (P_{DC}) vs Duty Cycle



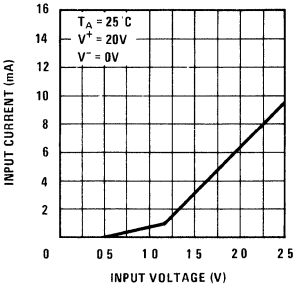
Transient Power (P_{AC}) vs Frequency



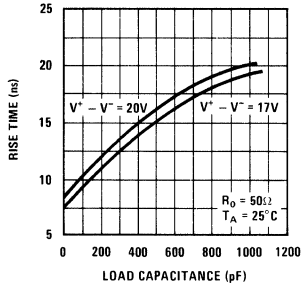
Supply Current vs Temperature



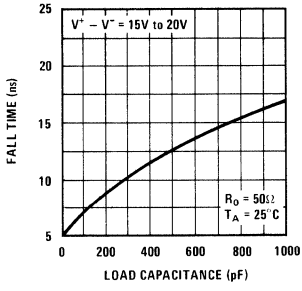
Input Current vs Input Voltage



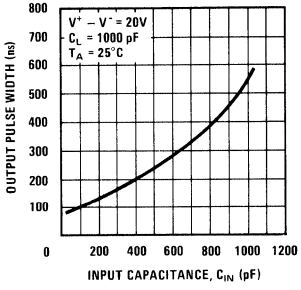
Rise Time vs Load Capacitance



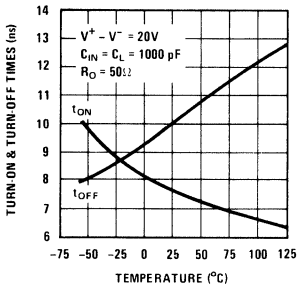
Fall Time vs Load Capacitance



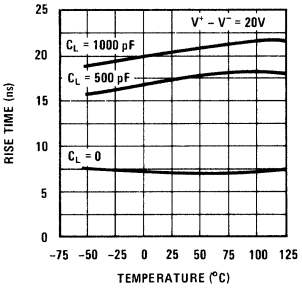
Optimum Input Capacitance vs Output Pulse Width



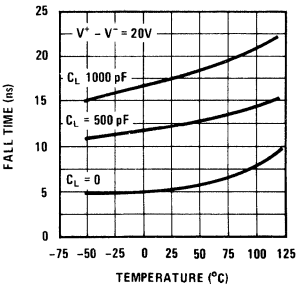
Turn-On & Turn-Off Time vs Temperature



Rise Time vs Temperature

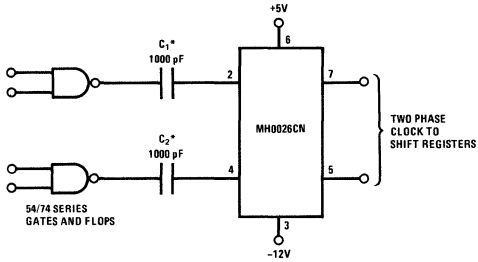


Fall Time vs Temperature



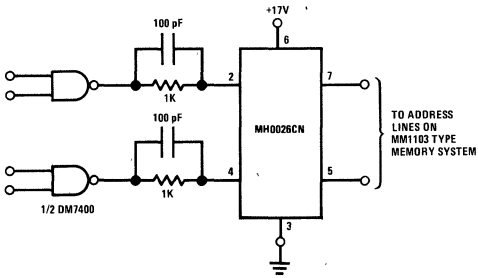
typical applications (cont.)

AC Coupled MOS Clock Driver

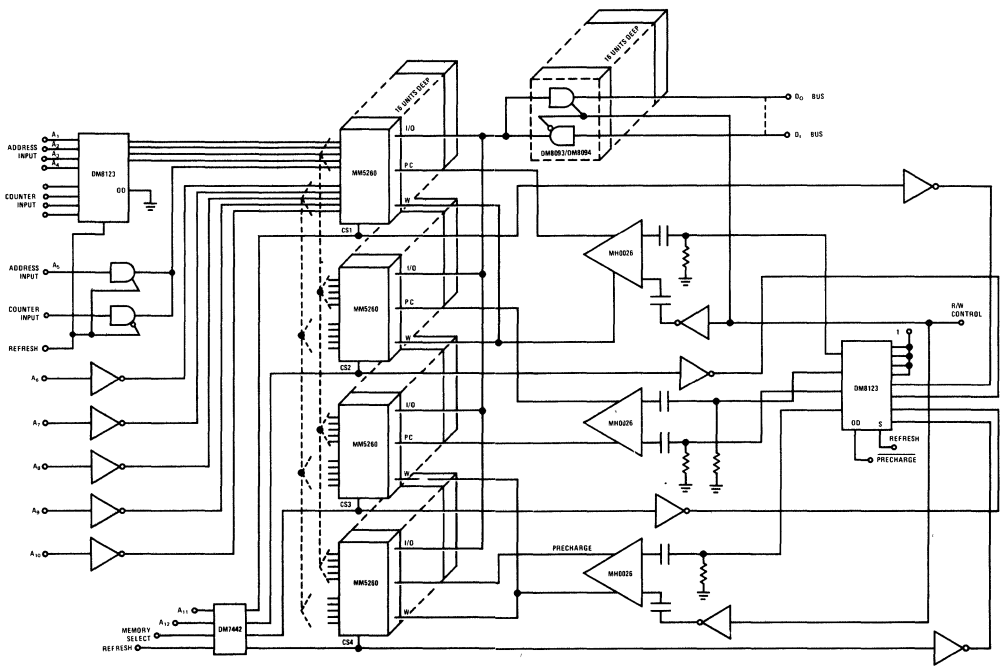


*See applications section on page 5 for detailed information on input/output design criterion

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

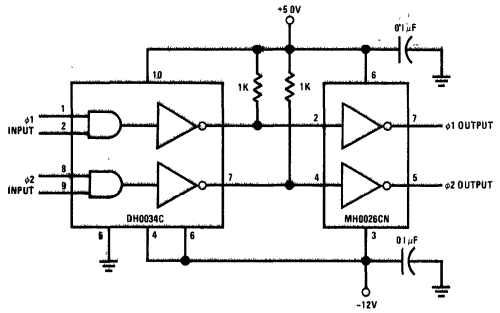


Precharge Driver for MOS RAM Memories

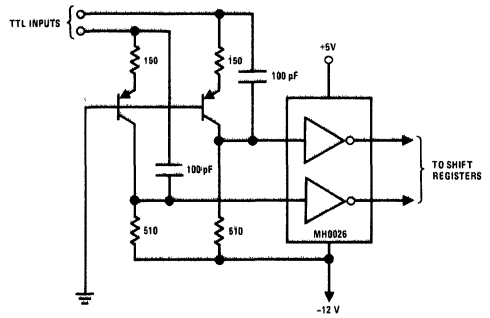


typical applications

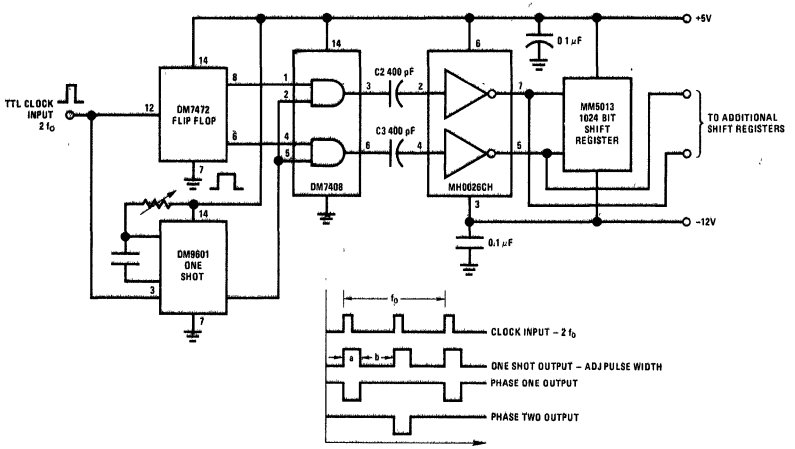
DC Coupled MOS Clock Driver



Transistor Coupled MOS Clock Driver



Logically Controlled AC Coupled Clock Driver



application information

1.0 Introduction

The MH0026 is capable of delivering 30 watts peak power (1.5 amps at 20V needed to rapidly charge large capacitative loads) while its package is limited to the watt range. This section describes the operation of the circuit and how to obtain optimum system performance. If additional design information is required, please contact your local National field application engineer.

2.0 Theory of Operation

Conventional MOS clock drivers like the MH0013 and similar devices have relied on the circuit configuration in Figure 1. The AC coupling of an input pulse allows the device to work over a wide range of supplies while the output pulse width may be controlled by the time constant $-R_1 \times C_1$.

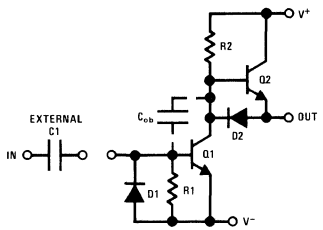


FIGURE 1. Conventional MOS Clock Drive

D_2 provides 0.7V of dead-zone thus preventing Q_1 and Q_2 from conducting at the same time. In order to drive large capacitive loads, Q_1 and Q_2 are large geometry devices but C_{ob} now limits useful output rise time. A high voltage TTL output stage (Figure 2) could be used; however, during switching until the stored charge is removed from Q_1, both output devices conduct at the same time. This is familiar in TTL with supply line glitches in the order of 60 to 100 mA. A clock driver built this way would introduce 1.5 amp spikes into the supply lines.

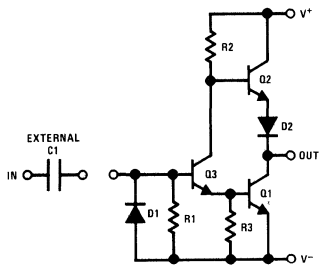


FIGURE 2. Alternate MOS Clock Drive

Unique circuit design and advanced semiconductor processing overcome these clasic problems allowing the high volume manufacture of a device, the MH0026, that delivers 1.5A peak output currents with 20ns rise and fall times into 1000pF loads. In a simplified diagram, D_1 (Figure 3) provides 0.7V dead zone so that Q_3 is turned ON for a rising input pulse and Q_2 OFF prior to Q_1 turning ON a few nanoseconds later. D_2 prevents zenering of the emitter-base junction of Q_2 and provides an initial discharge path for the load via Q_3 During a falling input, the stored charge in Q_3 is used beneficially to keep Q_3 ON thus preventing Q_2 from conducting until Q_1 is OFF. Q_1 stored charge is quickly discharged by means of common-base transistor Q_4.

The complete circuit of the MH0026 (see schematic on page 1) basically makes Darlingtons out of each of the transistors in Figure 3.

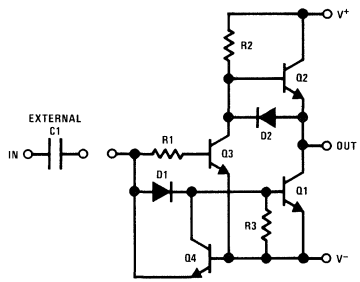


FIGURE 3. Simplified MH0026

When the output of the TTL input element (not shown) goes to the logic "1" state, current is supplied through C_{IN} to the base of Q_1 and Q_2 turning them ON, and Q_3 and Q_4 OFF when the input voltages reaches 0.7V. Initial discharge of the load as well as E-B protection for Q_3 and Q_4 are provided by D_1 and D_2. When the input voltage reaches about 1.5V, Q_6 and Q_7 begin to conduct and the load is rapidly discharged by Q_7. As the input goes low, the input side of C_{IN} goes negative with respect to V^- causing Q_8 and Q_9 to conduct momentarily to assure rapid turn-off of Q_2 and Q_7 respectively. When Q_1 and Q_2 turn OFF, Darlington connected Q_3 and Q_4 rapidly charge the load toward V^+ volts R_6 assures that the output will reach to within one V_{BE} of the V^+ supply

The real secret of the device's performance is proper selection of transistor geometries and resistor values so that Q_4 and Q_7 do not conduct at the same time while minimizing delay from input to output.

3.0 Power Dissipation Considerations

There are four considerations in determining power dissipations.

1. Average DC power
2. Average AC power
3. Package and heat sink selection
4. Remember—2 drivers per package

application information (cont.)

The total average power dissipated by the MH0026 is the sum of the DC power and AC transient power. The total must be less than given package power ratings.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Since the device dissipates only 2mW with output voltage high (MOS logic "0"), the dominating factor in average DC power is duty cycle or the percent of time in output voltage low state (MOS logic "1"). Percent of total power contributed by P_{DC} is usually neglible in shift register applications where duty cycle is less than 25%. P_{DC} dominates in RAM address line driver applications where duty cycle can exceed 50%.

3.1 DC Power (per driver)

DC Power is given by:

$$P_{DC} = (V^+ - V^-) \times (I_{S(Low)}) \times \left(\frac{\text{ON time}}{\text{OFF time}-\text{ON time}}\right)$$

or P_{DC} = (Output Low Power) X (Duty Cycle)

where: $I_{S(LOW)} = I_S$ @ $(V^+ - V^-)$

Example 1: ($V^+ = +5V$, $V^- = -12V$)

a) Duty cycle = 25%, therefore

$P_{DC} = 17V \times 40mA \times 17/20 \times 25\%$

P_{DC} = 145mW worst-case, each side

P_{DC} = 109mW typically

b) Duty cycle = 5%

P_{DC} = 21mW

c) See graph on page 3

The above illustrates that for shift register applications, the minimum clock width allowable for the given type of shift register should be used in order to drive the largest number of registers per clock driver.

Example 2: ($V^+ = +17V$, $V^- = GND$):

a) Duty cycle = 50%

P_{DC} = 290mW worst-case

P_{DC} = 218mW typically

b) Duty cycle = 100%

P_{DC} = 580mW

Thus for RAM address line applications, package type and heat sink technique will limit drive capability rather than AC power.

3.2 AC Transient Power (per driver)

AC Transient power is given by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L$$

where: f = frequency of operation

C_L = Load capacitance (including all strays and wiring)

Example 3: ($V^+ = +5V$, $V^- = -12V$)

$$P_{AC} = 17 \times 17 \times f(MHz) \times 10^6 \times C_L(nF) \times 10^{-9}$$

P_{AC} = 290mW per MHz per 1000pF

Thus at 5MHz, a 1000pF load will cause any driver to dissipate one and one half watts. For long shift registers, a driver with the highest package power rating will drive the largest number of bits for the lowest cost per bit.

3.3 Package Selection

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs on page 3 illustrate derating for various operating temperatures.

3.31 TO-5 ("H") Package: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving capability by 50%.

3.32 8-Pin ("N") Molded Mini-DIP: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0 watt soldered to PC board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

3.33 TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent–derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

application information (cont.)

3.4 Summary—Package Power Considerations

The maximum capacitative load that the MH0026 can drive is thus determined by package type, heat sink technique, ambient temperature, AC power (which is proportional to frequency and capacitive load) and DC power (which is principally determined by duty cycle). Combining equations previously given, the following formula is valid for any clock driver with negligible input power and negligible power in output high state:

$$C_L \text{ (max in pF)} = \frac{10^{-3}}{n} \times \frac{P_{max(mW)}(T_A, pkg) \times R_{eq} - (V^+ - V^-)^2 \times (Dc) \times 10^3}{(V^+ - V^-)^2 \times R_{eq} \times f(MHz)}$$

or:

$$C_L \text{ (max in pF)} = 5 \times 10^{-3} \times \frac{P_{max}(mW) \times 500 - V_S^2 \times Dc \times 10^3}{V_S^2 \times 500 \times f(MHz)}$$

Where: n = number of drivers per pkg. (2 for the MH0026)

$P_{max(mW)}(T_A,$ pkg) = Package power rating in milliwatts for given package, heat sink, and max, ambient temperature (See graphs)

R_{eq} = equivalent internal resistance

$R_{eq} = (V^+ - V^-)/I_{S(Low)} = 500$ ohms (worst case over temperature for the MH0026 or 660 ohms typically)

$V_S = (V^+ - V^-)$ = total supply voltage across device

Dc = Duty Cycle =

$$\frac{\text{Time in output low state}}{\text{Time in output low + Time in output high state}}$$

Table I illustrates MH0026 drive capability under various system conditions.

4.0 Pulse Width Control

The MH0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + \frac{t_r + t_f}{2} = PW_{IN} + 25ns$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the MH0026 discharges to just above the devices threshold (about 1.5V). If the input is allowed to discharge below the threshold, t_{OFF} and t_f will be degraded. The graph on page 3 shows optimum values for C_{IN} vs desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\,(PW)_{OUT}$$

For an output pulse width of 500ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})(500 \times 10^{-9}) \cong 1000pF$$

TABLE 1. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max Operating Frequency	Max. Ambient Temp. ↓ / → Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2 7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2 2k	1.8k	1.4k	1 1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

***Note** Values in pF and assume both sides in use as non-overlaping 2 phase driver, each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$ For loads greater than 1200 pF, rise and fall times will be limited by output current, see Section 5 0

9

application information (cont.)

5.0 Rise & Fall Time Considerations(Note 3)

The MH0026's peak output current is limited to 1.5A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)(250 \times 10^{-12} + C_L)$$

Where: ΔV = The change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

For $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20V)(250 \times 10^{-12} + 10^{-12})$$
$$= 25ns$$

For small values of C_L, equation above predicts optimistic values for t_r. The graph on page 3 shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2R\left(C_S + \frac{C_L}{h_{FE} + 1}\right)$$

6.0 Clock Overshoot

The output waveform of the MH0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the ouput of the MH0026. The critical valve for $R_s = 2\sqrt{L/C\ell}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_s is readily determined empirically, and values typically range between 10 and 51 ohms. R_s does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2R_S C_L$$

7.0 Clock Line Cross Talk

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the MH0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least 2 V_{BE} before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the MH0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10k ohms.

8.0 Power Supply Decoupling

Power supply decoupling is a widespread and accepted practice. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each MH0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

MH0027C dual high speed MOS interface driver

general description

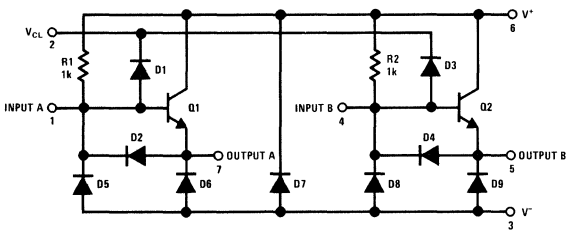
The MH0027C is a dual high current active pull-up designed to operate with a high current sink such as the DH0034 or LM7541A and thus provides fully TTL compatible DC coupled inputs The partitioning of current sinks and sources into separate packages provides higher overall power drive capability while minimizing system cost. The device is intended for use as a driver for MOS RAM memories such as the MM1103. The MH0027C is capable of sourcing over 1 ampere peak current with a rise-time of 25 ns into 600 pF loads.

features

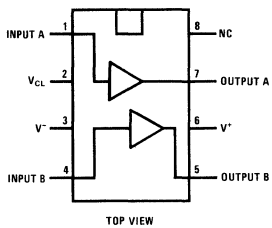
- Fast rise times – 25 ns into 600 pF load
- Peak output current in excess of 1 ampere
- Fully compatible with DH0034 dual level shifter and LM75450 series peripheral drivers.
- Wide operating supply range – 5V to 25V
- Output voltage clamp
- Low power dissipation – 1 mW typical in logic "1" state

The MH0027C operates over an ambient temperature range of 0°C to +85°C and is supplied in a miniature 8-pin molded dual-in-line package.

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Continuous Supply Voltage	25V
Peak Supply Voltage (10 ms)	30V
Input Voltage	25V
Output Voltage	V_{CC}
Peak Output Current (each side)	1.2A
Power Dissipation (Note 1)	1.0W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (T_A = +25°C, V^+ = 24V, V_{CL} = 21V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Low Level Input Current (I_{IL})	V_{IN} = 0V	18	25	32	mA
High Level Output Voltage (V_{OH})	I_{OH} = 4 mA	20 75	21 0	21.25	V
Low Level Output Voltage (V_{OL})	I_{OL} = 100 mA		0 7	1.0	V
Turn-On Time (t_{dON})	C_L = 600 pF		5	15	ns
Turn-Off Time (t_{dOFF})	C_L = 600 pF		5	15	ns
Rise Time (t_r)	C_L = 600 pF		20	45	ns
Fall Time (t_f)	C_L = 600 pF		15	35	ns

Note 1: Rating applies for device soldered to a printed circuit board with 8 copper conductors 03 inches wide For ambient temperatures above 25°C, derate linearly at 6 7 mW/°C

For specifications on other National MOS clock drivers and interface circuits, see the following data sheets:

MOS Clock Drivers

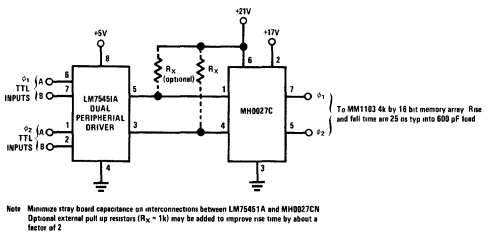
Single Phase, TTL Input DC Coupled – MH0007
Two Phase DC Coupled – MH0009
Single Phase, High Speed DC Coupled – MH0012
Two Phase AC Coupled – MH0013
Two Phase Low Cost – MH0025
Two Phase High Speed AC Coupled – MH0026

MOS Interface Circuits

Dual Voltage Translator – DM7800/DM8800
Dual High Speed Translator – DH0034/DH0034C
Quad 2-Input NAND TTL/MOS Interface – DM8810,DM8811
Quad 2-Input AND TTL/MOS Interface – DM8810
Hex Inverter TTL/MOS Interface – DM8812
Dual Peripheral Drivers – LM350,LM351/LM75450A,LM75451A
Analog Comparator to MOS – LM111 series
Dual Analog Comparator to MOS – LH2111 series

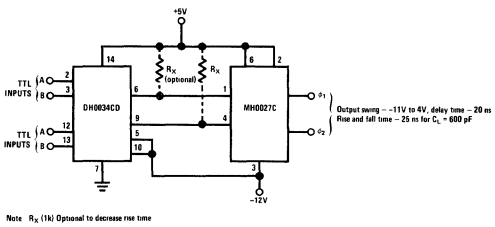
typical applications

TTL to MM1103 High Speed Memory Interface



Note: Minimize stray board capacitance on interconnections between LM75451A and MH0027CN Optional external pull up resistors (R_X = 1k) may be added to improve rise time by about a factor of 2

TTL to Negative Level Interface (DC Coupled MOS Clock)



Note: R_X (1k) Optional to decrease rise time

Interface Circuits

MH8808 dual high speed MOS clock driver

general description

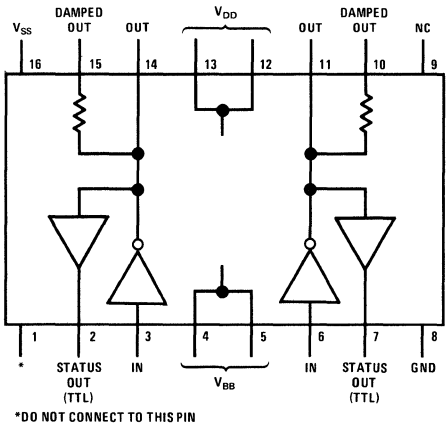
The MH8808 is a high speed dual MOS clock driver intended to drive the two phases of a memory array of 500 pF per phase at rates up to 4 MHz. The design includes output current limiting for controlled rise and fall times, and thermal shutdown which protects the chip against excessive power dissipation or accidental output shorts Two DTL/TTL compatible status outputs monitor clock outputs and provide a corresponding TTL logic level for status indication. Both direct and internally damped outputs are available for each phase to suit the particular application. It is ideally suited for driving MM5262 2k RAMs.

features

- High Speed 18 ns typ delay and 20 ns typ rise and fall times with 500 pF load
- Current limited outputs ±450 mA typ
- Direct and damped outputs available
- Thermal shutdown protection
- TTL compatible status outputs
- 1W dissipation capability at 25°C T_A
- 16 pin cavity dual-in-line package
- Output high level clamped to +5V

connection diagram

Dual-In-Line Package



*DO NOT CONNECT TO THIS PIN

TOP VIEW

absolute maximum ratings

V_{SS}	+7V
$V_{BB} - V_{DD}$	26V
Total Power Dissipation (Note 1)	1W
Operating Temperature Range	0°C to +70°C

electrical characteristics

The following apply for V_{BB} = +7V, V_{SS} = +5V, V_{DD} = −15V, T_A = 25°C unless otherwise stated

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Input Current	V_{IN} = −9V (Note 2)		10	mA
Output Low Voltage	I_{OUT} = +1 mA, V_{IN} = −10V (Note 2)	−14		V
Output High Voltage	I_{OUT} = −1 mA, V_{IN} = −14V	4 5	5 3	V
Status "1" Voltage	I_{OUT} = −250 μA, V_{IN} = −14V	3		V
Status "0" Voltage	I_{OUT} = 20 mA, V_{IN} = −10V (Note 2)		0 5	V
Output Leakage Current	V_{BB} = +8 5V, V_{SS} = 5V V_{DD} = −17 5V, V_{OUT} = +8 5V V_{IN} = open		100	μA
Damping Resistor		4		Ω
I_{BB}	V_{IN} = −11 5V V_{SS} = +6 5V, V_{DD} = −17 5V V_{BB} = +8 5V (Note 2)		32	mA
I_{SS}	V_{IN} = −11 5V V_{SS} = +6 5V, V_{DD} = −17 5V V_{BB} = +8 5V (Note 2)		23	mA
I_{DD}	V_{IN} = −11 5V V_{SS} = +6 5V, V_{DD} = −17 5V V_{BB} = +8 5V (Note 2)		−55	mA
Output Rise Time	C_L = 500 pF		26	ns
Output Fall Time	C_L = 500 pF		26	ns
Delay to Negative-Going Output	C_L = 500 pF	7	22	ns
Delay to Positive-Going Output	C_L = 500 pF	10	25	ns

Note 1 Maximum junction temperature is 110°C For operation above 25°C derate at 85°C/W θ_{JA} for still air

Note 2 Test only one input high (more positive) at a time

New Products

DM5485/DM7485(SN5485/SN7485)
4-bit magnitude comparator

general description

The DM5485/DM7485 performs magnitude comparison of straight binary and BCD (8421) codes. Three fully decoded decisions on two 4-bit words (A & B) are made and brought to three outputs.

This device is fully expandable by use of cascading inputs. When expanded the total comparison time is a function of word length and is two gate delays (≈ 12 ns) for each four bit section added to the basic device delay.

features

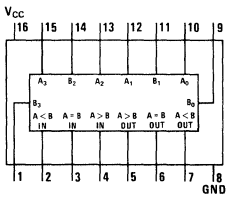
- Greater than, less than and equal to in one package
- Easily expandable through high speed cascading inputs
- Typical power 275 mW

truth table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

connection diagram



DM5491A/DM7491A(SN5491/SN7491) 8-bit shift register

general description

The DM5491A/DM7491A is a serial-in, serial-out, 8-bit shift register utilizing TTL technology. It is composed of eight RS master/slave flip flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1.0V. Power dissipation is typically 175 mW; a full fan out of 10 is available from the outputs.

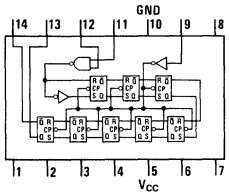
Data and input control are gated through inputs A and B to the first bit of the shift register. Drive for the common clock line is provided by an internal clock buffer. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

features

- High speed 18 MHz typ.
- Gated data input
- Both true and complement outputs of last bit
- Input loading of 1 on each input
- Typical power 175 mW

connection diagram



DM54123/DM74123(SN54123/SN74123) TTL/monostable multivibrator

general description

The DM54123/DM74123 is a dual retriggerable, resettable monostable multivibrator providing an output pulse whose duration and accuracy is a function of external timing components. Its inputs and outputs are standard TTL and compatible with all 5400 and 7400 products.

There are two inputs per function, one active LOW and one active HIGH. This permits triggering on either the leading (positive going) or trailing (negative going) edge. Triggering is independent of input transition time or pulse width. An input cycle time shorter than the output R*C cycle time will retrigger the DM54123 and result in a continuous output.

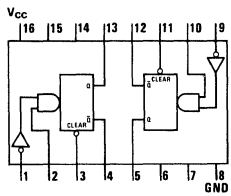
Retriggering may be inhibited by tying the $\overline{Q}$ output to the active LOW trigger input or the Q output to the active HIGH input.

The true output may be forced LOW during any phase of input or output timing by connecting a logic LOW level to the reset input.

features

- Retriggerable 0% to 100% duty cycle
- TTL compatible inputs and outputs
- Triggers on leading or trailing edge
- Complementary outputs
- Compensated for temperature and power supply variations
- High speed trigger to Q 21 ns (typ.)

connection diagram



DM54141/DM74141 (SN54141/SN74141) BCD to decimal decoder/driver

general description

The DM54141/DM74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

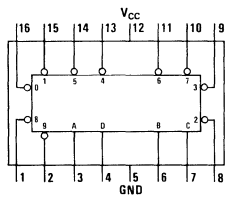
Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance NPN output transistors have a maximum reverse current of 50μA at 55V.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 mW, which is about one-half the power requirement of earlier designs.

features

- Drives cold cathode numeric indicator tubes directly
- Low leakage current at 55V (50μA max.)
- Low power dissipation of 55 mW (typ.)
- Fully decoded inputs ensure all outputs off for invalid codes
- Input clamp diodes for minimizing transmission line effects

connection diagram



DM54160/DM74160 (SN54160/SN74160), DM54161/DM74161 (SN54161/SN74161), DM54162/DM74162 (SN54162/SN74162), DM54163/DM74163 (SN54163/SN74163), synchronous 4-bit counter

general description

These synchronous, presettable counters feature an internal carry-look-ahead for applications in totally synchronous high speed counting schemes. The DM54160/DM74160 and DM54162/DM74162 are BCD decade counters and the DM54161/DM74161 and DM54163/DM74163 are 4-bit binary counters. All counting flip flops are triggered simultaneously from a common clock buffer, counting on the rising (positive going) edge of the clock input waveform.

All counters are synchronously presettable to either state. With a Low logic level on the Load input, the next rising edge of the clock will transfer into the counting register data present on the inputs A, B, C, and D.

The Clear functions for the DM54160/DM74160 and DM54161/DM74161 are asynchronous and a Low logic level on the Clear inputs will set all outputs Low regardless of the state of the clock or any other input (i.e., clear overrides all other functions).

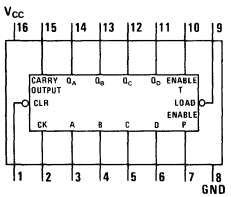
The Clear function for the DM54162/DM74162 and DM54163/DM74163 are totally synchronous. A Low logic level on the Clear input will set the outputs Low *after* the next clock pulse. This synchronous clear allows simplified count sequences as the maximum count can be decoded with one extra NAND gate. This gate then synchronously sets the counter to 0000 (all Low).

The internal carry-look-ahead provides for cascading up to 10 counters in totally synchronous applications without additional gating.

features

- Internal look-ahead for fast counting
- Terminal count output for ripple cascading
- Synchronous counting
- Synchronous loading
- Typical count frequencies over 32 MHz
- DM54160/DM74160 equal to FSC 9310
- DM54161/DM74161 equal to FSC 9316

connection diagram



10

DM54174/DM74174(SN54174/SN74174) hex D flip flop
DM54175/DM74175(SN54175/SN74175) quad D flip flop

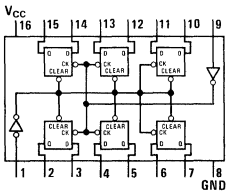
general description

Both devices contain positive edge-triggered D-type flip flops. Q outputs only appear on the DM54174/DM74174 whereas both Q and $\overline{Q}$ outputs are available on the DM54175/DM74175. Overriding Clear inputs are used to set the Q outputs to the logic "0" state.

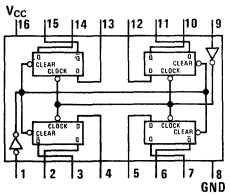
features

- Buffered clock and direct clear inputs
- Individual data input to each flip flop

connection diagrams



DM54174/DM74174



DM54175/DM74175

truth table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

*Available on the DM54175/DM74175
X = Don't care
↑ = Transition from low to high

DM54196/DM74196(SN54196/SN74196) presettable decade counter
DM54197/DM74197(SN54197/SN74197) presettable binary counter

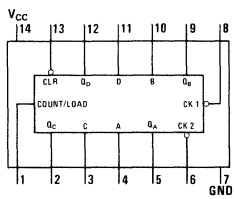
general description

These high-speed counters consist of four M/S flip flops which are internally connected to provide either a divide-by-two and a divide-by-five counter (DM54196/DM74196); or a divide-by-two and a divide-by-eight counter (DM54197/DM74197). The outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs, independent of the state of the clocks.

features

- Performs BCB, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Guaranteed to count at input frequencies from 0 to 50 MHz
- Input clamping diodes simplify system design
- Output Q_A will drive clock-2 input plus ten series 54/74 loads

connection diagram



truth tables

DM54196/DM74196 DECADE

(BCD) (See Note 1)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY

(5-2) (See Note 2)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

DM54197/DM74197
(See Note 1)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Note 1. Output Q_A connected to CLOCK-2 input
Note 2. Output Q_D connected to CLOCK-1 input

DM7512/DM8512 dual gated master/slave JK/D flip flop

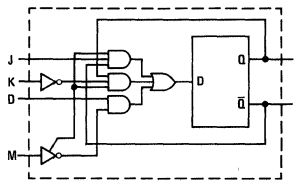
general description

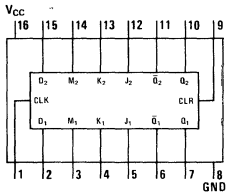
The DM7512/DM8512 is a dual flip flop which can operate in either a J, K mode or in a D-type mode. Both flip flops operate from a common clock and a common asynchronous clear but have separate mode inputs so that one can operate as a J, K flip flop while the other is operating as a D-type flip flop. (See truth table.)

features

- Positive-edge-triggered
- High speed, 40 MHz typical operation
- DM75L12/DM85L12 pin compatible
- Target power dissipation 270 mW max.

logic and connection diagrams





truth table

J	K	M	CLR	Q_{N+1}
0	0	1	0	Q_N
1	0	1	0	1
0	1	1	0	0
1	1	1	0	$\overline{Q}_N$
X	X	0	0	D
X	X	X	1	0*

*Asynchronous transition
X = Don't care

DM7555/DM8555 TRI-STATE®programmable decade counter

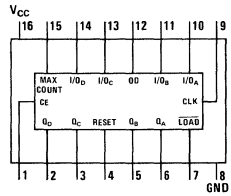
general description

The DM7555/DM8555 is a TRI-STATE four-bit decade counter which has both conventional and TRI-STATE outputs. When the TRI-STATE outputs are in the high-impedance mode, they can be used to load information into the subsequent stage. This is particularly useful in applications involving program counters. Fully synchronous operation results when these devices are cascaded.

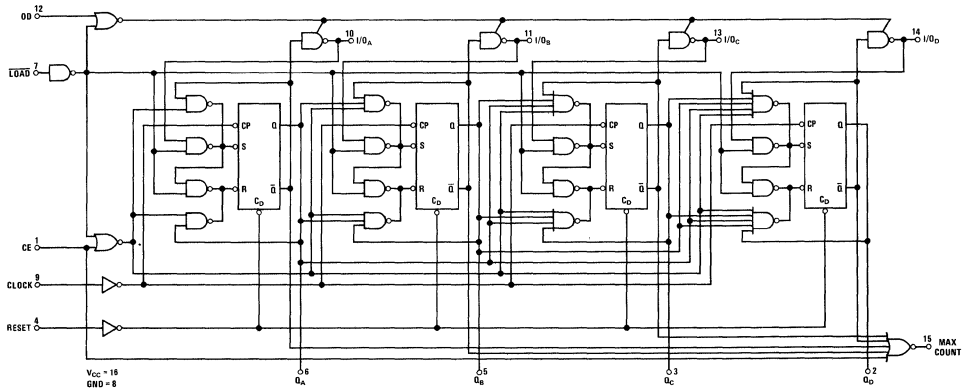
features

- Typical power dissipation 375 mW
- Target propagation delay 27 ns
- Target clock frequency 50 MHz

connection diagram



logic diagram



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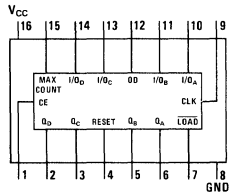
DM7556/DM8556 TRI-STATE®programmable binary counter

general description

The DM7556/DM8556 is a TRI-STATE four-bit binary counter which has both conventional and TRI-STATE outputs. When the TRI-STATE outputs are in the high-impedance mode they can be used to load information into the subsequent stage. This is particularly useful in applications involving program counters. Fully synchronous operation results when these devices are cascaded.

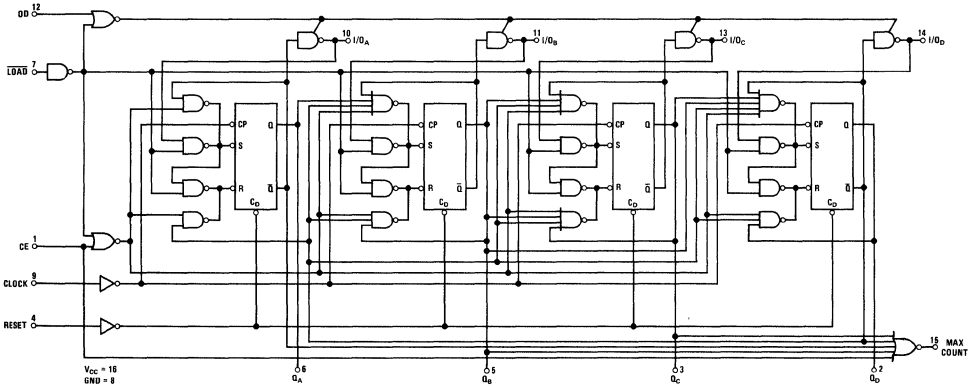
connection diagram



features

- Typical power dissipation 375 mW
- Target propagation delay 27 ns
- Target clock frequency 50 MHz

logic diagram



DM7613/DM8613 quad gated D flip flop

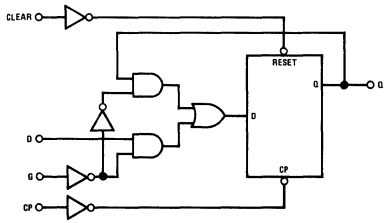
general description

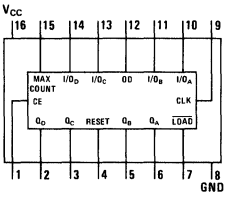
DM7613/DM8613 is a positive-edge-triggered quad gated D flip flop with direct clear and gated inputs. The gate, if set to a logical "1" level, will inhibit data entry from the data input.

features

- Positive-edge-triggered, buffered clock
- Target power dissipation 380 mW max.
- Target propagation delay 42 ns max.
- Target clock rate 20 MHz min.

logic and connection diagrams





truth table

D	G	CLR	Q_{N+1}
1	0	0	1
0	0	0	0
X	1	0	Q_N
X	X	1	0*

X = Don't care
*Asynchronous transition

DM7833/DM8833, DM7834/DM8834, DM7835/DM8835, DM7839/DM8839 quad TRI-STATE® transceivers

general description

This family of TRI-STATE® party line transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DM7833/DM8833 and DM7835/DM8835 employ TRI-STATE outputs on the receiver also, while on the DM7834/DM8834 and DM7839/DM8839 the receiver outputs are standard active pull up T²L.

The DM7833/DM8833 are non-inverting quad transceivers with a common driver disable control and a common receiver disable control.

The DM7839/DM8839 are non-inverting quad transceivers with a common two-input driver disable control.

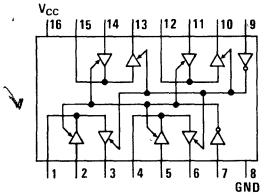
The DM7834/DM8834 are inverting quad transceivers with a common two input driver disable control.

The DM7835/DM8835 are inverting quad transceivers with a common driver disable control and a common receiver disable control.

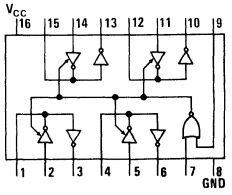
features

- Receiver hysteresis 450 mV (typ)
- Receiver noise immunity 1.4V (typ)
- Receiver input current for normal V_{CC} or V_{CC} = 0V 50 μA (max)
- Receivers
  - Sink 16 mA at 0.4V (max)
  - Source 2.0 mA (mil), 5.2 mA (com) at 2.4V (min)
- Drivers
  - Sink 50 mA at 0.5V (max) or 32 mA at 0.4V (max)
  - Source 10.4 mA at 2.4V (min)
- Drivers have TRI-STATE outputs
- DM7833/DM8833 and DM7835/DM8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω DC terminated buses
- 74 series TTL compatible

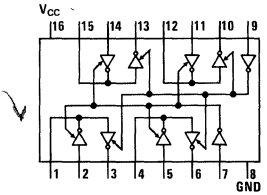
connection diagrams



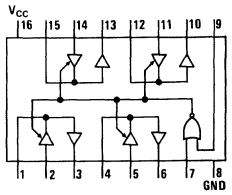
DM7833/DM8833



DM7834/DM8834



DM7835/DM8835



DM7839/DM8839

DM9602/DM8602 dual TTL/monostable multivibrator

general description

The DM9602/DM8602 is a dual retriggerable, resettable monostable multivibrator providing an output pulse whose duration and accuracy is a function of external timing components. Its inputs and outputs are standard TTL and compatible with all 7400, 74H and 74S families.

There are two inputs per function, one active Low and one active High. This permits triggering on either the leading (positive going) or trailing (negative going) edge. Triggering is independent of input transition time or pulse width. An input cycle time shorter than the output R*C cycle time will retrigger the DM9602 and result in a continuous output.

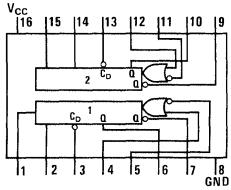
Retriggering may be inhibited by tying the $\overline{Q}$ output to the active Low trigger input or the Q output to the active High input.

The true output may be forced Low during any phase of input or output timing by connecting a logic Low level to the reset input.

features

- Resettable and retriggerable — 0% to 100% duty cycle
- TTL compatible inputs and outputs
- Triggers on leading or trailing edge
- Complementary outputs
- Compensated for temperature and power supply variations

connection diagram



DM54L89A/DM74L89A 64-bit random access memory

general description

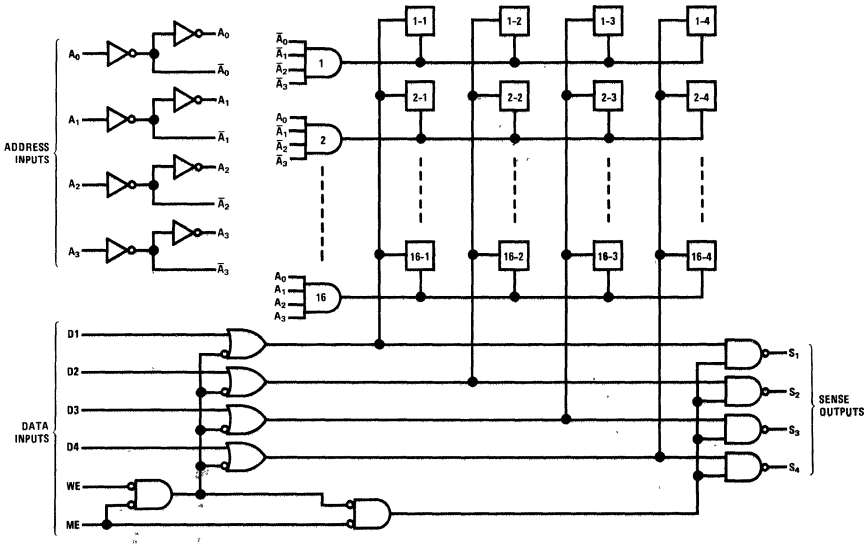
The DM54L89A/DM74L89A is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

The "A" suffix is used to denote that full "tenth-power" technology has been employed in building this RAM.

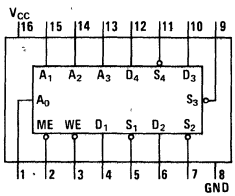
features

- Series 54L/74L compatible
- Organized as 16 4-bit words
- Typical access from chip enable 50 ns
- Typical power dissipation 55 mW
- Open collector outputs to permit "wire OR" capability
- Pin compatible with SN5489/7489, 3101, 5501

logic diagram



connection diagram



truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

DM54L123/DM74L123(SN54L123/SN74L123)
dual TTL/monostable multivibrator

general description

The DM54L123 is a low power dual retriggerable, resettable monostable multivibrator providing an output pulse whose duration and accuracy is a function of external timing components. Its inputs and outputs are compatible with all 54L and 74L products.

There are two inputs per function, one active LOW and one active HIGH. This permits triggering on either the leading (positive going) or trailing (negative going) edge. Triggering is independent of input transition time or pulse width. An input cycle time shorter than the output R*C cycle time will retrigger the DM54L123 and result in a continuous output.

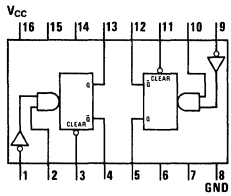
Retriggering may be inhibited by tying the $\overline{Q}$ output to the active LOW trigger input or the Q output to the active HIGH input.

The true output may be forced LOW during any phase of input or output timing by connecting a logic LOW level to the reset input.

features

- Low power 25 mW
- Resettable and retriggerable 0% to 100% duty cycle
- Low power TTL compatible inputs and outputs
- Triggers on leading or trailing edge
- Complementary outputs
- Compensated for temperature power supply variations
- High speed, trigger to Q 50 ns (typ)

connection diagram



DM54L187A/DM74L187A 1024-bit read only memory

general description

The DM54L187A/DM74L187A is a custom-programmed read-only-memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs.

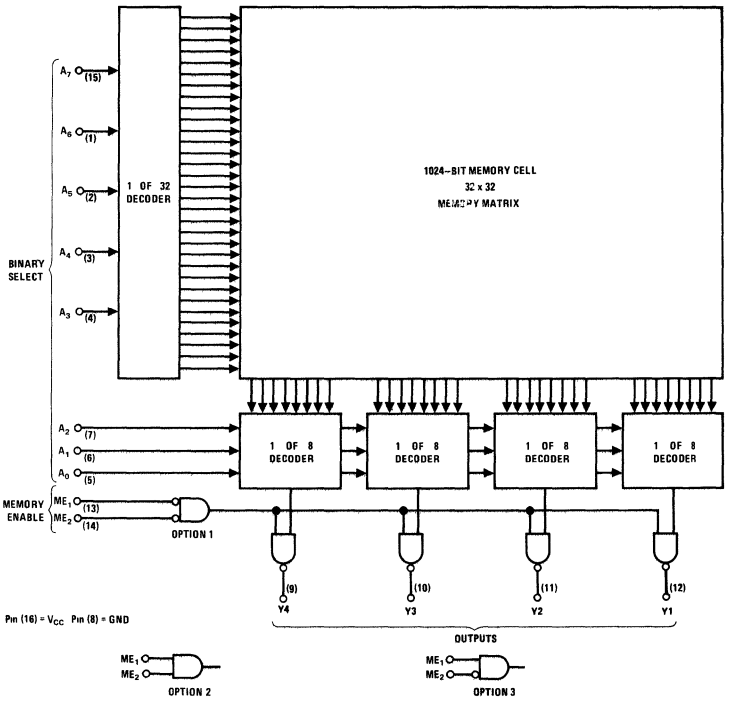
The "A" suffix is used to denote that full "tenth-power" technology has been employed in building this ROM.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the logical "1" state.

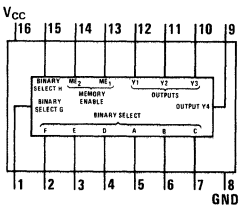
features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 60 mW
- Typical access time 85 ns
- Custom-programmed memory enable inputs
- Open-collector outputs

logic diagram



connection diagram



truth table

OPTION	ME_1	ME_2	OUTPUTS
1	0	0	Normal
	1	X	Logical 1
	X	1	Logical 1
2	1	1	Normal
	0	X	Logical 1
	X	0	Logical 1
3	1	0	Normal
	X	1	Logical 1
	0	X	Logical 1

X = Don't care

DM70L95, DM70L97 TRI-STATE® hex buffers

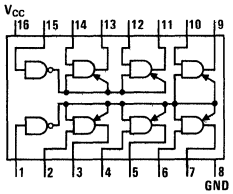
general description

The DM70L95 and DM70L97 are a collection of six non-inverting buffer gates which can be disabled to provide a high impedance (TRI-STATE) output. The disable function is performed by two inputs, DIS_1 and DIS_2, which produce the TRI-STATE when taken high. For the DM70L95 all outputs go to the Hi-z STATE if DIS_1 or DIS_2 are high. For the DM70L97, outputs 1, 2, 3, and 4 are disabled (Hi-z) when DIS_1 = "1" and outputs 5 and 6 are disabled (Hi-z) for DIS_2 = "1."

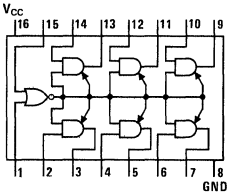
features

- TRI-STATE outputs
- Typical power dissipation 22 mW
- Typical propagation delay 40 ns
- DM70L95 and DM70L97 have same pinouts as DM7095 and DM7097 respectively

connection diagrams



DM70L95



DM70L97

DM70L96, DM70L98 TRI-STATE® hex buffers

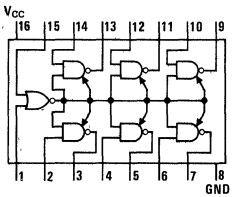
general description

The DM70L96 and DM70L98 are a collection of six inverting buffer gates which can be disabled to provide a high impedance (TRI-STATE) output. The disable function is performed by two inputs, DIS_1 and DIS_2, which produce the TRI-STATE when taken high. For the DM70L96 all outputs go to the Hi-z STATE if DIS_1 or DIS_2 are high. For the DM70L98, outputs 1, 2, 3, and 4 are disabled (Hi-z) when DIS_1 = "1" and outputs 5 and 6 are disabled (Hi-z) for DIS_2 = "1."

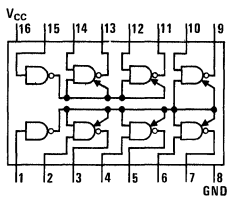
features

- TRI-STATE outputs
- Typical power dissipation 17 mW
- Typical propagation delay 30 ns
- DM70L96 and DM70L98 have same pinouts as DM7096 and DM7098 respectively

connection diagrams



DM70L96



DM70L98

DM76L13/DM86L13 quad gated D flip flop

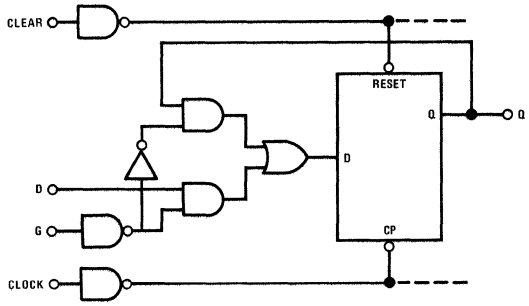
general description

The DM76L13/DM86L13 is a low power TTL quad gated D flip flop with direct clear and gated inputs. The gate, if set to a logical "1" level, will inhibit data entry from the data input.

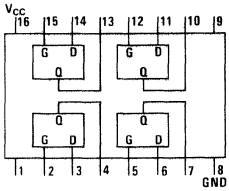
features

- Positive-edge-triggered, buffered clock
- Typical power dissipation 25 mW
- Typical propagation delay 70 ns
- Pin compatible with std. TTL DM7613/DM8613

logic diagram



connection diagram



truth table

D	G	CLR	Q_{N+1}
1	0	0	1
0	0	0	0
X	1	0	Q_N
X	X	1	0*

*Asynchronous transition
X = Don't care

DM76L97/DM86L97 TRI-STATE® 1024-bit read only memory

general description

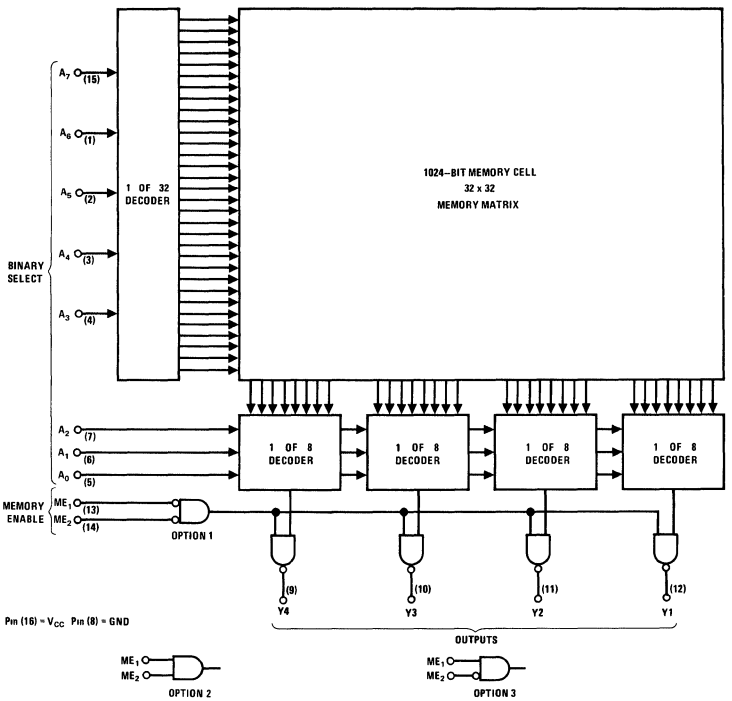
The DM76L97/DM86L97 is a custom-programmed read-only-memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the high impedance state.

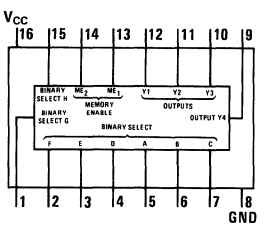
features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 60 mW
- Typical access time 70 ns
- Custom-programmed memory enable inputs
- TRI-STATE outputs

logic diagram



connection diagram



truth table

OPTION	ME_1	ME_2	OUTPUTS
1	0	0	Normal
	1	X	Logical 1
	X	1	Logical 1
2	1	1	Normal
	0	X	Logical 1
	X	0	Logical 1
3	1	0	Normal
	X	1	Logical 1
	0	X	Logical 1

X = Don't care

DM76L99/DM86L99 TRI-STATE® 64-bit random access memory

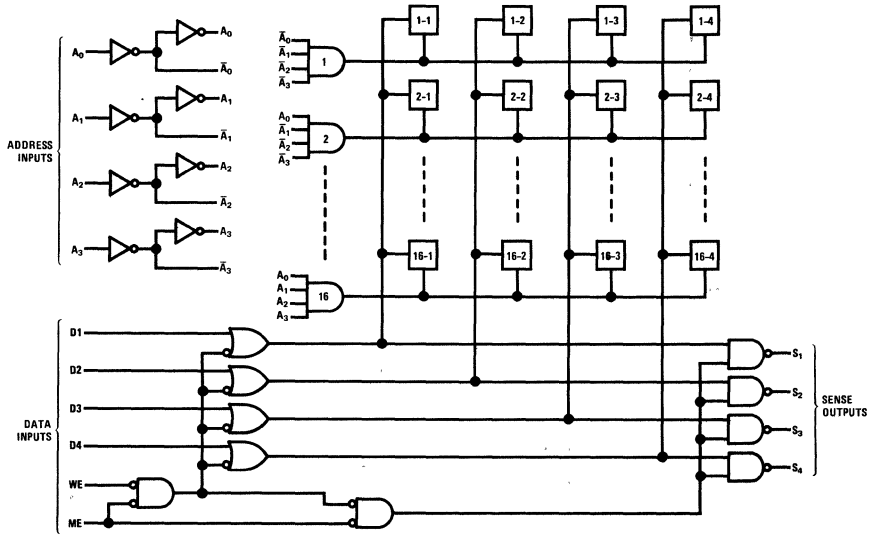
general description

The DM76L99/DM86L99 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 75 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

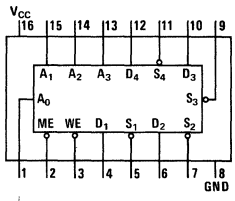
features

- Series 54L74L compatible
- Same pin-out as SN5489/SN7489, 3101, 5501
- Organized as 16 4-bit words
- Expandable to 1200 4-bit words without additional resistors
- Typical access from chip enable 50 ns
- Typical access time 80 ns
- Typical power dissipation 55 mW

logic diagram



connection diagram



truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

LM160 high speed differential voltage comparator

general description

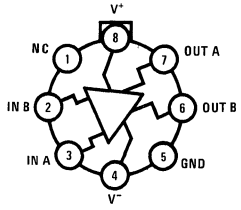
The LM160 high speed comparator is designed to be used in D to A and disc file pre amp applications where speed is critical. It is designed with a high impedance differential input stage and provides complementary saturated logic output levels, with minimum skew between outputs. The device operates off of ±4.5V to ±6.0V supplies and has outputs which are compatible with standard DTL/TTL levels. This product is pin and function compatible with the μA760. TO-5, dual-in-line and flat package versions of this product will be available.

features

- Response time 15 ns
- Bias current max. 10 μA
- Offset voltage 2 mV
- Voltage gain 3000

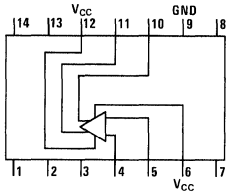
connection diagrams

Metal Can Package



TOP VIEW

Dual-In-Line Package



LM161 high speed differential voltage comparator

general description

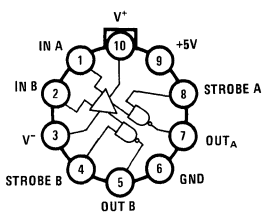
The LM161 high speed comparator is designed for D to A and disc file pre amp applications where speed is critical. It features a high impedance differential input stage and provides complementary saturated logic output levels with minimum skew between outputs. Each output is individually strobed and is compatible with standard DTL/TTL levels. The preamplifier section is capable of operating from ±4.5V to ±15V supplies, and is independent of supply symmetry. This comparator is pin and function compatible with the NE529. TO-5, dual-in-line and flat package versions of the product will be available.

features

- Op amp supply compatible
- Common mode range ±7V
- Individual output strobing
- Maximum bias current 10 μA
- Response time 15 ns
- Offset voltage 2 mV
- Voltage gain 3000

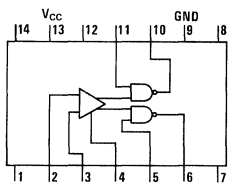
connection diagrams

Metal Can Package



TOP VIEW

Dual-In-Line Package



LM55325/LM75325 memory driver

general description

The LM55325 and LM75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

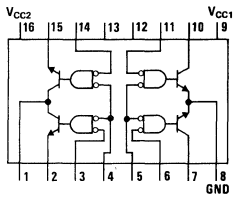
The source stage features node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then nodes R and R_{INT} can be shorted externally. This activates an internal resistor connected from V_{CC2} to node R. This method provides adequate base drive for source current up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

The LM55325 operates over the full military temperature range of −55°C to 125°C, while the LM75325 operates from 0°C to 70°C.

features

- 600 mA output capability
- 24 volt output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

connection diagram



truth table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

Note Not more than one output is to be on at any one time

LM75324 memory driver with decode inputs

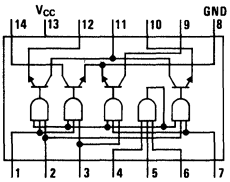
general description

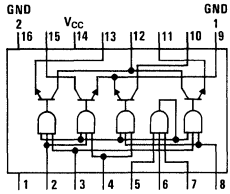
The LM75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X).

features

- 400 mA output capability
- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- Fast switching times
- 0°C to 70°C operation
- DTL/TTL compatible

connection diagrams





truth table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

Note 1: X - Logical 1 or logical 0

Note 2: Not more than one output is to be allowed to be ON at one time When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0

LM75461, LM75462, LM75463, LM75464 dual peripheral drivers (high voltage)

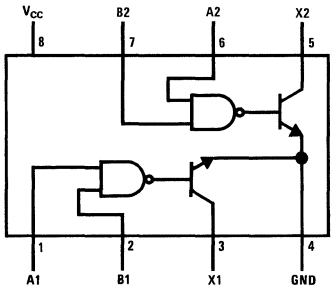
general description

These circuits are high voltage versions of the LM75451A, LM75452, LM75453, and LM75454 series. Pin configurations for the corresponding parts in the two series are identical. Each circuit contains two independent high voltage transistors each capable of sinking 300 mA at the same time.

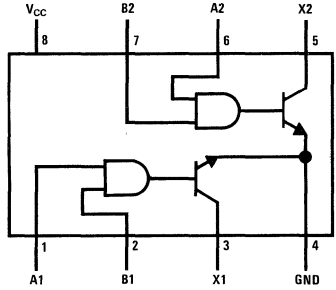
features

- High breakdown
- Outputs withstand high voltage with V_{CC} = 0V for power strobing applications
- Both outputs can sink 300 mA simultaneously
- Two separate drivers per package
- 0°C to 70°C operation
- Identical pin configurations as the lower voltage LM75450 series equivalents
- 8-pin mini-dual-in-line package
- Inputs have clamp diodes and are DTL/TTL compatible

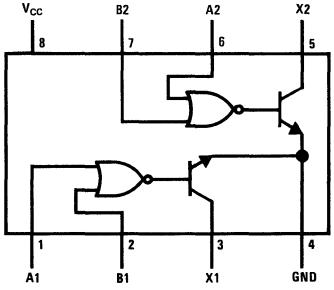
connection diagrams



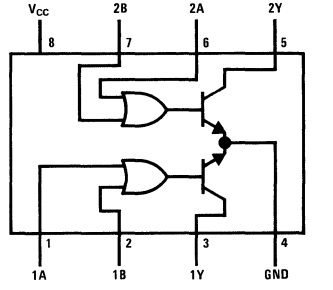
TOP VIEW
LM75461



TOP VIEW
LM75462



TOP VIEW
LM75463



TOP VIEW
LM75464

MH7803/MH8803, MH7807/MH8807 oscillator/clock drivers

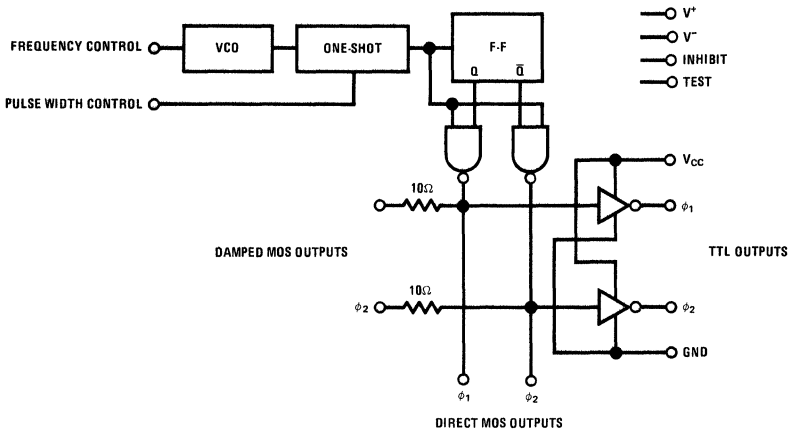
general description

The MH7803/MH8803 and MH7807/MH8807 are complete self-contained two-phase oscillators and clock driver subsystems for MOS micro-computer, calculator and shift register systems.

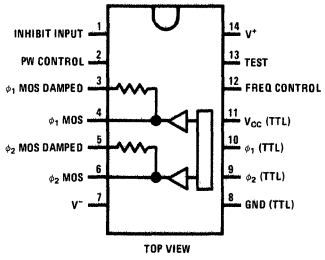
features

- No external timing components
- Two non-overlapping outputs
- Both frequency and pulse width are voltage controlled
- Frequency adjustable from 100 kHz to 500 kHz (MH7803/MH8803) and from 400 kHz to 2 MHz (MH7807/MH8807)
- Pulse width adjustable from 300 ns to 2μs
- Low power for battery operation
- TTL outputs for verification and synchronization
- Both direct and damped MOS outputs

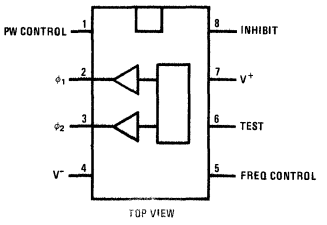
logic diagram



connection diagrams



MH7803/MH8803



MH7807/MH8807

MH8804, MH8805 quad, dual MOS memory drivers

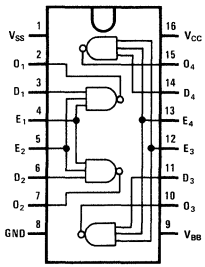
general description

The quad MH8804 and the dual MH8805 are bipolar to MOS drivers specifically designed to drive input address lines for MOS memory arrays using MM1103 type RAMs. The MH8804 is pin compatible with the 13207 and the MH8805 with the SN75361.

features

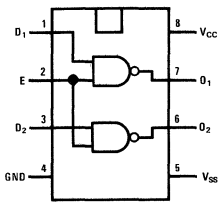
- Current mode output drive ±500 mA
- Rise and fall times 20 ns
- Delay times 15 ns
- High output voltage V_{SS} − 1.0V
- Low output voltage 0.3V
- Input levels TTL/DTL

connection diagrams



TOP VIEW

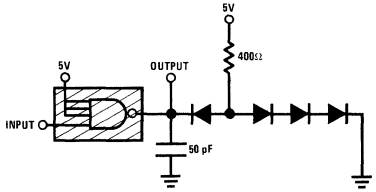
MH8804



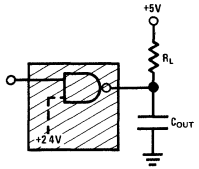
TOP VIEW

MH8805

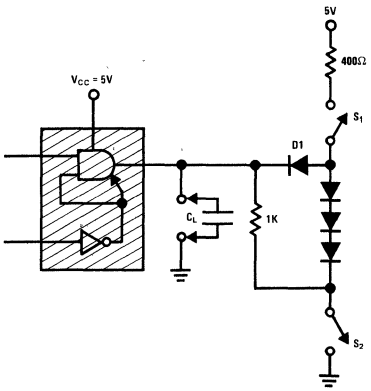
AC Test Circuits



Test Circuit 1



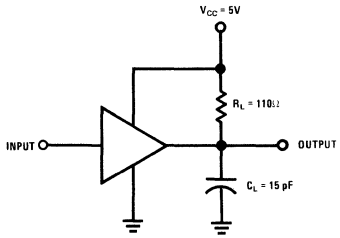
Test Circuit 2



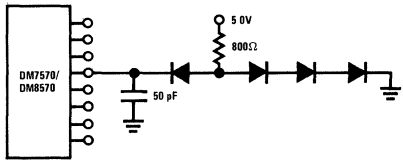
	S_1	S_2	C_L
t_{pd1}	Closed	Closed	50 pF
t_{pd0}	Closed	Closed	50 pF
t_{0H}	Closed	Closed	5 pF *
t_{1H}	Closed	Closed	5 pF *
t_{H0}	Closed	Open	50 pF
t_{H1}	Open	Closed	50 pF

*Approximate value of jig capacitance only

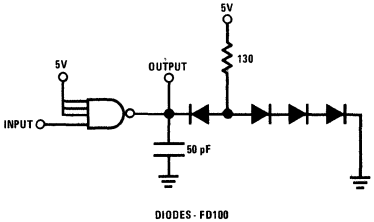
Test Circuit 3



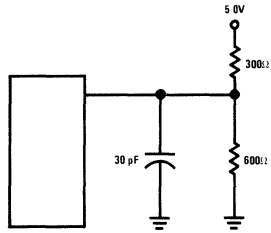
Test Circuit 4



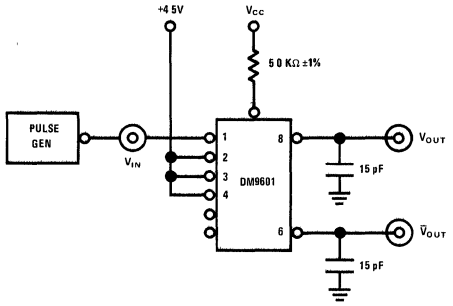
Test Circuit 5



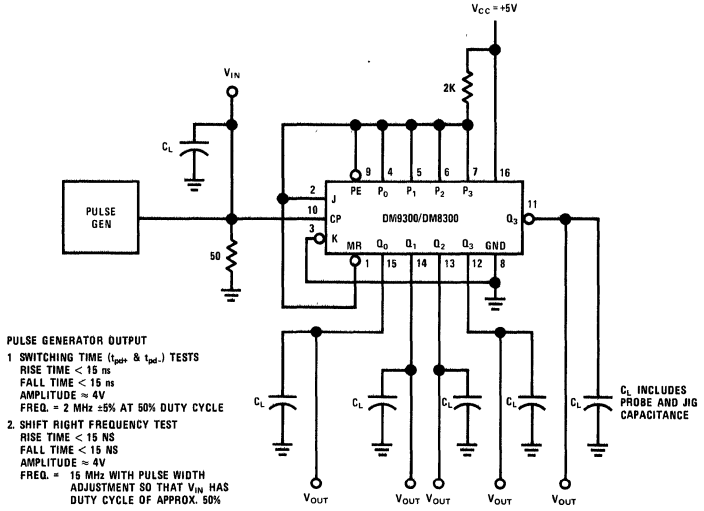
Test Circuit 6



Test Circuit 7



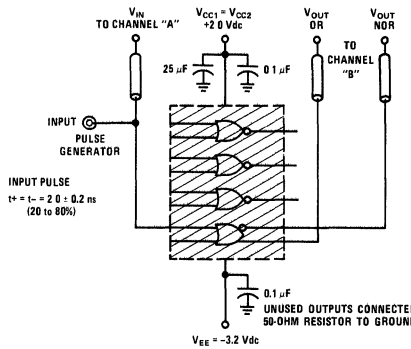
Test Circuit 8



PULSE GENERATOR OUTPUT

1. SWITCHING TIME (t_{pd+} & t_{pd-}) TESTS
   RISE TIME < 15 ns
   FALL TIME < 15 ns
   AMPLITUDE ≈ 4V
   FREQ. = 2 MHz ±5% AT 50% DUTY CYCLE
2. SHIFT RIGHT FREQUENCY TEST
   RISE TIME < 15 NS
   FALL TIME < 15 NS
   AMPLITUDE ≈ 4V
   FREQ. = 15 MHz WITH PULSE WIDTH ADJUSTMENT SO THAT V_{IN} HAS DUTY CYCLE OF APPROX. 50%

Test Circuit 9



ALL INPUT AND OUTPUT CABLES TO THE SCOPE ARE EQUAL LENGTHS OF 50-OHM COAXIAL CABLE WIRE LENGTH SHOULD BE < 1/4 INCH FROM TP_{IN} TO INPUT PIN AND TP_{OUT} TO OUTPUT PIN.

Test Circuit 10

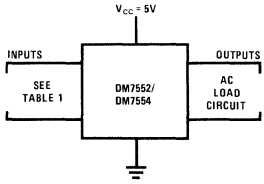
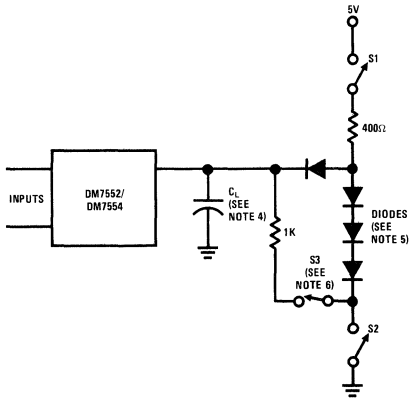


Figure 1 (Test Circuit)

TEST	INPUT CONDITIONS						
	OD1	OD2	CE	CLEAR	PRESET	CP	TRANSFER ENABLE
t_{pd0}	GND	GND	V_{CC}	GND	GND	See Note 1	V_{CC}
t_{pd1}	GND	GND	V_{CC}	GND	GND	See Note 1	V_{CC}
$t_{pd(TE)}$	GND	GND	V_{CC}	GND	GND	See Note 1	See Note 2
t_{1H}	See Note 3	See Note 3	GND	GND	V_{CC}	GND	V_{CC}
t_{0H}	See Note 3	See Note 3	GND	V_{CC}	GND	GND	V_{CC}
t_{H1}	See Note 3	See Note 3	GND	GND	V_{CC}	GND	V_{CC}
t_{H0}	See Note 3	See Note 3	GND	V_{CC}	GND	GND	V_{CC}
f_{clock}	GND	GND	V_{CC}	GND	GND	See Note 8	V_{CC}

Table 1



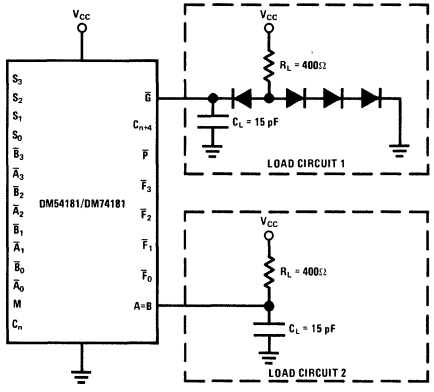
NOTE 1 PULSE GEN PRR ≤ MHz, $t_r \leq 15$ ns, $t_f \leq 5$ ns, t_p (CLOCK) ≥ 200 ns
NOTE 2 See AC SWITCHING TIME WAVEFORMS
NOTE 3 TIE THESE INPUTS TOGETHER, SEE SWITCHING TIME WAVEFORMS
NOTE 4 INCLUDES JIG CAPACITANCE
NOTE 5 ALL DIODES ARE FD100 OR EQUIVALENT
NOTE 6 OPEN SWITCH S_3 FOR t_{pd0}(TC), t_{pd1} (TC), t_{pd0}(CET), AND t_{pd1}(CET)
NOTE 7 JIG CAPACITANCE
NOTE 8 f_{CLOCK} USE 50% DUTY CYCLE

Figure 2 (Load Circuit)

TEST	SWITCH S_1	SWITCH S_2	C_L
t_{pd0}	Closed	Closed	50 pF
t_{pd1}	Closed	Closed	50 pF
$t_{pd(TE)}$	Closed	Closed	50 pF
t_{1H}	Closed	Closed	5 pF (See Note 7)
t_{0H}	Closed	Closed	5 pF (See Note 7)
t_{H1}	Open	Closed	50 pF
t_{H0}	Closed	Open	50 pF
f_{clock}	Closed	Closed	50 pF

Table 2

Test Circuit 11



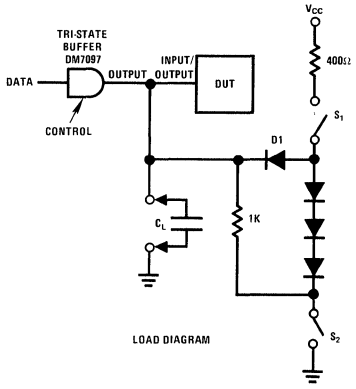
NOTE 1. USE LOAD CIRCUIT 2 FOR A = B OUTPUT ONLY LOAD CIRCUIT 1 SHOULD BE USED TO TEST THE REST OF THE OUTPUTS

NOTE 2 FOR INPUT PULSE, F = 1 MHz, $Z_{OUT} \approx 50\Omega$ 50% DUTY CYCLE, $V_{IN\ PP}$ = 3V $t_r = t_f \leq 10$ ns

NOTE 3 C_L INCLUDES PROBE AND JIG CAPACITANCE

NOTE 4 ALL DIODES ARE IN3064

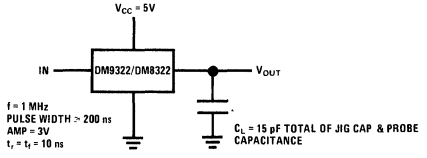
Test Circuit 12



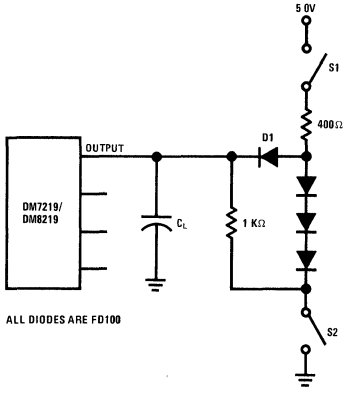
	S_1	S_2	C_L
t_S, t_h, t_{pdR}	Closed	Closed	50 pF
t_{wpw}, t_{rpw}	Closed	Closed	50 pF
t_{0H}	Closed	Closed	5 pF*
t_{1H}	Closed	Closed	5 pF*
t_{H0}	Closed	Open	50 pF
t_{H1}	Open	Closed	50 pF

*Approximate value of jig capacitance only

Test Circuit 13

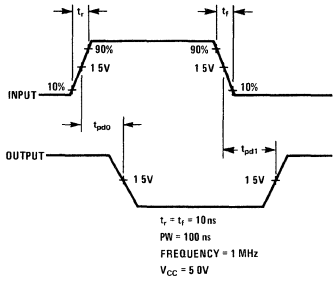


Test Circuit 14

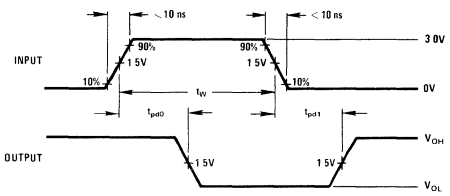


Test Circuit 15

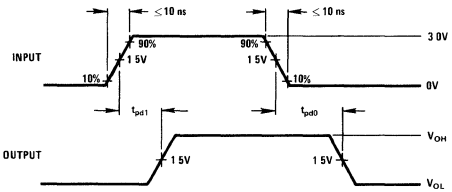
Switching Time Waveforms



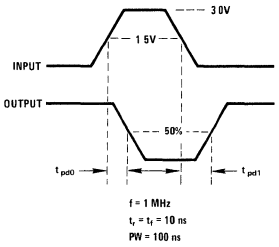
Waveform 1



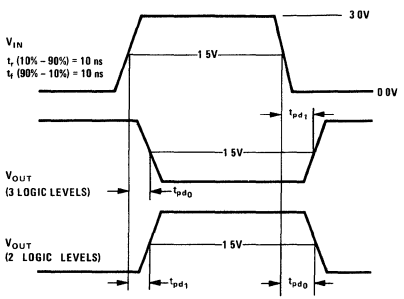
Waveform 2



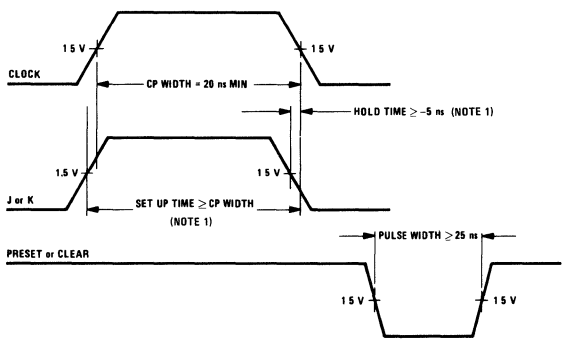
Waveform 3



Waveform 4

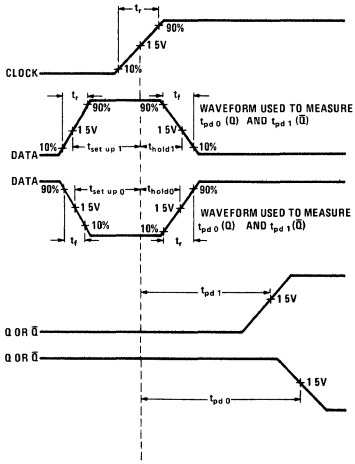


Waveform 5



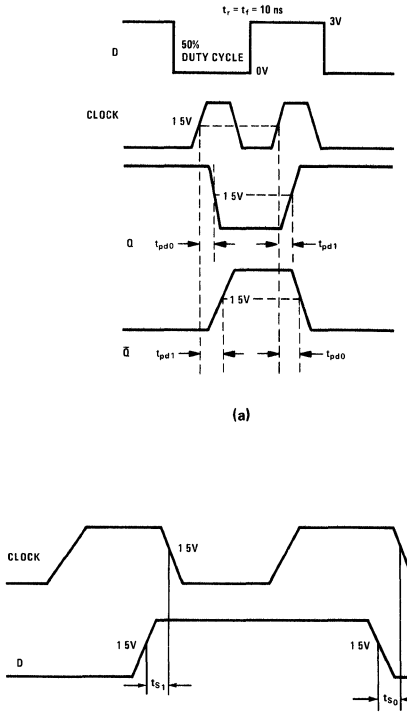
NOTE 1 J AND K INFORMATION WILL REGISTER PROPERLY EVEN THOUGH THE INFORMATION IS REMOVED 5 NS BEFORE THE CLOCK PULSE VOLTAGE FALLS HOWEVER WHEN THIS OCCURS IT MUST BE ASSURED THAT THE LOGICAL "1" CLOCK PULSE LEVEL AND THE DESIRED J AND K INFORMATION OCCUR SIMULTANEOUSLY FOR AT LEAST 20 NS

Waveform 6

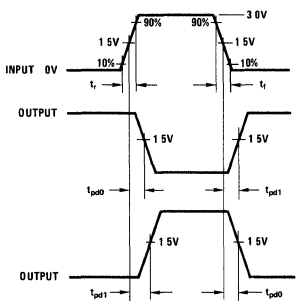


NOTE NO MAXIMUM RISE AND FALL TIMES ARE IMPOSED UPON THE CLOCK VOLTAGE HOWEVER VERY SLOW TRANSITIONS WHICH ALLOW AN INPUT TO REMAIN IN THRESHOLD REGION CAN CAUSE NOISE PROBLEMS

Waveform 7



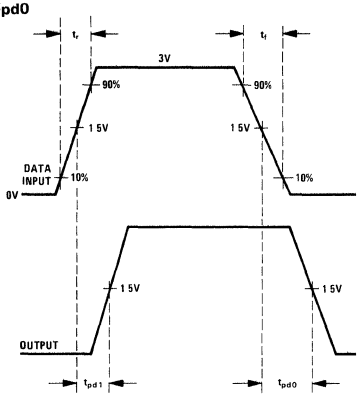
Waveform 8



FREQUENCY = 1 MHz
DUTY CYCLE = 50%
$t_r = t_f = 10$ ns

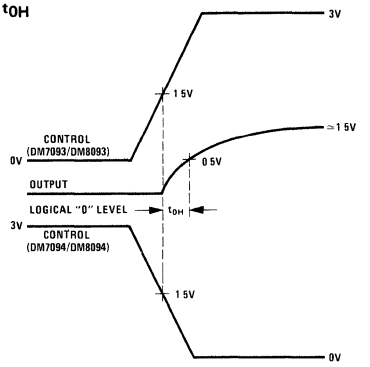
Waveform 9

t_{pd1} & t_{pd0}



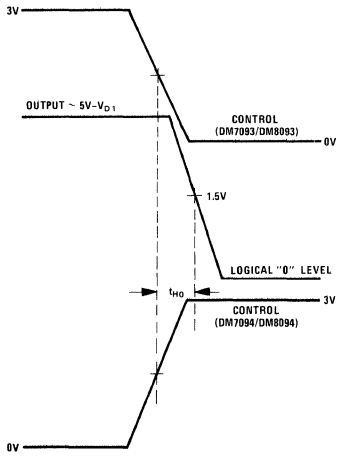
(a)

t_{0H}



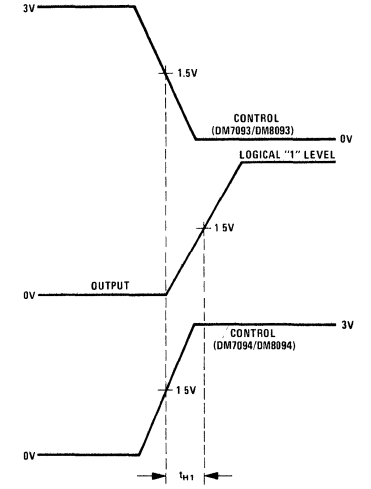
(b)

t_{H0}



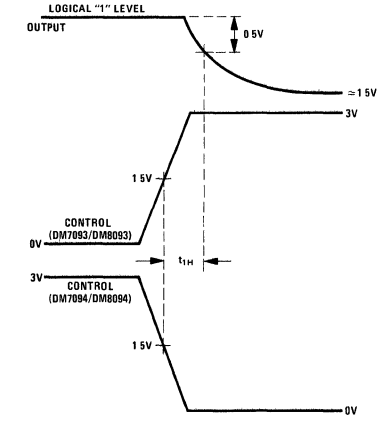
(c)

t_{H1}



(d)

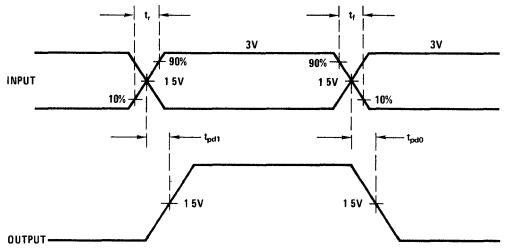
t_{1H}



(e)

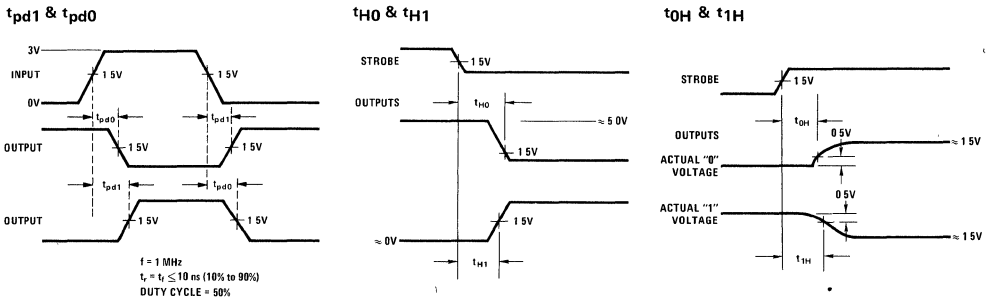
INPUT CHARACTERISTICS
FREQUENCY 1 MHz
PULSE WIDTH 100 ns
$t_r = t_f \leq 10$ ns
AMPLITUDE = 3V

Waveform 10

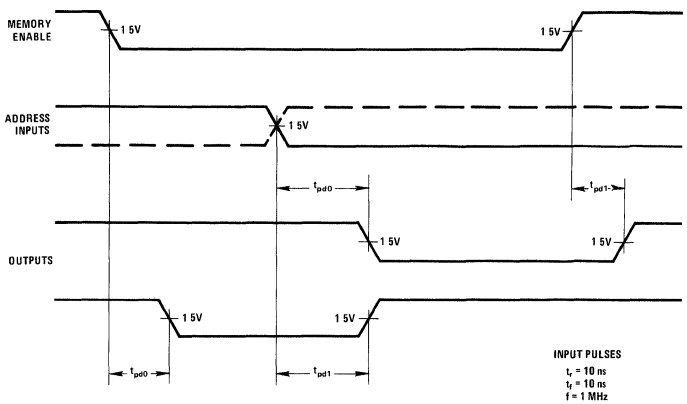


INPUT CHARACTERISTICS
AMPLITUDE = 3V
FREQUENCY = 1 MHz
$t_r = t_f = 10$ ns

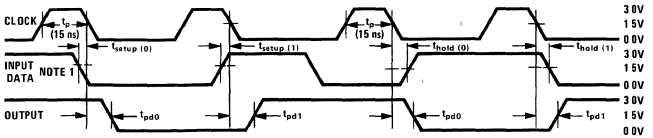
Waveform 11



Waveform 12



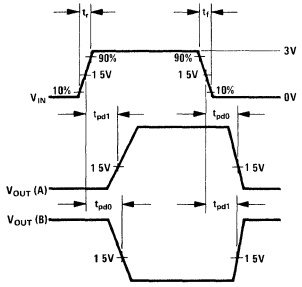
Waveform 13



$t_r = t_f = 10$ ns (10% to 90%) ON CLOCK AND INPUT DATA WAVEFORMS

NOTE 1 INPUT DATA IS APPLIED TO SERIAL INPUT WHEN MODE CONTROL EQUALS A LOGICAL ZERO INPUT DATA IS APPLIED TO INPUT A, B, C, OR D, WHEN MODE CONTROL EQUALS A LOGICAL ONE

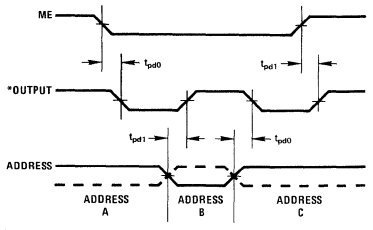
Waveform 14



$t_r = t_f = 10$ ns
PW = 100 ns
FREQUENCY = 1 MHz
V_{CC} = +5 0V

Waveform 15

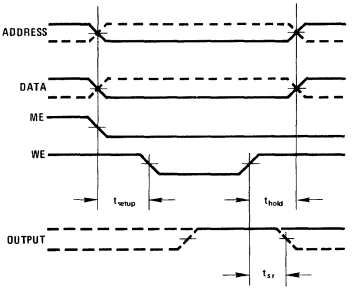
Read Cycle



*OUTPUT SHOWN FOR STORED DATA IN ADDRESS A = 1, IN ADDRESS B = 0

(a)

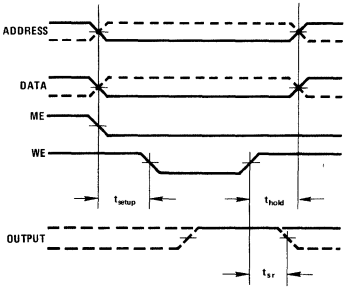
Write Cycle



(b)

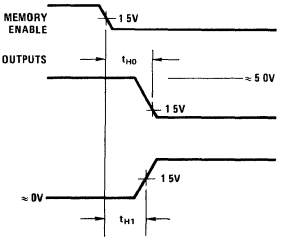
Waveform 16

Write Cycle



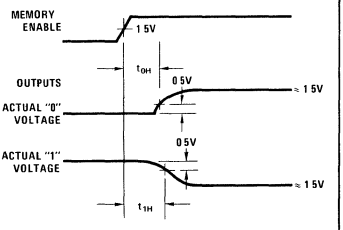
(a)

t_{H0} & t_{H1}



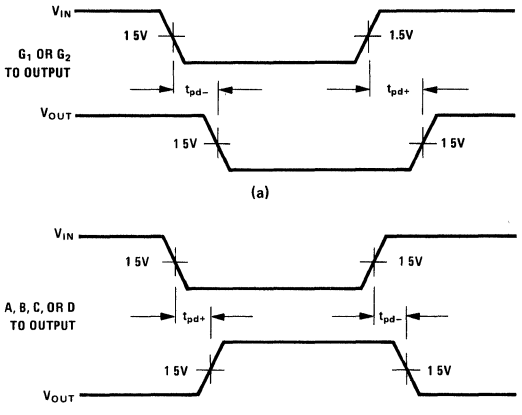
(b)

t_{0H} & t_{1H}

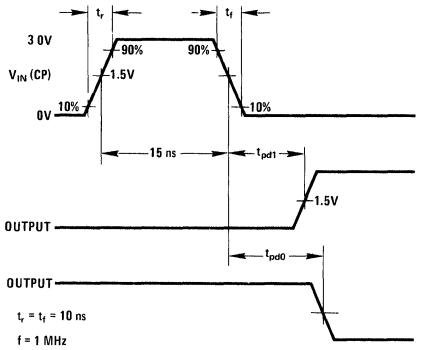


(c)

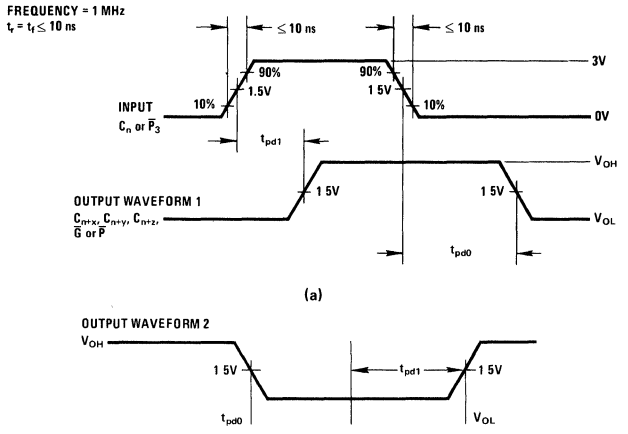
Waveform 17



Waveform 18



Waveform 19

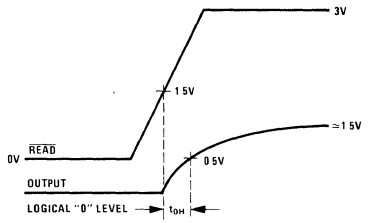


NOTE 1. C_L = 50 pF INCLUDING PROBE AND JIG CAPACITANCE FOR DM54182, DM74182.
NOTE 2 ALL DIODES ARE IN3064

(b)

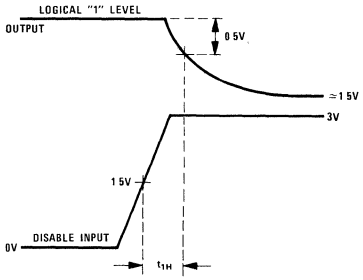
Waveform 20

t_{0H}



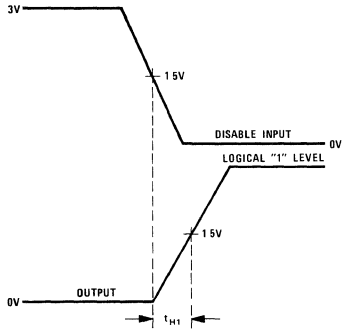
(a)

t_{1H}



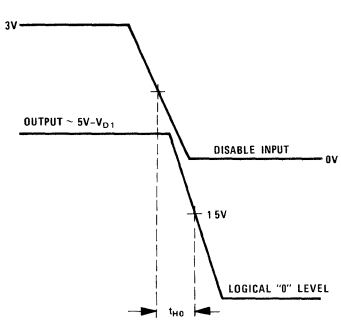
(b)

t_{H1}



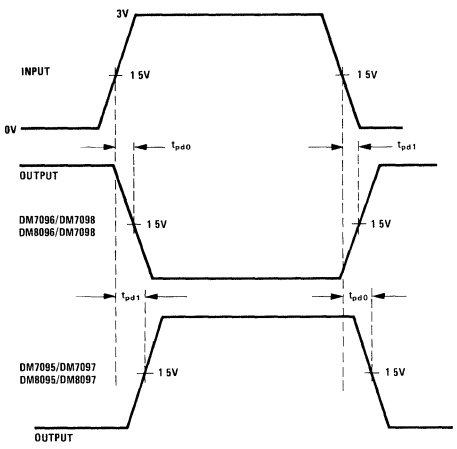
(c)

t_{H0}



(d)

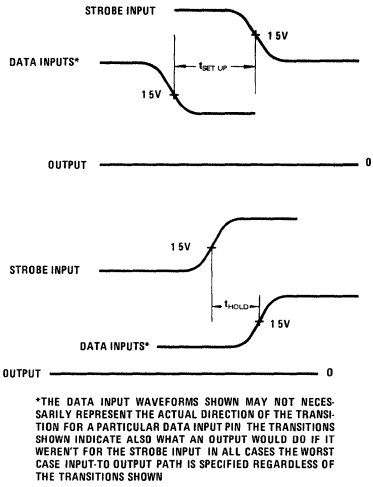
t_{pd1} & t_{pd0}



INPUT CHARACTERISTIC
AMPLITUDE = 3V
FREQUENCY = 1 MHz, 50% DUTY CYCLE
$t_r \simeq t_p \leq 10$ ns (10% to 90%)

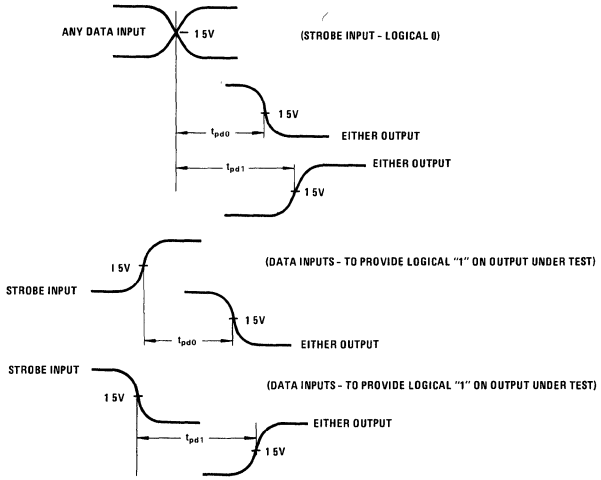
(e)

Waveform 21



*THE DATA INPUT WAVEFORMS SHOWN MAY NOT NECESSARILY REPRESENT THE ACTUAL DIRECTION OF THE TRANSITION FOR A PARTICULAR DATA INPUT PIN THE TRANSITIONS SHOWN INDICATE ALSO WHAT AN OUTPUT WOULD DO IF IT WEREN'T FOR THE STROBE INPUT IN ALL CASES THE WORST CASE INPUT-TO OUTPUT PATH IS SPECIFIED REGARDLESS OF THE TRANSITIONS SHOWN

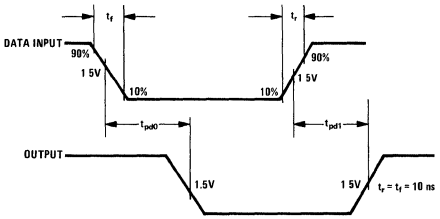
(a)



(b)

Waveform 22

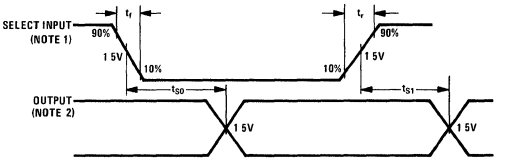
1 PROPAGATION DELAYS FROM DATA INPUTS TO OUTPUT



SET INPUTS A, B, C SUCH THAT TESTED INPUT IS ROUTED TO THE OUTPUT

(a)

2 SETTLING TIMES FROM CHANGE OF A, B, or C TO CORRECT DATA OUTPUT



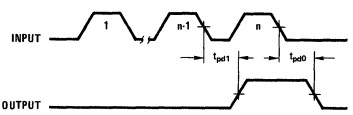
DATA INPUTS CONNECTED IN ANY LOGIC CONFIGURATION

NOTE 1 WHEN THE SELECT INPUTS ARE TAKEN TO OPPOSITE LOGICAL LEVELS SIMULTANEOUSLY, THE ONE (ONES) MAKING THE LOGICAL "1" TO LOGICAL "0" TRANSITION PROVIDE THE WORST-CASE PATH

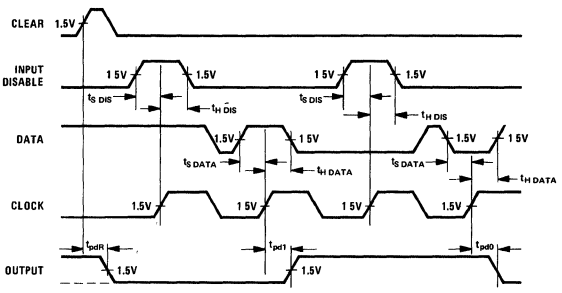
NOTE 2 TRANSITION TIMES SPECIFIED ARE INDEPENDENT OF THE DIRECTION OF THE OUTPUT WAVEFORM

(b)

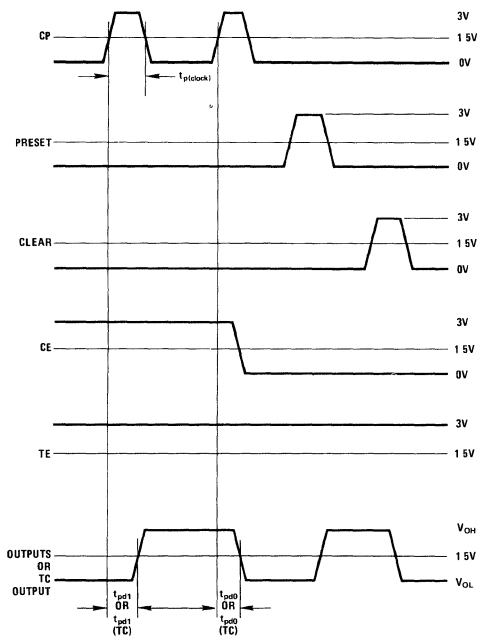
Waveform 23



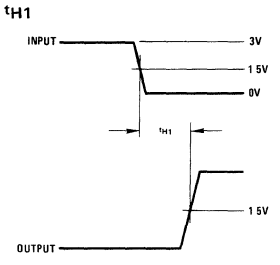
Waveform 24



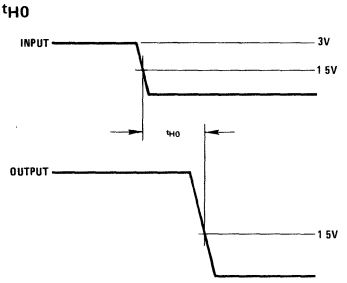
Waveform 25



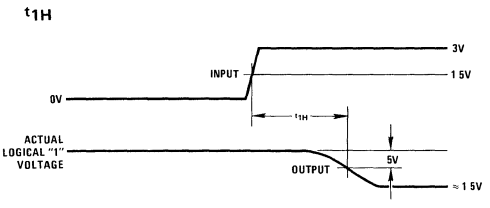
(a)



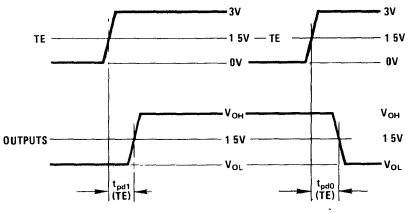
(b)



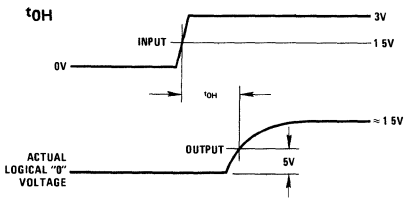
(c)



(d)



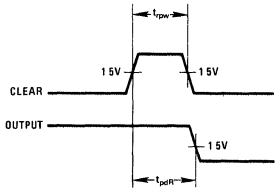
(e)



(f)

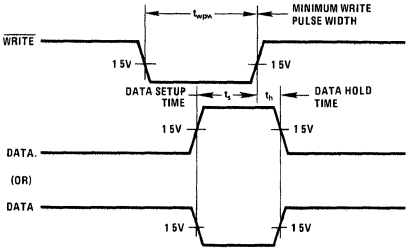
Waveform 26

Clear Pulse Width and Delay



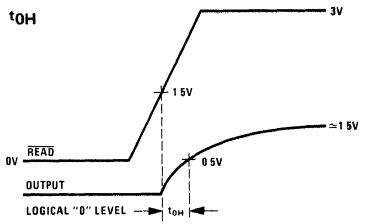
(a)

Data Setup and Hold



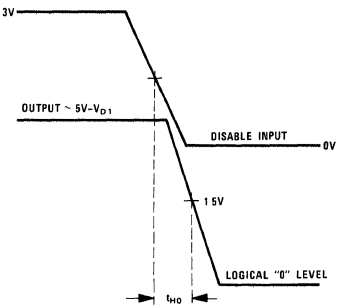
(b)

t_{0H}



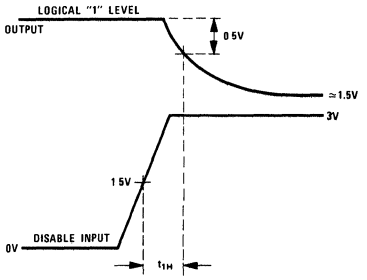
(c)

t_{H0}



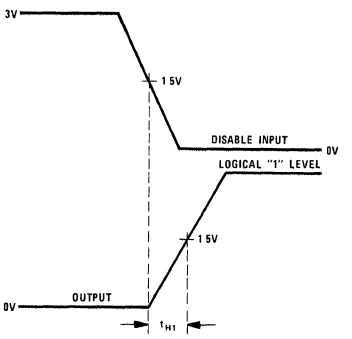
(d)

t_{1H}



(e)

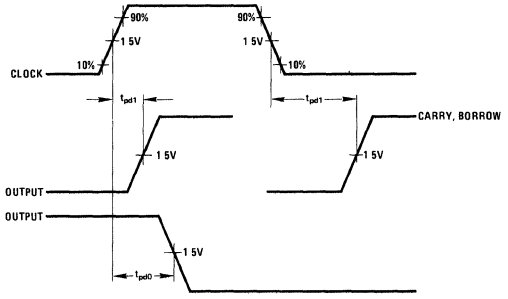
t_{H1}



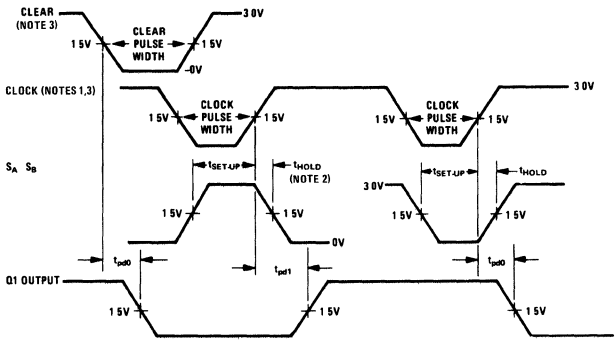
(f)

INPUT CHARACTERISTICS
FREQ 1 MHz
PULSE WIDTH 100 ns
$t_r = t_f < 10$ ns
AMPLITUDE = 3V

Waveform 27



Waveform 28

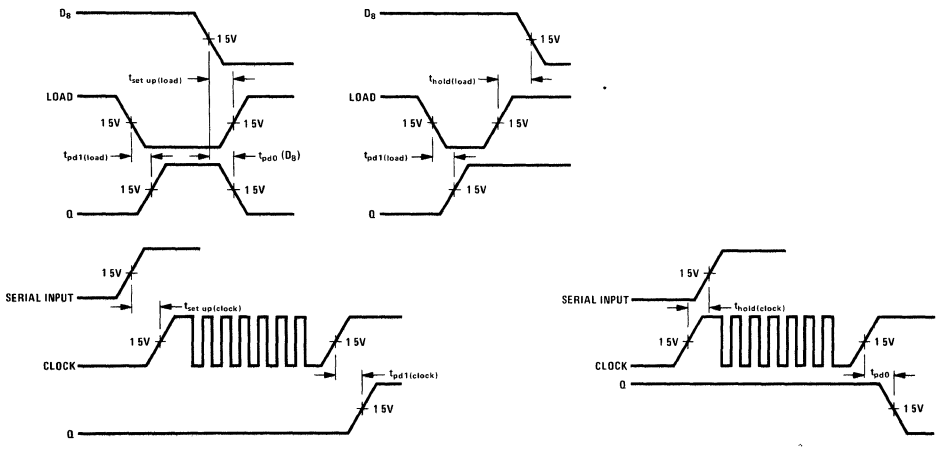


NOTE 1. CLOCK MAY BE AT EITHER A LOGICAL "1" OR A LOGICAL "0" WHILE CLEARING

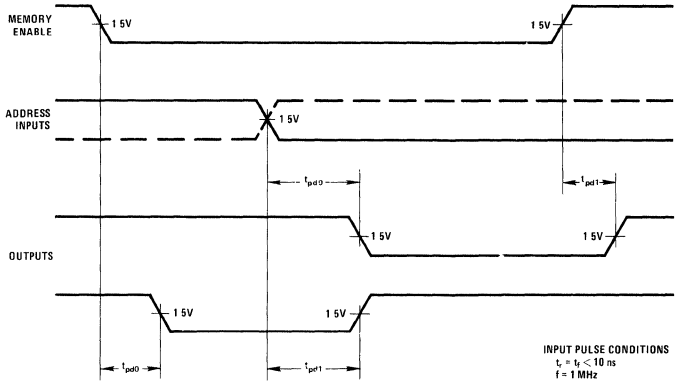
NOTE 2. NEGATIVE HOLD TIME VALUES INDICATE S_A - S_B INFORMATION MAY BE RELEASED PRIOR TO THE TIME THE CLOCK PULSE REACHES ITS 1 5V LEVEL

NOTE 3 CLEAR AND CLOCK WAVEFORMS $t_r = t_f = 10$ ns (10%-90%, 90%-10% TRANSITION), f = 1 MHz

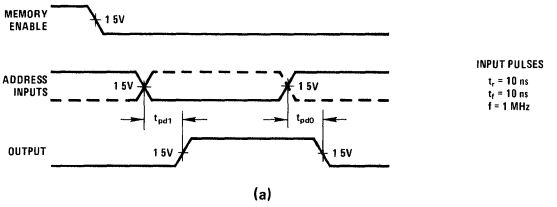
Waveform 29



Waveform 30

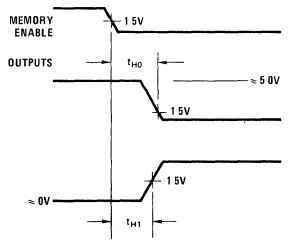


Waveform 31



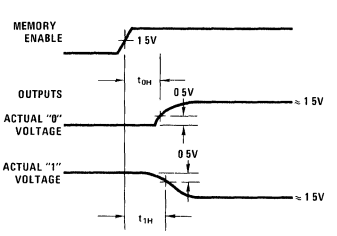
(a)

t_{H0} & t_{H1}



(b)

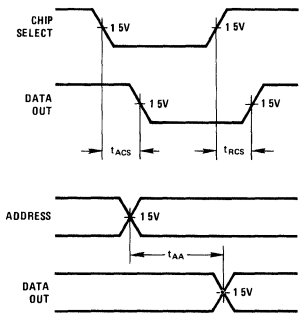
t_{0H} & t_{1H}



(c)

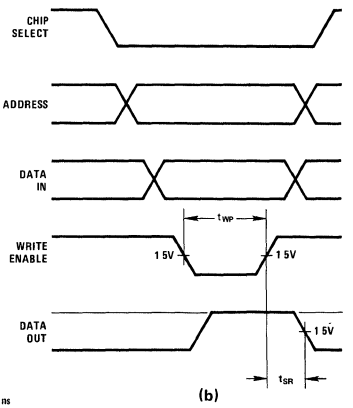
Waveform 32

Read Mode



(a)

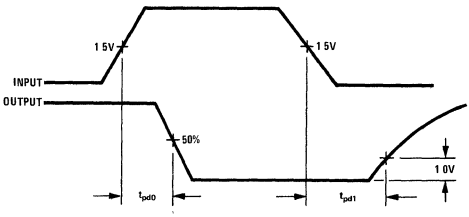
Write Mode



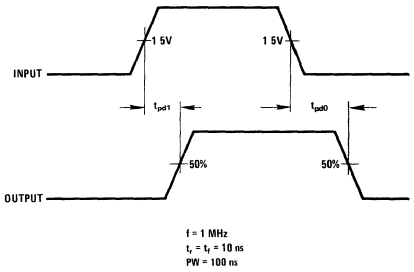
(b)

PULSE AMPLITUDE = 3 0V
RISE TIME AND FALL TIME ≤ ns

Waveform 33

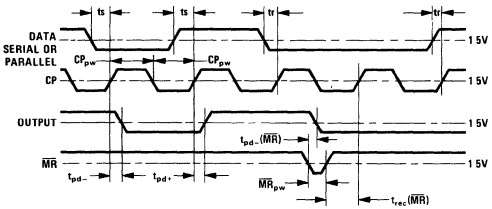


Waveform 34

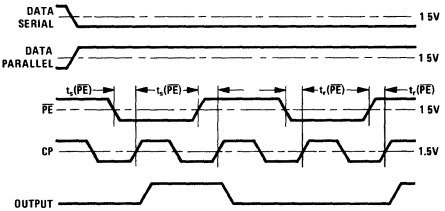


f = 1 MHz
$t_r = t_f$ = 10 ns
PW = 100 ns

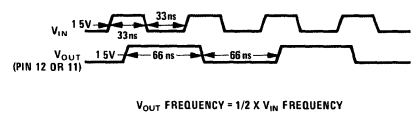
Waveform 35



(a)



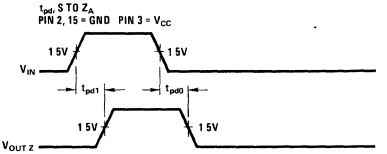
(b)



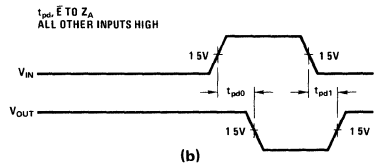
V_{OUT} FREQUENCY = 1/2 X V_{IN} FREQUENCY

(c)

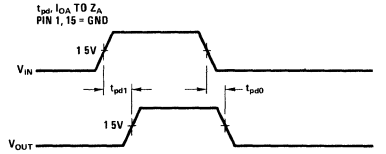
Waveform 36



(a)

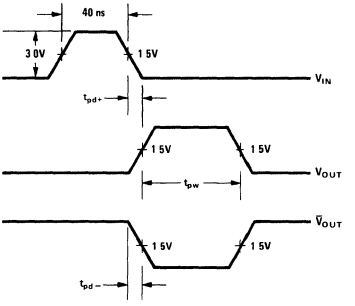


(b)



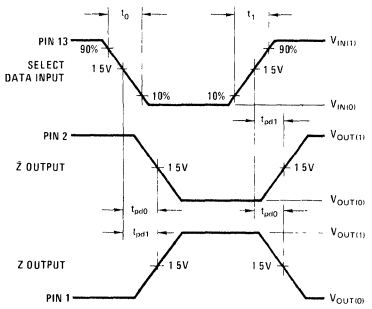
(c)

Waveform 37



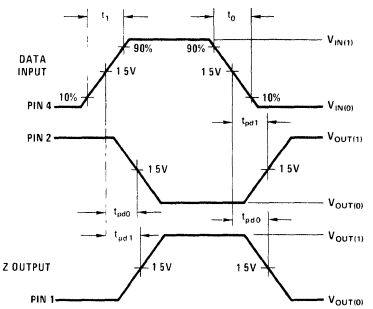
NOTE CAPACITANCE INCLUDES JIG AND PROBE

Waveform 38



SELECT DATA INPUT TO OUTPUT VOLTAGE WAVEFORMS E IS LOGICAL "0", I_0 IS LOGICAL "1" & V_1 = 0V
PINS 3, 5, 11 = GND
PINS 4, 6, 7, 9, 10, 12 = V_{CC}

(a)

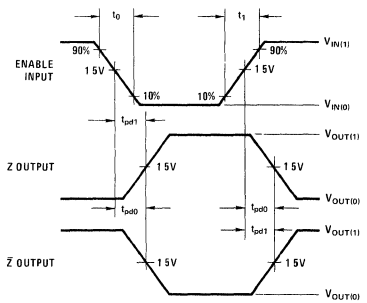


DATA INPUT TO OUTPUT VOLTAGE WAVEFORMS
PINS 5, 6, 7, 9, 10, 11 = V_{CC}
E & S_0 ARE LOGICAL "0" & V_1 = 4.5V
PINS 3, 13 = GND

(b)

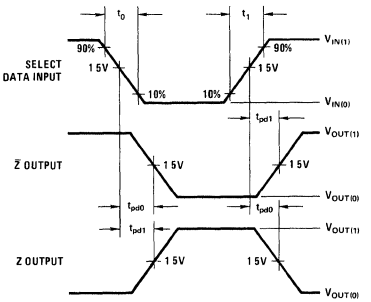
FREQUENCY = 1 MHz
DUTY CYCLE = 50%
$t_r = t_f$ = 10 ns
AMPLITUDE = 3V

Waveform 39



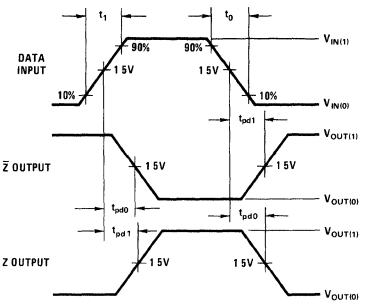
ENABLE TO OUTPUT VOLTAGE WAVEFORMS
S_0 IS LOGICAL "0" I_0 IS LOGICAL "1" & V_1 = 4.5V

(a)



SELECT DATA INPUT TO-OUTPUT VOLTAGE WAVEFORMS E IS LOGICAL "0", I_0 IS LOGICAL "1" & V_1 = 0V

(b)

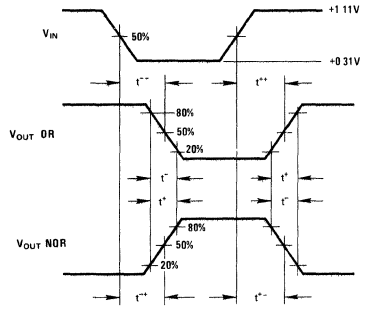


DATA INPUT-TO OUTPUT VOLTAGE WAVEFORMS
E & S_0 ARE LOGICAL "0" & V_1 = 4.5V

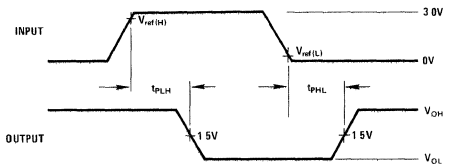
(c)

FREQUENCY = 1 MHz
DUTY CYCLE = 50%
$t_r = t_f$ = 10 ns
AMPLITUDE = 3V

Waveform 40



Waveform 41



Waveform 42

Physical Dimensions

PACKAGES

DUAL-IN-LINE PACKAGES

(N) All devices ordered with the "N" suffix are supplied in either the 14-pin, 16-pin, or 24-pin molded dual-in-line package. Molding material is EPOXY B, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot solder dipped surface to allow for ease of solderability.

(J) All devices ordered with the "J" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic dual-in-line package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(D) All devices ordered with the "D" suffix are supplied in either 14-pin or 16-pin glass/metal dual-in-line package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

METAL CAN PACKAGES

(H) All devices ordered with the "H" suffix are supplied in either 8-pin or 10-pin TO-5 style metal can package. The cap is chrome-plated kovar and the leads are gold-plated kovar.

(G) All devices ordered with the "G" suffix are supplied in a 12-pin TO-8 style metal can package. The cap is chrome-plated kovar and the leads are gold plated kovar.

FLAT PACKAGES

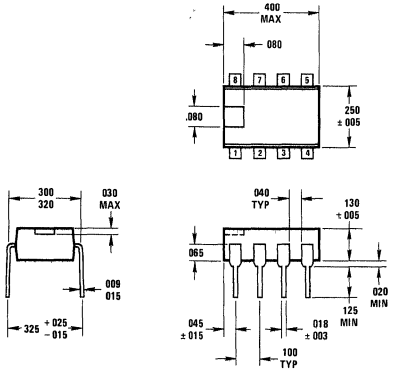
(W) All devices ordered with the "W" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic flat package The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(F) All devices ordered with the "F" suffix are supplied in either the 14-pin, 16-pin, or 24-pin glass/metal flat package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

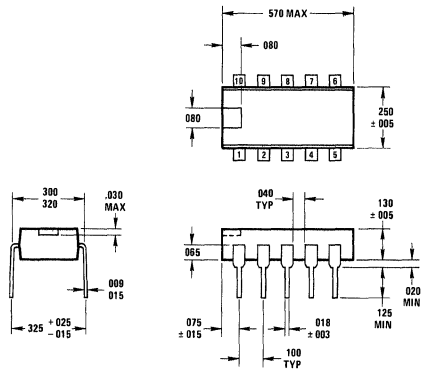
Four combinations of bottom insulator and formed leads are supplied. Suffix coding is as follows:

Suffix	Bottom Insulator	Formed Leads
–00 (Ex: DM54L00F-00)	No	No
–01	Yes	Yes
–06	Yes	No
–07	No	Yes

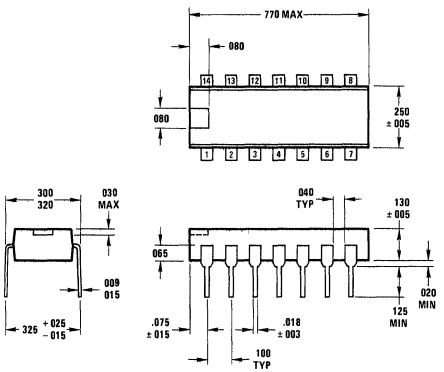
If no suffix is added, parts will be supplied as if the –00 suffix had been ordered.
Note: All dimensions are in inches.



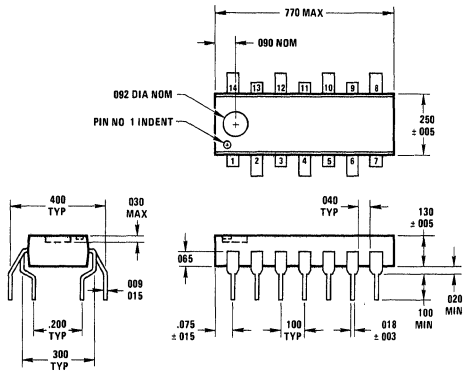
Package 1
8 Lead Molded Mini DIP (N)



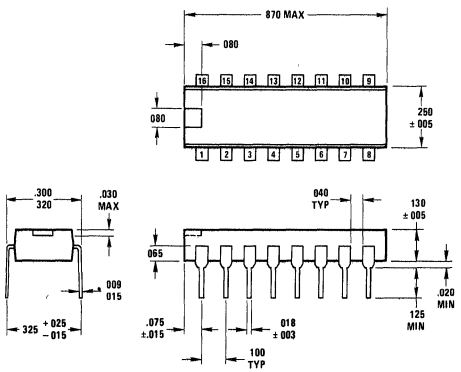
Package 2
10 Lead Molded DIP (N)



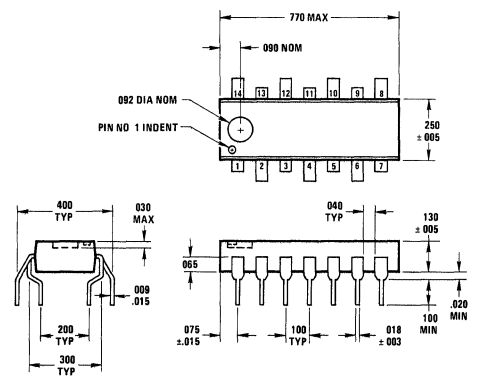
Package 3
14 Lead Molded DIP (N)



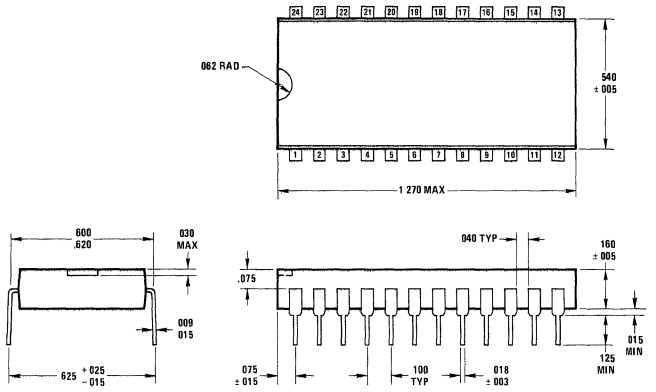
Package 4
14 Lead Molded DIP (N-01)
(Staggered Leads)



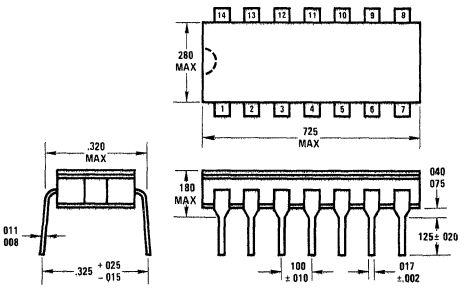
Package 5
16 Lead Molded DIP (N)



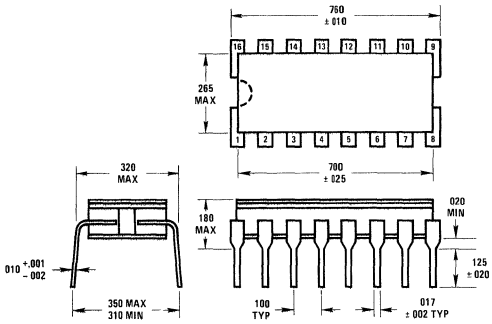
Package 6
16 Lead Molded DIP (N-01)
(Staggered Leads)



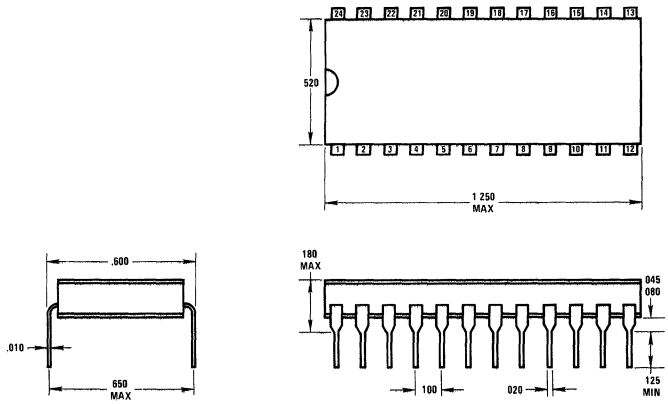
Package 7
24 Pin Molded DIP (N)



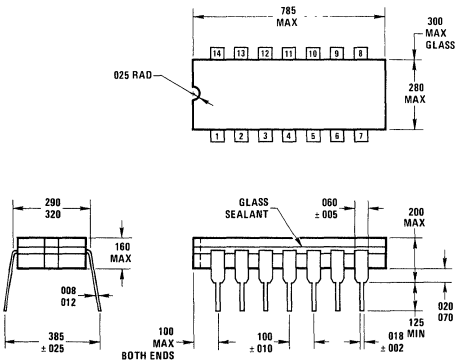
Package 8
14 Pin Cavity DIP (D)



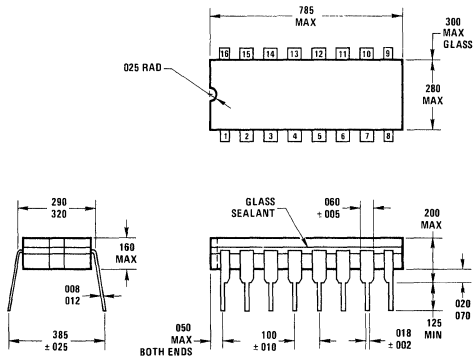
Package 9
16 Pin Cavity DIP (D)



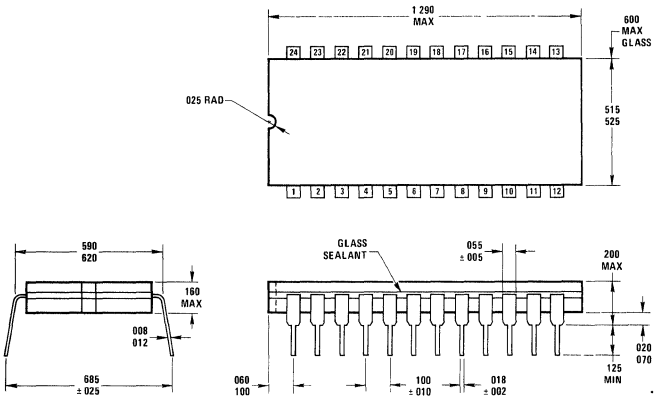
Package 10
24 Pin Cavity DIP (D)



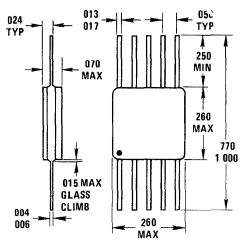
Package 11
14 Lead Cavity DIP (J)



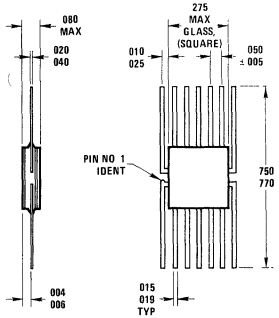
Package 12
16 Lead Cavity DIP (J)



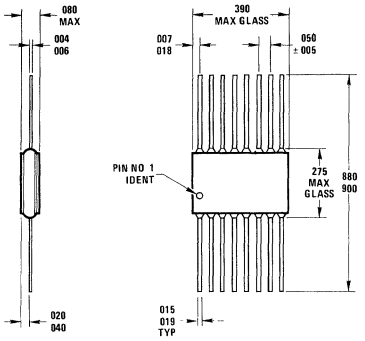
Package 13
24 Lead Cavity DIP (J)



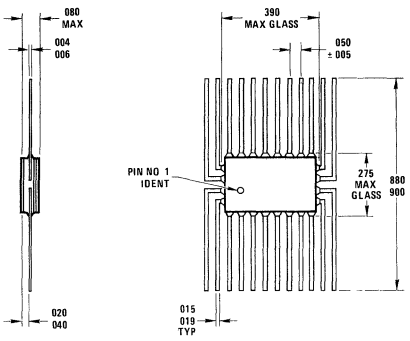
Package 14
10 Lead Flat Package (F)



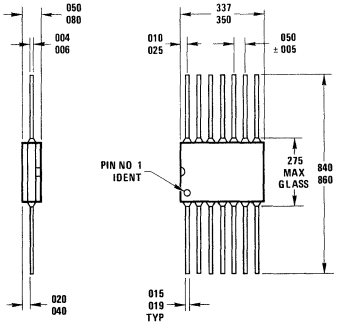
Package 15
14 Lead Flat Package (F)



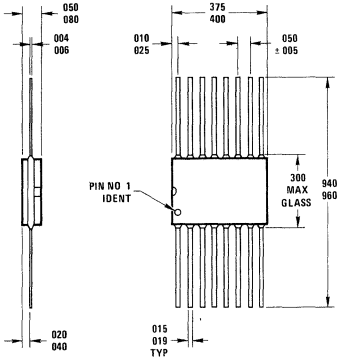
Package 16
16 Lead Flat Package (F)



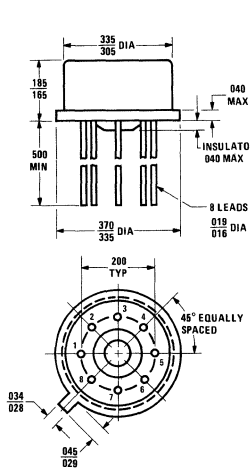
Package 17
24 Lead Flat Package (F)



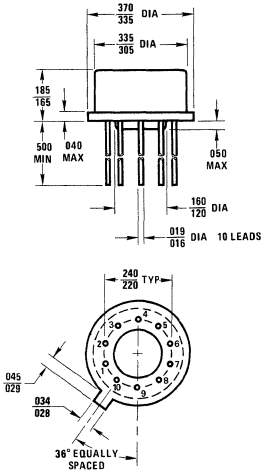
Package 18
14 Lead Flat Package (W)



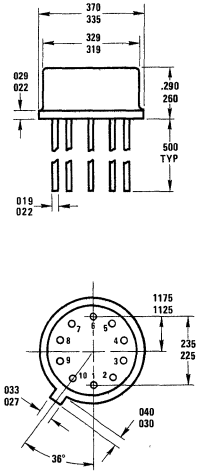
Package 19
16 Lead Flat Package (W)



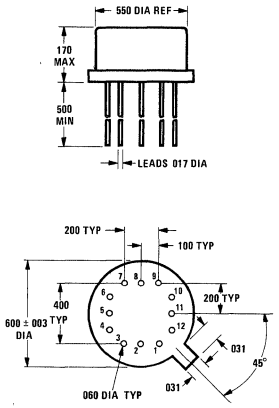
Package 20
8 Lead Metal Can Package (H)



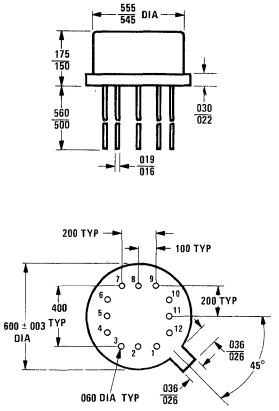
Package 21
10 Lead Metal Can Package (H)



Package 22
10 Lead Metal Can Package (H)
(Hybrids Only)



Package 23
12 Lead TO-8 Metal Can Package (G)
(Hybrids Only)



Package 24
12 Lead TO-8 Metal Can Package (G)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
001	.0254	.010	254	.100	2.54
002	0508	020	.508	.200	5.08
.003	.0762	.030	.762	300	7.62
004	1016	.040	1.016	400	10.16
005	.1270	.050	1.270	500	12 70
.006	.1524	060	1.524	600	15.24
007	1778	.070	1.778	700	17.78
.008	2032	.080	2.032	.800	20.32
.009	2286	090	2.286	900	22.86

All package dimensions are in inches.

Available Digital Applications Literature

The following is a listing of Digital applications literature. This literature, plus information on National's other product lines, is available through our sales offices, representatives, distributors, or our headquarters in Santa Clara.

application notes

AN-12	Applications of the DM7200/DM8200 Digital Comparator
AN-17	Programmable Divider Applications
AN-22	Integrated Circuits for Digital Data Transmissions
AN-35	High-Speed TTL Adders
AN-36	TTL MSI Applications
AN-37	TTL MSI Multiplexers and Demultiplexers
AN-43	TRI-STATE® Logic in Modular Systems
AN-45	Characteristics and Applications of TRI-STATE® IC's
AN-47	TRI-STATE® Logic in High-Speed Memories of Microprogrammed Computers
AN-49	Pin Diode Drivers
AN-60	A Method of Implementing Stacks with Existing Minicomputer Memory
AN-61	The Application of ROMs
AN-68	Using TRI-STATE® Logic for "Rubber-Band" Memories
AN-73	TRI-STATE® Logic Applied in a Computer System Can Reduce System Cost and Provide Added Performance
AN-84	Driving 7-Segment Gas Discharge Display Tubes with National Semiconductor Circuits

Notes

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15300 Ventura Boulevard, Suite 305
Sherman Oaks, California 91403
(213) 783-8272
TWX: 910-495-1773

DISTRICT SALES OFFICE
17452 Irvine Boulevard, Suite 2
Tustin, California 92680
(714) 832-8113
TWX: 910-595-1523

FLORIDA
REGIONAL SALES OFFICE
2721 South Bayshore Drive, Suite 121
Miami, Florida 33133
(305) 446-8309
TWX: 810-848-9725

ILLINOIS
NORTH-CENTRAL REGIONAL OFFICE
800 E. Northwest Highway, Suite 1060
Palatine, Illinois 60067
(312) 693-2660
TWX: 910-693-4805

KANSAS
DISTRICT SALES OFFICE
13201 West 82nd Street
Lenexa, Kansas 66215
(816) 358-8102

MARYLAND
REGIONAL SALES OFFICE
300 Hospital Drive, No. 232
Glen Burnie, Maryland 21061
(301) 760-5220
TWX: 710-861-0519

MASSACHUSETTS
NORTH-EAST REGIONAL OFFICE
No. 3 New England, Exec. Office Park
Burlington, Massachusetts 01803
(617) 273-1350
TWX: 710-332-0166

NEW JERSEY/NEW YORK CITY
MID-ATLANTIC REGIONAL OFFICE
301 Sylvan Avenue
Englewood Cliffs, New Jersey 07632
(201) 871-4410
TWX: 710-991-9734

NEW YORK (UPSTATE)
DISTRICT SALES OFFICE
104 Pickard Drive
Syracuse, New York 13211
(315) 455-5858

OHIO/PENNSYLVANIA/
W. VIRGINIA/KENTUCKY
EAST-CENTRAL REGIONAL OFFICE
Financial South Building
5335 Far Hills, Suite 214
Dayton, Ohio 45429
(513) 434-0097

OREGON
DISTRICT SALES OFFICE
P.O. Box "B"
Beaverton, Oregon 97005
(503) 643-5445

TEXAS
SOUTH-CENTRAL REGIONAL OFFICE
5925 Forest Lane, Suite 205
Dallas, Texas 75230
(214) 233-6801
TWX: 910-860-5091

INTERNATIONAL SALES OFFICES

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NATIONAL SEMICONDUCTOR
ELECTRONICS PTY. LTD.
Cnr. Stud Road & Mountain Highway
Bayswater, Victoria 3153
Australia
Telephone: 729-0733
Telex: 32096

CANADA
NATIONAL SEMICONDUCTOR LTD.
1111 Finch Avenue West
Downsview, Ontario, Canada
(416) 635-9880
TWX: 610-492-2510

DENMARK
NATIONAL SEMICONDUCTOR
SCANDINAVIA
Vordingborggade 22
2100 Copenhagen
Denmark
Telephone: (01) 92-OBRO-5610
Telex: DK 6827 MAGNA

ENGLAND
NATIONAL SEMICONDUCTOR (UK) LTD.
The Precinct
Broxbourne, Hertfordshire
England
Telephone: 69571
Telex: 267-204

FRANCE
NATIONAL SEMICONDUCTOR
FRANCE, S.A.R.L.
40 Boulevard Felix Faure
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Telephone: 253 60 50
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HONG KONG
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HONG KONG LTD.
9 Lai Yip Street
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WEST GERMANY
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8000 Munchen 81
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